

SN74CBTLV16211 LOW-VOLTAGE 24-BIT FET BUS SWITCH

SCDS043I – DECEMBER 1997 – REVISED OCTOBER 2003

- Member of the Texas Instruments Widebus™ Family
- 5-Ω Switch Connection Between Two Ports
- Rail-to-Rail Switching on Data I/O Ports
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

description/ordering information

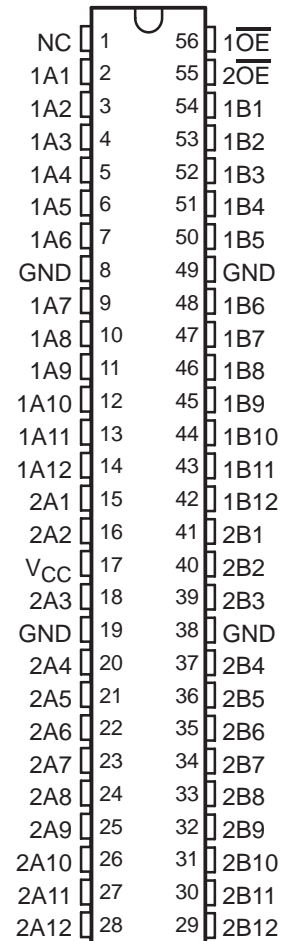
The SN74CBTLV16211 provides 24 bits of high-speed bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as dual 12-bit bus switches with separate output-enable (\overline{OE}) inputs. It can be used as two 12-bit bus switches or as one 24-bit bus switch. When \overline{OE} is low, the associated 12-bit bus switch is on, and port A is connected to port B. When \overline{OE} is high, the switch is open, and the high-impedance state exists between the two ports.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

DGG, DGV, OR DL PACKAGE (TOP VIEW)



NC – No internal connection

ORDERING INFORMATION

T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tube	SN74CBTLV16211DL	CBTLV16211
		Tape and reel	SN74CBTLV16211DLR	
	TSSOP – DGG	Tape and reel	SN74CBTLV16211GR	CBTLV16211
	TVSOP – DGV	Tape and reel	SN74CBTLV16211VR	CN211

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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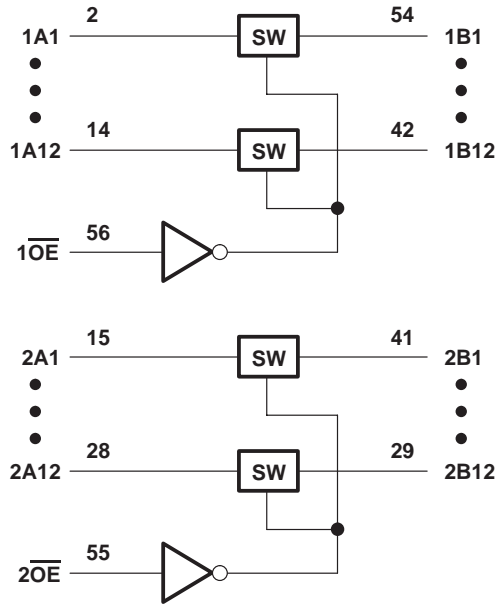
SN74CBTLV16211 LOW-VOLTAGE 24-BIT FET BUS SWITCH

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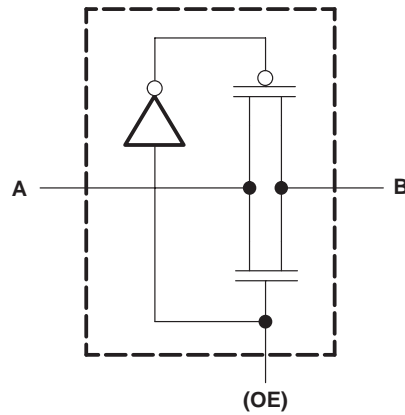
FUNCTION TABLE
(each 12-bit bus switch)

INPUT \overline{OE}	FUNCTION
L	A port = B port
H	Disconnect

logic diagram (positive logic)



simplified schematic, each FET switch



SN74CBTLV16211

LOW-VOLTAGE 24-BIT FET BUS SWITCH

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 4.6 V	
Input voltage range, V_I (see Note 1)	–0.5 V to 4.6 V	
Continuous channel current	128 mA	
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA	
Package thermal impedance, θ_{JA} (see Note 2):	DGG package	64°C/W
	DGV package	48°C/W
	DL package	56°C/W
Storage temperature range, T_{stg}	–65°C to 150°C	

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.3	3.6	V
V_{IH}	High-level control input voltage	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2	
V_{IL}	Low-level control input voltage	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	0.7	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	0.8	
T_A	Operating free-air temperature	–40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN74CBTLV16211

LOW-VOLTAGE 24-BIT FET BUS SWITCH

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		$V_{CC} = 3\text{ V}$,	$I_I = -18\text{ mA}$			-1.2	V
I_I		$V_{CC} = 3.6\text{ V}$,	$V_I = V_{CC}$ or GND			± 1	μA
I_{off}		$V_{CC} = 0$,	V_I or $V_O = 0$ to 3.6 V			10	μA
I_{CC}		$V_{CC} = 3.6\text{ V}$,	$I_O = 0$, $V_I = V_{CC}$ or GND			10	μA
$\Delta I_{CC}‡$	Control inputs	$V_{CC} = 3.6\text{ V}$,	One input at 3 V , Other inputs at V_{CC} or GND			300	μA
C_i	Control inputs	$V_I = 3.3\text{ V}$ or 0				4.5	pF
$C_{io(OFF)}$		$V_O = 3.3\text{ V}$ or 0 ,	$\overline{OE} = V_{CC}$			6.5	pF
$r_{on}§$	$V_{CC} = 2.3\text{ V}$, TYP at $V_{CC} = 2.5\text{ V}$	$V_I = 0$	$I_I = 64\text{ mA}$	5	8	Ω	
			$I_I = 24\text{ mA}$	5	8		
		$V_I = 1.7\text{ V}$,	$I_I = 15\text{ mA}$	27	40		
	$V_{CC} = 3\text{ V}$	$V_I = 0$	$I_I = 64\text{ mA}$	5	7		
			$I_I = 24\text{ mA}$	5	7		
		$V_I = 2.4\text{ V}$,	$I_I = 15\text{ mA}$	10	15		

† All typical values are at $V_{CC} = 3.3\text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

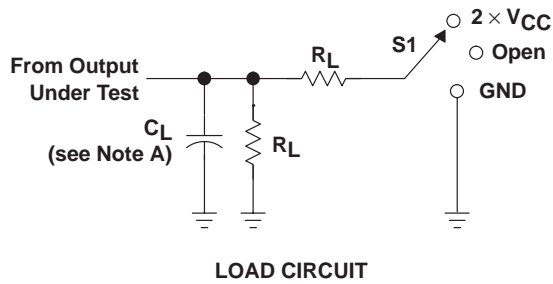
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
$t_{pd}¶$	A or B	B or A	0.15		0.25		ns
t_{en}	\overline{OE}	A or B	1	7	1	6.2	ns
t_{dis}	\overline{OE}	A or B	1	7.2	1	7.7	ns

¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

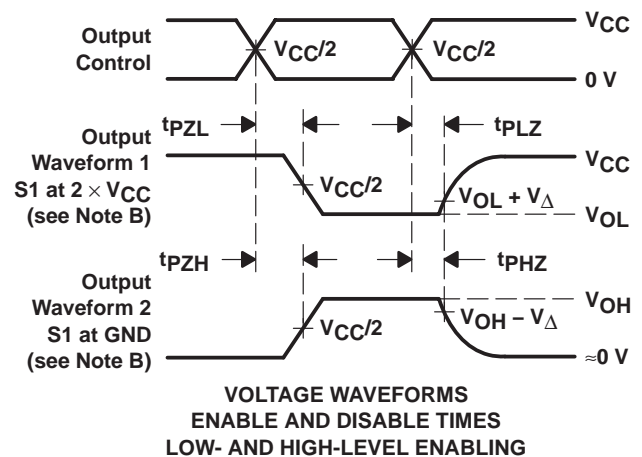
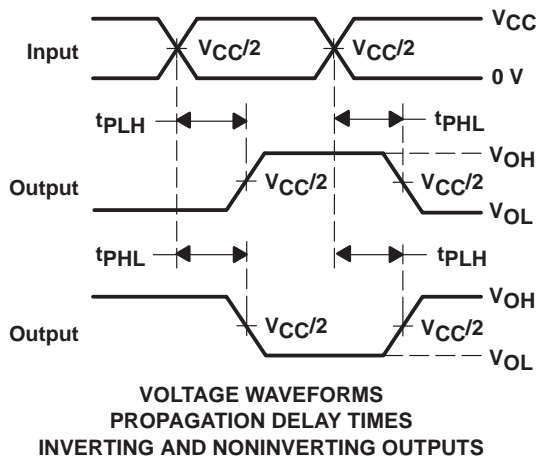
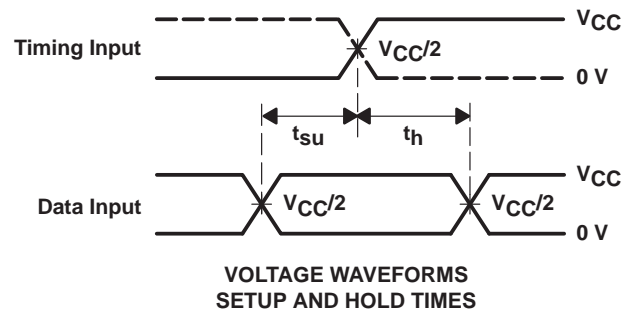
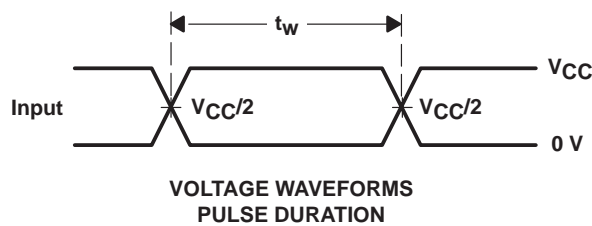


PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

V_{CC}	C_L	R_L	V_{Δ}
$2.5\text{ V} \pm 0.2\text{ V}$	30 pF	500 Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	50 pF	500 Ω	0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74CBTLV16211DLRG4	Active	Production	SSOP (DL) 56	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV16211
74CBTLV16211GRG4	Active	Production	TSSOP (DGG) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV16211
SN74CBTLV16211DL	Active	Production	SSOP (DL) 56	20 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV16211
SN74CBTLV16211DL.Z	Active	Production	SSOP (DL) 56	20 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV16211
SN74CBTLV16211DLR	Active	Production	SSOP (DL) 56	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV16211
SN74CBTLV16211DLR.Z	Active	Production	SSOP (DL) 56	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV16211
SN74CBTLV16211GR	Active	Production	TSSOP (DGG) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV16211
SN74CBTLV16211GR.Z	Active	Production	TSSOP (DGG) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV16211
SN74CBTLV16211VR	Active	Production	TVSOP (DGV) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CN211
SN74CBTLV16211VR.Z	Active	Production	TVSOP (DGV) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CN211

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



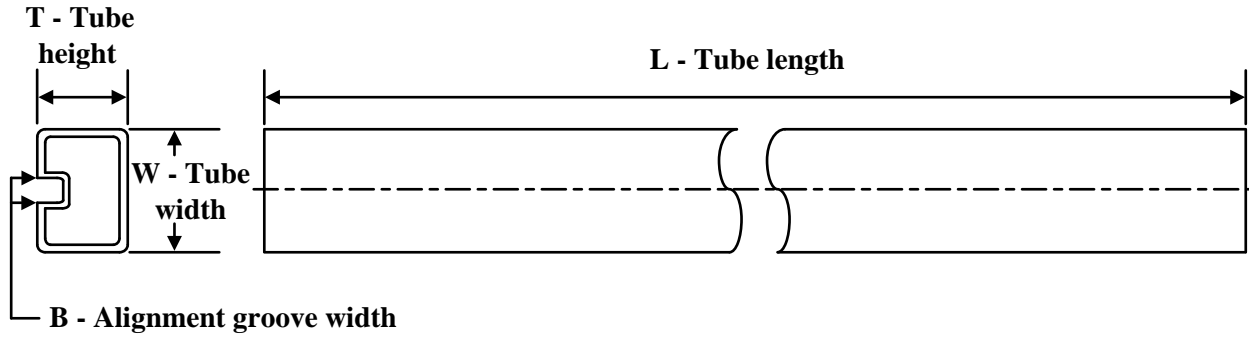
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBTLV16211DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
SN74CBTLV16211GR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74CBTLV16211VR	TVSOP	DGV	56	2000	330.0	24.4	6.8	11.7	1.6	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBTLV16211DLR	SSOP	DL	56	1000	367.0	367.0	55.0
SN74CBTLV16211GR	TSSOP	DGG	56	2000	367.0	367.0	45.0
SN74CBTLV16211VR	TVSOP	DGV	56	2000	367.0	367.0	45.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74CBTLV16211DL	DL	SSOP	56	20	473.7	14.24	5110	7.87
SN74CBTLV16211DL.Z	DL	SSOP	56	20	473.7	14.24	5110	7.87

DGV (R-PDSO-G**)

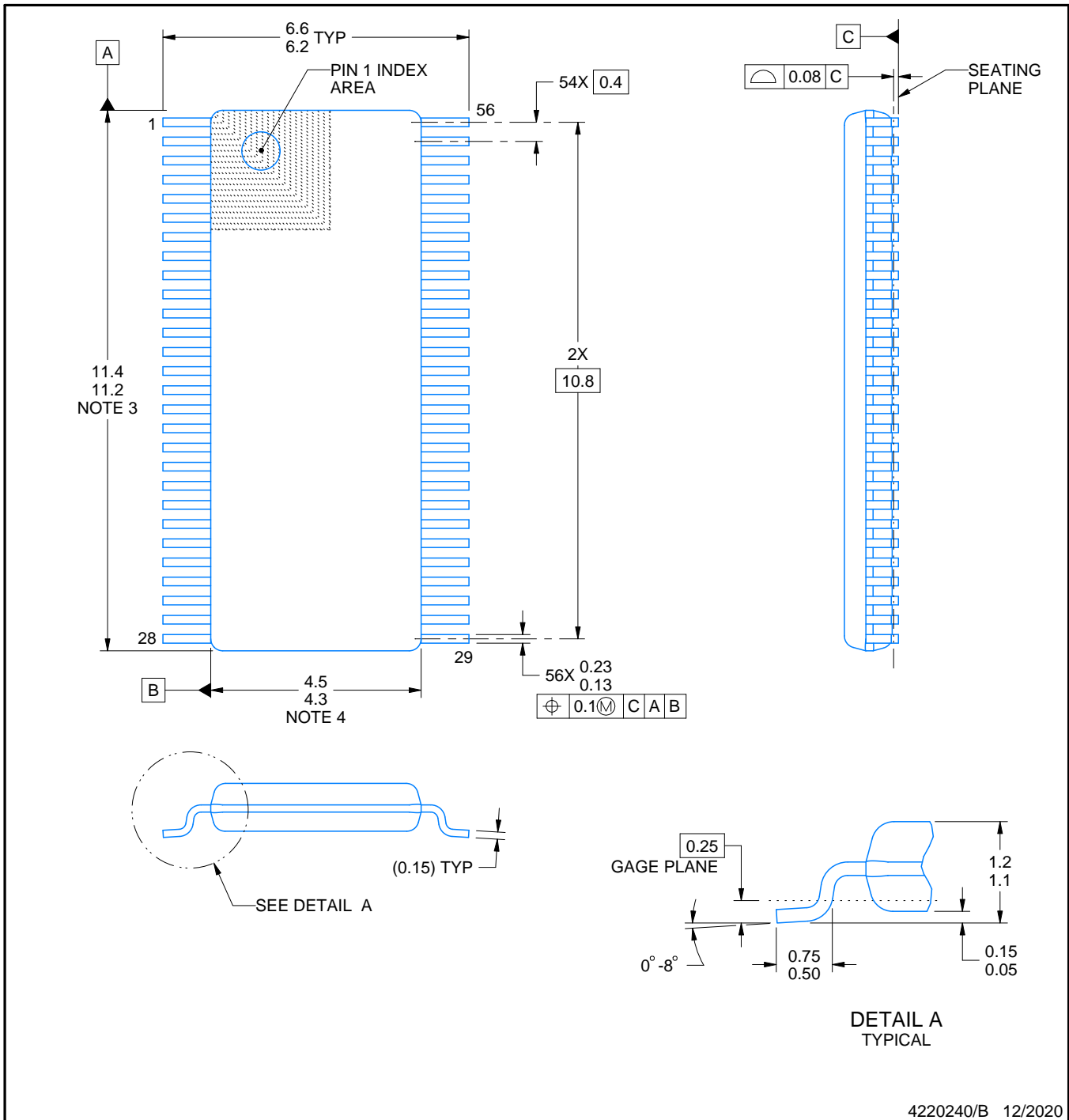
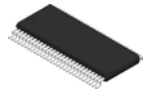
PLASTIC SMALL-OUTLINE

24 PINS SHOWN



4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194



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NOTES:

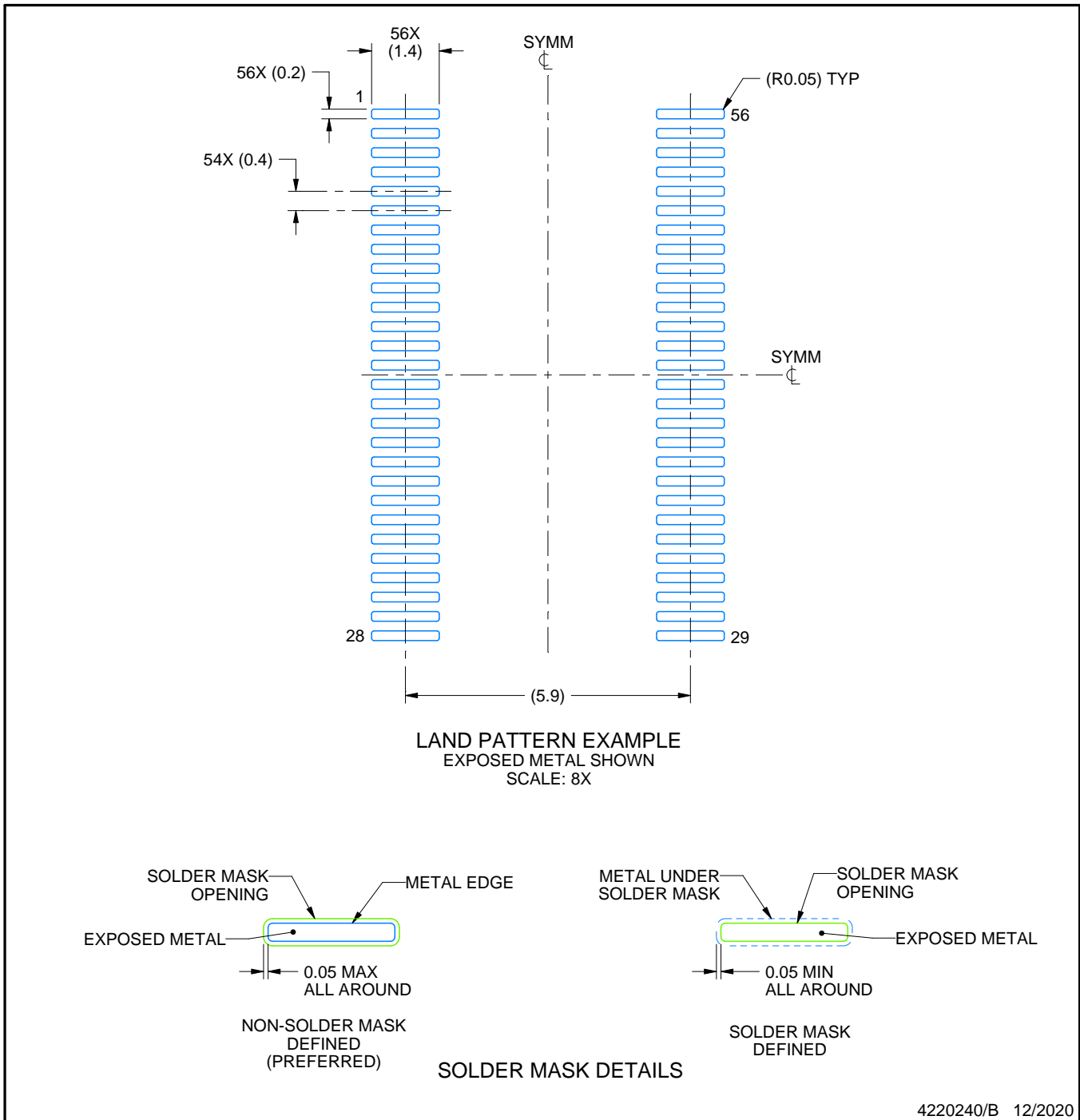
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-194.

EXAMPLE BOARD LAYOUT

DGV0056A

TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

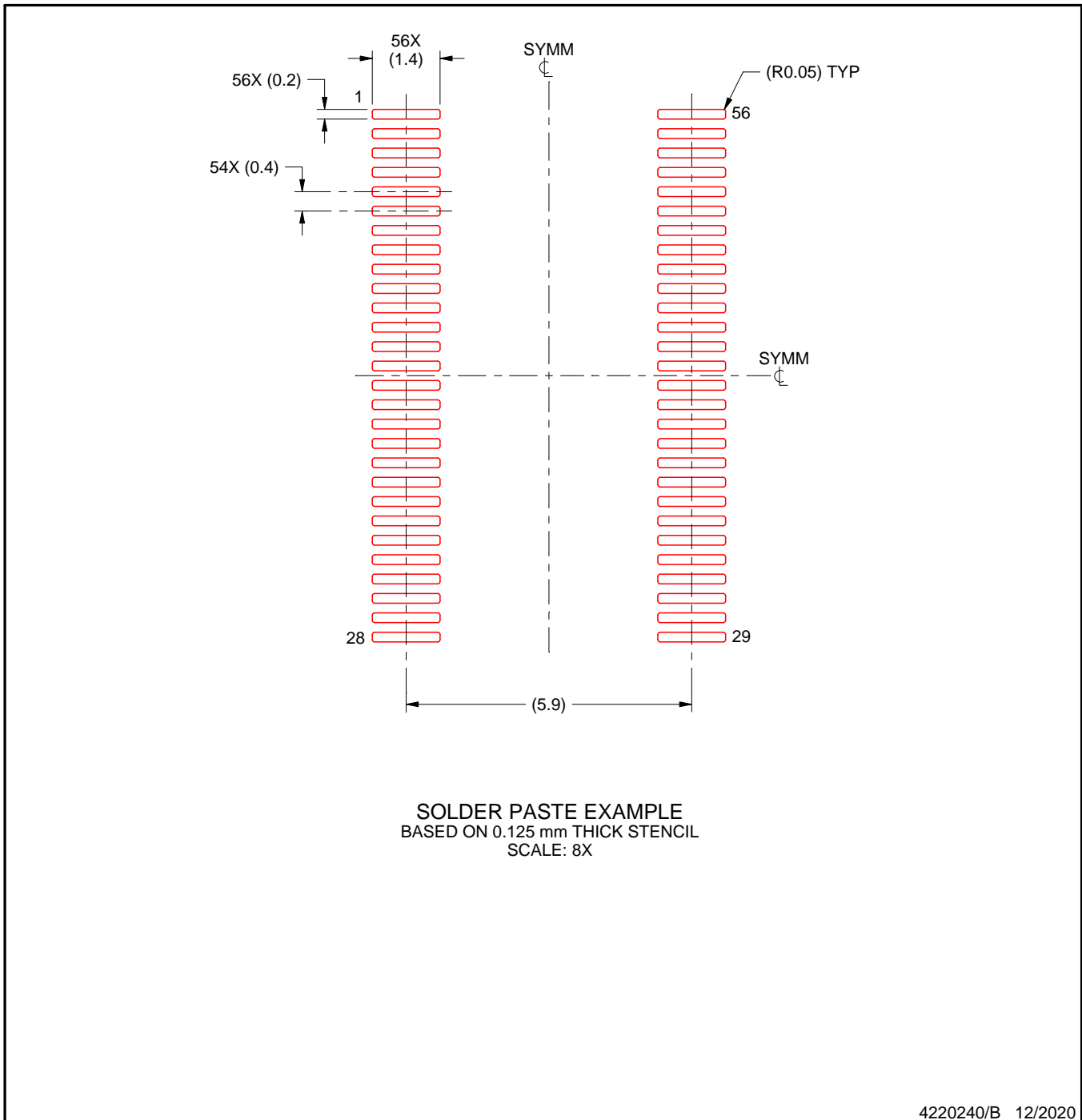
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGV0056A

TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



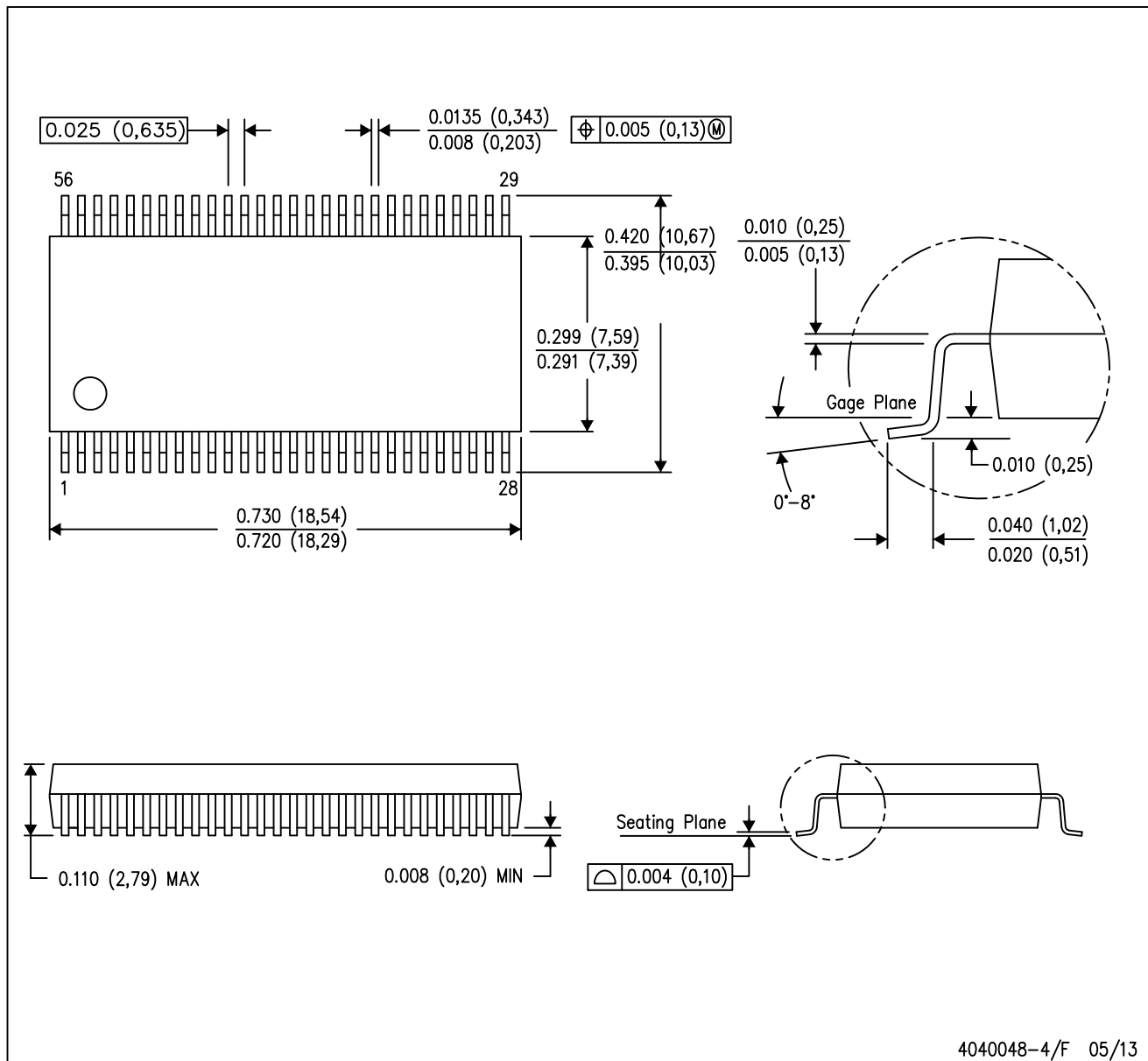
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MO-118

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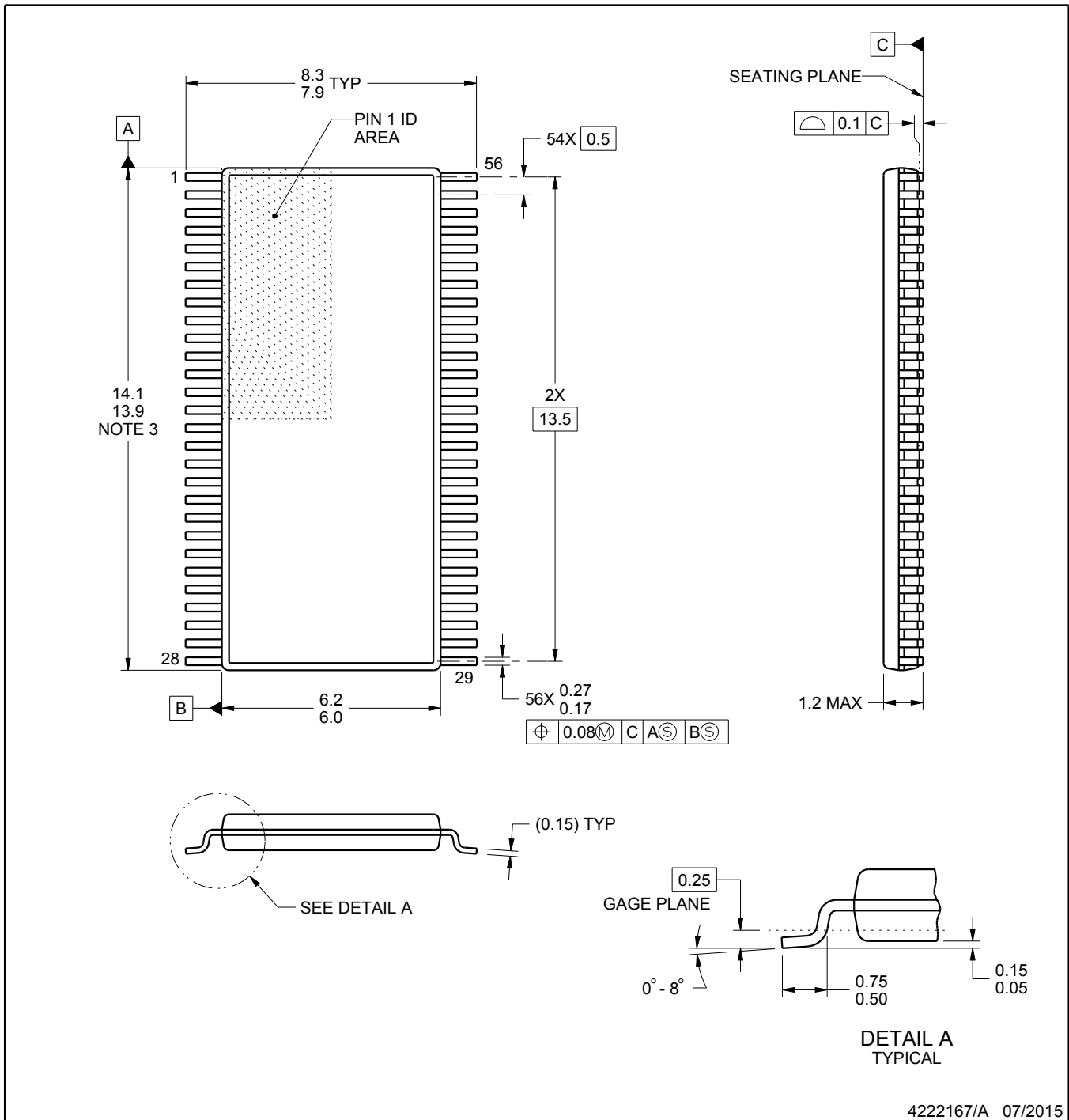
DGG0056A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4222167/A 07/2015

NOTES:

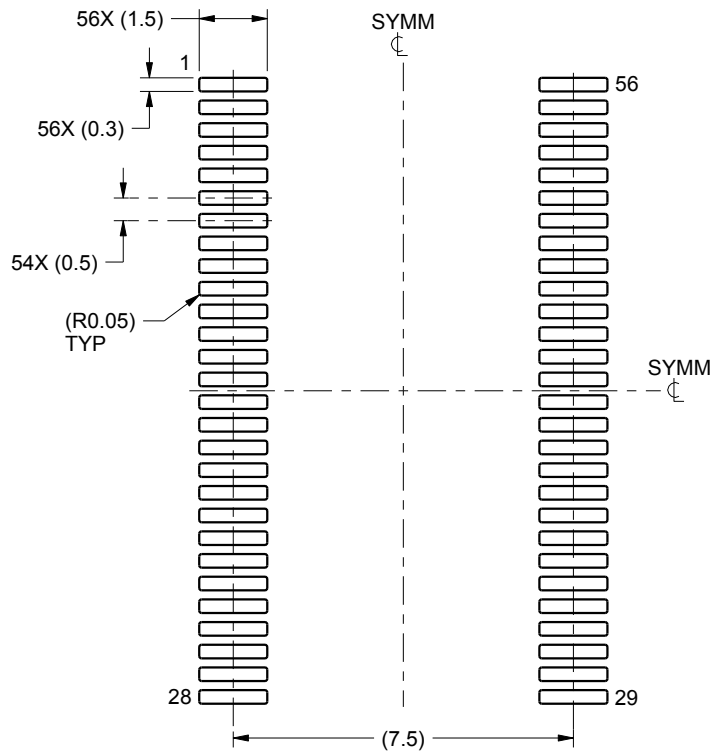
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

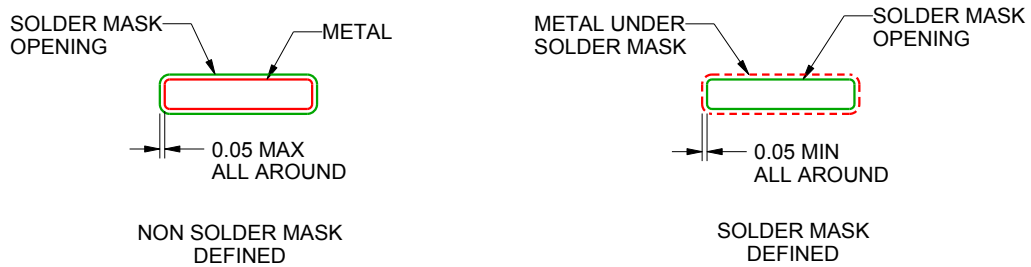
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

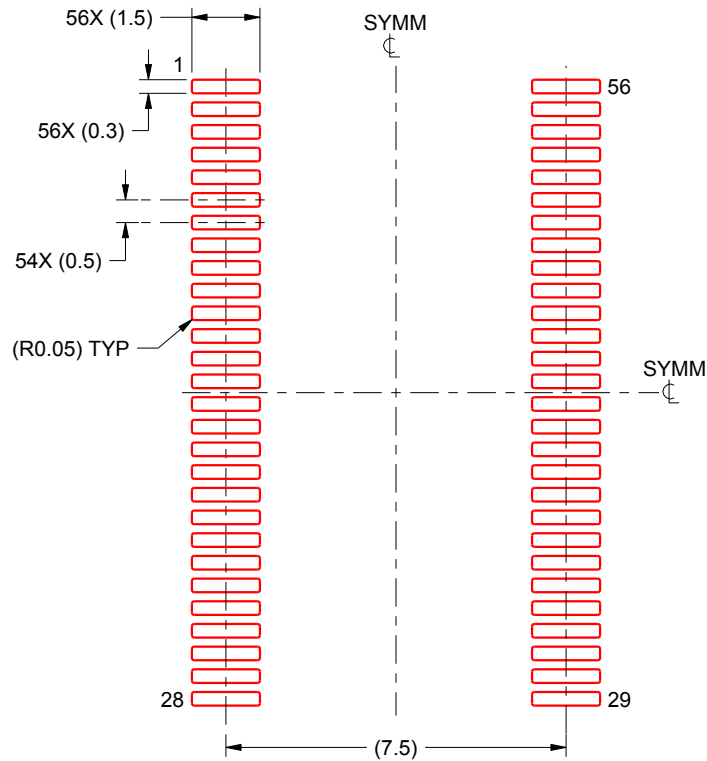
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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