The SN74CBTS3384 provides ten bits of high-speed TTL-compatible bus switching with Schottky diodes on the I/Os to clamp undershoot. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as two 5-bit bus switches with separate output-enable (OE) inputs. When OE is low, the switch is on, and port A is connected to port B. When OE is high, the switch is open, and the high-impedance state exists between the two ports.

ORDERING INFORMATION

<table>
<thead>
<tr>
<th>T_A</th>
<th>PACKAGE†</th>
<th>ORDERABLE PART NUMBER</th>
<th>TOP-SIDE MARKING</th>
</tr>
</thead>
<tbody>
<tr>
<td>−40°C to 85°C</td>
<td>SOIC – DW</td>
<td>Tube</td>
<td>SN74CBTS3384DW</td>
</tr>
<tr>
<td></td>
<td>SSOP – DB</td>
<td>Tape and reel</td>
<td>SN74CBTS3384DBR</td>
</tr>
<tr>
<td></td>
<td>SSOP (QSOP) – DBQ</td>
<td>Tape and reel</td>
<td>SN74CBTS3384DBQR</td>
</tr>
<tr>
<td></td>
<td>TSSOP – PW</td>
<td>Tube</td>
<td>SN74CBTS3384PWR</td>
</tr>
<tr>
<td></td>
<td>TVSOP – DGV</td>
<td>Tape and reel</td>
<td>SN74CBTS3384DGVR</td>
</tr>
</tbody>
</table>

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

(each 5-bit bus switch)

<table>
<thead>
<tr>
<th>INPUTS</th>
<th>INPUTS/OUTPUTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>1OE</td>
<td>2OE</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
</tr>
</tbody>
</table>

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
logic diagram (positive logic)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

- Supply voltage range, $V_{CC}$: $-0.5$ V to $7$ V
- Input voltage range, $V_I$ (see Note 1): $-0.5$ V to $7$ V
- Continuous channel current: $128$ mA
- Input clamp current, $I_{IK}$ ($V_{I/O} < 0$): $-50$ mA
- Package thermal impedance, $\theta_{JA}$ (see Note 2):
  - DB package: $63^\circ$C/W
  - DBQ package: $61^\circ$C/W
  - DGV package: $86^\circ$C/W
  - DW package: $46^\circ$C/W
  - PW package: $88^\circ$C/W
- Storage temperature range, $T_{stg}$: $-65^\circ$C to $150^\circ$C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td>4</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>2</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td></td>
<td>0.8</td>
<td>V</td>
</tr>
<tr>
<td>$T_{A}$</td>
<td>$-40$</td>
<td>$85$</td>
<td>°C</td>
</tr>
</tbody>
</table>

NOTE 3: All unused control inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP†</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IK}$</td>
<td>A or B inputs</td>
<td>$V_{CC} = 4.5 , V$, $I_I = -18 , mA$</td>
<td>-0.6</td>
<td>-1.2</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Control inputs</td>
<td>$V_{CC} = 5.5 , V$, $V_I = 5.5 , V$</td>
<td>150</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>$I_I$</td>
<td>$I_{IL}$</td>
<td>$V_{CC} = 5.5 , V$, $V_I = GND$</td>
<td>-1</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td>$I_{IH}$</td>
<td>$V_{CC} = 5.5 , V$, $V_I = 5.5 , V$</td>
<td>3</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>$I_{CC}$</td>
<td>Control inputs</td>
<td>$V_{CC} = 5.5 , V$, $I_O = 0$, $V_I = V_{CC}$ or GND</td>
<td>2.5</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$\Delta I_{CC}$</td>
<td>Control inputs</td>
<td>$V_{CC} = 5.5 , V$, One input at 3.4 $V$, Other inputs at $V_{CC}$ or GND</td>
<td>6</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>$C_i$</td>
<td>Control inputs</td>
<td>$V_I = 3 , V$ or 0</td>
<td>6.5</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>$C_{io(OFF)}$</td>
<td>$V_O = 3 , V$ or 0, $\overline{OE} = V_{CC}$</td>
<td>6</td>
<td></td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>$r_{on}$</td>
<td>$V_{CC} = 4 , V$, TYP at $V_{CC} = 4 , V$</td>
<td>14</td>
<td></td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_{CC} = 4.5 , V$, $V_I = 2.4 , V$, $I_I = 15 , mA$</td>
<td>5</td>
<td></td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_I = 0$, $I_I = 64 , mA$</td>
<td>5</td>
<td></td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$I_I = 30 , mA$</td>
<td>7</td>
<td></td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_I = 2.4 , V$, $I_I = 15 , mA$</td>
<td>10</td>
<td></td>
<td>Ω</td>
<td></td>
</tr>
</tbody>
</table>

†All typical values are at $V_{CC} = 5 \, V$ (unless otherwise noted). $T_A = 25^\circ C$.
‡This is the increase in supply current for each input that is at the specified TTL voltage level, rather than $V_{CC}$ or GND.
§Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \, pF$ (unless otherwise noted) (see Figure 1)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>$V_{CC} = 4 , V$</th>
<th>$V_{CC} = 5 , V \pm 0.5 , V$</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{pd}$</td>
<td>A or B</td>
<td>B or A</td>
<td>0.35</td>
<td>0.25</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{en}$</td>
<td>$\overline{OE}$</td>
<td>A or B</td>
<td>6.2</td>
<td>1.9</td>
<td>5.7</td>
</tr>
<tr>
<td>$t_{dis}$</td>
<td>$\overline{OE}$</td>
<td>A or B</td>
<td>5.5</td>
<td>2.1</td>
<td>5.2</td>
</tr>
</tbody>
</table>

†The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
PARAMETER MEASUREMENT INFORMATION

**LOAD CIRCUIT**

- From Output Under Test
- $C_L = 50 \text{ pF}$ (see Note A)
- 7 V
- Open
- GND
- 500 $\Omega$

**VOLTAGE WAVEFORMS**

**PROPAGATION DELAY TIMES**

**ENABLE AND DISABLE TIMES**

**TEST** | **S1**
---|---
$t_{pd}$ | Open
$t_{PLZ}$/$t_{PZL}$ | 7 V
$t_{PHZ}$/$t_{PZH}$ | Open

**NOTES:**

A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.
E. $t_{PLZ}$ and $t_{PZH}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PHZ}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

**Figure 1. Load Circuit and Voltage Waveforms**

---

**Texas Instruments**

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## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN74CBTS3384DW</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>DW</td>
<td>24</td>
<td>25</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>CBTS3384</td>
<td>Samples</td>
</tr>
<tr>
<td>SN74CBTS3384PW</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>PW</td>
<td>24</td>
<td>60</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>CR384</td>
<td>Samples</td>
</tr>
<tr>
<td>SN74CBTS3384PWR</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>PW</td>
<td>24</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>CR384</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSCLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead/Ball Finish** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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# TAPE AND REEL INFORMATION

**Dimensions**

- **Device**: SN74CBTS3384PWR
- **Package Type**: TSSOP
- **Drawing**: PW
- **Pins**: 24
- **SPQ**: 2000

**Dimensions (mm)**

- **Reel Diameter**: 330.0
- **Reel Width W1**: 16.4
- **A0**: 6.95
- **B0**: 8.3
- **K0**: 1.6
- **P1**: 8.0
- **W**: 16.0
- **Pin1 Quadrant**: Q1

*All dimensions are nominal.*

## TAPE DIMENSIONS

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

- **Q1**, **Q2**, **Q3**, **Q4**: Pocket Quadrants
- **Sprocket Holes**: User Direction of Feed

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Pack Materials-Page 1
### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN74CBTS3384PWR</td>
<td>TSSOP</td>
<td>PW</td>
<td>24</td>
<td>2000</td>
<td>367.0</td>
<td>367.0</td>
<td>38.0</td>
</tr>
</tbody>
</table>
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.
NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
D. Falls within JEDEC MS–013 variation AD.
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