This synchronous, presettable, 4-bit binary counter has internal carry look-ahead circuitry for use in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable (ENP, ENT) inputs and internal gating. This mode of operation eliminates the output counting spikes that normally are associated with asynchronous (ripple-clock) counters. However, counting spikes can occur on the ripple-carry (RCO) output. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of CLK.

This counter is fully programmable. That is, it can be preset to any number between 0 and 15. Because presetting is synchronous, a low logic level at the load (LOAD) input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of ENP and ENT.

The clear function is synchronous, and a low logic level at the clear (CLR) input sets all four of the flip-flop outputs to low after the next low-to-high transition of the clock, regardless of the levels of ENP and ENT. This synchronous clear allows the count length to be modified easily by decoding the Q outputs for the maximum count desired. The active-low output of the gate used for decoding is connected to the clear input to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications, without additional gating. This function is implemented by the ENP and ENT inputs and an RCO output. Both ENP and ENT must be high to count, and ENT is fed forward to enable RCO. RCO, thus enabled, produces a high-logic-level pulse while the count is 15 (HHHH). The high-logic-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at ENP or ENT are allowed, regardless of the level of CLK.

The SN74F163A features a fully independent clock circuit. Changes at ENP, ENT, or LOAD that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the setup and hold times.

### ORDERING INFORMATION

<table>
<thead>
<tr>
<th>TA</th>
<th>PACKAGE†</th>
<th>ORDERABLE PART NUMBER</th>
<th>TOP-SIDE MARKING</th>
</tr>
</thead>
<tbody>
<tr>
<td>0°C to 70°C</td>
<td>PDIP – N</td>
<td>Tube</td>
<td>SN74F163AN</td>
</tr>
<tr>
<td></td>
<td>SOIC – D</td>
<td>Tube</td>
<td>SN74F163AD</td>
</tr>
<tr>
<td></td>
<td>SSOP – DB</td>
<td>Tape and reel</td>
<td>SN74F163ADR</td>
</tr>
</tbody>
</table>

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
state diagram

- 0 → 1 → 2 → 3 → 4
- 15
- 14
- 13
- 12 → 11 → 10 → 9 → 8
- 5
- 6
- 7
logic diagram (positive logic)
logic symbol, each flip-flop

logic diagram, each flip-flop (positive logic)
typical clear, preset, count, and inhibit sequences

The following timing sequence is illustrated below:

1. Clear outputs to zero
2. Preset to binary 12
3. Count to 13, 14, 15, 0, 1, and 2
4. Inhibit
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

- Supply voltage range, \( V_{CC} \) ........................................... -0.5 V to 7 V
- Input voltage range, \( V_I \) (see Note 1) .................................. -1.2 V to 7 V
- Input current range ...................................................... -30 mA to 5 mA
- Voltage range applied to any output in the high state ............. -0.5 V to \( V_{CC} \)
- Current into any output in the low state ............................. 40 mA
- Package thermal impedance, \( \theta_JA \) (see Note 2): D package ........ 73°C/W
- DB package .................................................. 82°C/W
- N package ................................................. 67°C/W

Storage temperature range, \( T_{stg} \) ......................................... -65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input voltage ratings may be exceeded provided the input current ratings are observed.
   2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{CC} )</td>
<td>Supply voltage</td>
<td>4.5</td>
<td>5</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>( V_IH )</td>
<td>High-level input voltage</td>
<td>2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{IL} )</td>
<td>Low-level input voltage</td>
<td>0.8</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( I_{IK} )</td>
<td>Input clamp current</td>
<td>-18</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>( I_{OH} )</td>
<td>High-level output current</td>
<td>-1</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>( I_{OL} )</td>
<td>Low-level output current</td>
<td>20</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>( T_A )</td>
<td>Operating free-air temperature</td>
<td>0</td>
<td>70</td>
<td></td>
<td>°C</td>
</tr>
</tbody>
</table>

NOTE 3: All unused inputs of the device must be held at \( V_{CC} \) or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP‡</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{IK} )</td>
<td>( V_{CC} = 4.5 \text{ V}, \ I_I = -18 \text{ mA} )</td>
<td>2.5</td>
<td>3.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{OH} )</td>
<td>( V_{CC} = 4.5 \text{ V}, \ I_OH = -1 \text{ mA} )</td>
<td>2.7</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{OL} )</td>
<td>( V_{CC} = 4.5 \text{ V}, \ I_OH = V_{CC} = 20 \text{ mA} )</td>
<td>0.3</td>
<td>0.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( I_I )</td>
<td>( V_{CC} = 5.5 \text{ V}, \ V_I = 7 \text{ V} )</td>
<td>0.1</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>( I_{IH} )</td>
<td>( V_{CC} = 5.5 \text{ V}, \ V_I = 2.7 \text{ V} )</td>
<td>20</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>( I_{IL} )</td>
<td>ENP, CLK, A, B, C, D</td>
<td>0.6</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>ENT, LOAD</td>
<td>-1.2</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>CLR</td>
<td>-1.2</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>( I_{OS} )</td>
<td>( V_{CC} = 5.5 \text{ V}, \ V_O = 0 )</td>
<td>-60</td>
<td>-150</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>( I_{CC} )</td>
<td>( V_{CC} = 5.5 \text{ V} )</td>
<td>37</td>
<td>55</td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

‡ All typical values are at \( V_{CC} = 5 \text{ V}, \ T_A = 25^\circ \text{C} \).
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
The image contains a technical document from Texas Instruments, detailing the timing requirements and switching characteristics of the SN74F163A synchronous 4-bit binary counter.

### Timing Requirements

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Unit</th>
<th>MIN</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>f&lt;sub&gt;clock&lt;/sub&gt;</td>
<td>Clock frequency</td>
<td>0</td>
<td>100 MHz</td>
</tr>
<tr>
<td>f&lt;sub&gt;W&lt;/sub&gt;</td>
<td>Pulse duration</td>
<td>5</td>
<td>5 ns</td>
</tr>
<tr>
<td>t&lt;sub&gt;su&lt;/sub&gt;</td>
<td>Setup time</td>
<td>11</td>
<td>11.5 ns</td>
</tr>
<tr>
<td>t&lt;sub&gt;hold&lt;/sub&gt;</td>
<td>Hold time</td>
<td>2</td>
<td>2 ns</td>
</tr>
</tbody>
</table>

### Switching Characteristics

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>V&lt;sub&gt;CC&lt;/sub&gt; = 5 V, T&lt;sub&gt;A&lt;/sub&gt; = 25°C</th>
<th>V&lt;sub&gt;CC&lt;/sub&gt; = 4.5 V TO 5.5 V, T&lt;sub&gt;A&lt;/sub&gt; = MIN TO MAX†</th>
</tr>
</thead>
<tbody>
<tr>
<td>f&lt;sub&gt;max&lt;/sub&gt;</td>
<td>f&lt;sub&gt;max&lt;/sub&gt;</td>
<td>100</td>
<td>120 MHz</td>
<td>90</td>
</tr>
<tr>
<td>t&lt;sub&gt;PLH&lt;/sub&gt; (CLK LOAD high)</td>
<td>Any Q</td>
<td>2.7</td>
<td>5.1</td>
<td>7.5 ns</td>
</tr>
<tr>
<td>t&lt;sub&gt;PHL&lt;/sub&gt; (CLK LOAD low)</td>
<td>Any Q</td>
<td>3.2</td>
<td>5.6</td>
<td>8.5 ns</td>
</tr>
<tr>
<td>t&lt;sub&gt;PLH&lt;/sub&gt;</td>
<td>RCO</td>
<td>4.2</td>
<td>9.6</td>
<td>14 ns</td>
</tr>
<tr>
<td>t&lt;sub&gt;PHL&lt;/sub&gt;</td>
<td>RCO</td>
<td>1.7</td>
<td>4.1</td>
<td>7.5 ns</td>
</tr>
</tbody>
</table>

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 4: Load circuits and waveforms are shown in Figure 1.
PARAMETER MEASUREMENT INFORMATION

<table>
<thead>
<tr>
<th>TEST</th>
<th>S1</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_{PLH}/t_{PHL}</td>
<td>Open</td>
</tr>
<tr>
<td>t_{PLZ}/t_{PZL}</td>
<td>7 V</td>
</tr>
<tr>
<td>t_{PHZ}/t_{PZH}</td>
<td>Open</td>
</tr>
<tr>
<td>Open Collector</td>
<td>7 V</td>
</tr>
</tbody>
</table>

LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS

VOLTAGE WAVEFORMS
PULSE DURATION

Timing Input

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns, duty cycle = 50%.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead finish/Ball material</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN74F163AD</td>
<td>LIFEBUY</td>
<td>SOIC</td>
<td>D</td>
<td>16</td>
<td>40</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>F163A</td>
<td>Samples</td>
</tr>
<tr>
<td>SN74F163ADR</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>16</td>
<td>2500</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>F163A</td>
<td>Samples</td>
</tr>
<tr>
<td>SN74F163AN</td>
<td>ACTIVE</td>
<td>PDIP</td>
<td>N</td>
<td>16</td>
<td>25</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>N / A for Pkg Type</td>
<td>0 to 70</td>
<td>SN74F163AN</td>
<td>Samples</td>
</tr>
<tr>
<td>SN74F163ANE4</td>
<td>ACTIVE</td>
<td>PDIP</td>
<td>N</td>
<td>16</td>
<td>25</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>N / A for Pkg Type</td>
<td>0 to 70</td>
<td>SN74F163AN</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead finish/Ball material** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN74F163ADR</td>
<td>SOIC</td>
<td>D</td>
<td>16</td>
<td>2500</td>
<td>330.0</td>
<td>16.4</td>
<td>6.5</td>
<td>10.3</td>
<td>2.1</td>
<td>8.0</td>
<td>16.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>
### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN74F163ADR</td>
<td>SOIC</td>
<td>D</td>
<td>16</td>
<td>2500</td>
<td>340.5</td>
<td>336.1</td>
<td>32.0</td>
</tr>
<tr>
<td>Device</td>
<td>Package Name</td>
<td>Package Type</td>
<td>Pins</td>
<td>SPQ</td>
<td>L (mm)</td>
<td>W (mm)</td>
<td>T (µm)</td>
</tr>
<tr>
<td>--------------</td>
<td>--------------</td>
<td>--------------</td>
<td>------</td>
<td>-----</td>
<td>--------</td>
<td>--------</td>
<td>--------</td>
</tr>
<tr>
<td>SN74F163AD</td>
<td>D</td>
<td>SOIC</td>
<td>16</td>
<td>40</td>
<td>507</td>
<td>8</td>
<td>3940</td>
</tr>
<tr>
<td>SN74F163AN</td>
<td>N</td>
<td>PDIP</td>
<td>16</td>
<td>25</td>
<td>506</td>
<td>13.97</td>
<td>11230</td>
</tr>
<tr>
<td>SN74F163AN</td>
<td>N</td>
<td>PDIP</td>
<td>16</td>
<td>25</td>
<td>506</td>
<td>13.97</td>
<td>11230</td>
</tr>
<tr>
<td>SN74F163ANE4</td>
<td>N</td>
<td>PDIP</td>
<td>16</td>
<td>25</td>
<td>506</td>
<td>13.97</td>
<td>11230</td>
</tr>
<tr>
<td>SN74F163ANE4</td>
<td>N</td>
<td>PDIP</td>
<td>16</td>
<td>25</td>
<td>506</td>
<td>13.97</td>
<td>11230</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
⚠️ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.
⚠️ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.
E. Reference JEDEC MS-012 variation AC.
PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
⚠️ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
⚠️ The 20 pin end lead shoulder width is a vendor option, either half or full width.
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