

## SN74HC00-Q1 Automotive Quadruple 2-Input NAND Gates

### 1 Features

- AEC-Q100 Qualified for automotive applications:
  - Device temperature grade 1: –40°C to +125°C, T<sub>A</sub>
- Buffered inputs
- Positive and negative input clamp diodes
- Wide operating voltage range: 2 V to 6 V
- Supports fanout up to 10 LSTTL loads
- Significant power reduction compared to LSTTL logic ICs

### 2 Applications

- [Alarm / tamper detect circuit](#)
- S-R latch

### 3 Description

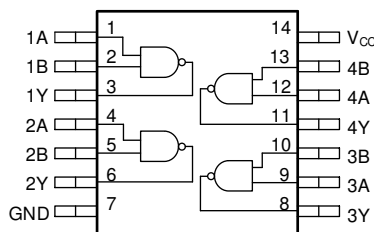
This device contains four independent 2-input NAND gates. Each gate performs the Boolean function  $Y = \overline{A \bullet B}$  in positive logic.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74HC00QDRQ1	SOIC (14)	8.70 mm x 3.90 mm
SN74HC00QPWRQ1	TSSOP (14)	5.00 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Functional pinout of the SN74HC00-Q1



## Table of Contents

<b>1 Features</b> .....	<b>1</b>	8.3 Feature Description .....	<b>7</b>
<b>2 Applications</b> .....	<b>1</b>	8.4 Device Functional Modes .....	<b>8</b>
<b>3 Description</b> .....	<b>1</b>	<b>9 Application and Implementation</b> .....	<b>9</b>
<b>4 Revision History</b> .....	<b>2</b>	9.1 Application Information .....	<b>9</b>
<b>5 Pin Configuration and Functions</b> .....	<b>3</b>	9.2 Typical Application .....	<b>9</b>
<b>6 Specifications</b> .....	<b>3</b>	<b>10 Power Supply Recommendations</b> .....	<b>11</b>
6.1 Absolute Maximum Ratings .....	<b>3</b>	<b>11 Layout</b> .....	<b>11</b>
6.2 ESD Ratings .....	<b>4</b>	11.1 Layout Guidelines .....	<b>11</b>
6.3 Recommended Operating Conditions .....	<b>4</b>	11.2 Layout Example .....	<b>11</b>
6.4 Thermal Information .....	<b>4</b>	<b>12 Device and Documentation Support</b> .....	<b>12</b>
6.5 Electrical Characteristics .....	<b>5</b>	12.1 Documentation Support .....	<b>12</b>
6.6 Switching Characteristics .....	<b>5</b>	12.2 Related Links .....	<b>12</b>
6.7 Operating Characteristics .....	<b>5</b>	12.3 Community Resources .....	<b>12</b>
6.8 Typical Characteristics .....	<b>6</b>	12.4 Trademarks .....	<b>12</b>
<b>7 Parameter Measurement Information</b> .....	<b>6</b>	12.5 Electrostatic Discharge Caution .....	<b>12</b>
<b>8 Detailed Description</b> .....	<b>7</b>	12.6 Glossary .....	<b>12</b>
8.1 Overview .....	<b>7</b>	<b>13 Mechanical, Packaging, and Orderable Information</b> .....	<b>12</b>
8.2 Functional Block Diagram .....	<b>7</b>		

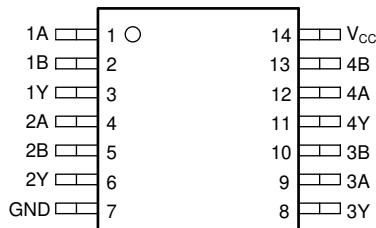
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision A (April 2008) to Revision B</b>	<b>Page</b>
• Updated to new data sheet standards .....	<b>1</b>
• Changed $R_{\theta JA}$ for PW package from 113 °C/W to 151.7 °C/W .....	<b>4</b>
• Changed $R_{\theta JA}$ for D package from 86 °C/W to 133.6 °C/W .....	<b>4</b>

## 5 Pin Configuration and Functions

**D or PW Package  
14-Pin SOIC or TSSOP  
Top View**



**Pin Functions**

PIN		I/O	DESCRIPTION
NAME	NO.		
1A	1	Input	Channel 1, Input A
1B	2	Input	Channel 1, Input B
1Y	3	Output	Channel 1, Output Y
2A	4	Input	Channel 2, Input A
2B	5	Input	Channel 2, Input B
2Y	6	Output	Channel 2, Output Y
GND	7	—	Ground
3Y	8	Output	Channel 3, Output Y
3A	9	Input	Channel 3, Input A
3B	10	Input	Channel 3, Input B
4Y	11	Output	Channel 4, Output Y
4A	12	Input	Channel 4, Input A
4B	13	Input	Channel 4, Input B
V <sub>CC</sub>	14	—	Positive Supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	−0.5	7	V
I <sub>IK</sub>	Input clamp current <sup>(2)</sup>		±20	mA
		V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>CC</sub>		
I <sub>OK</sub>	Output clamp current <sup>(2)</sup>		±20	mA
		V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub>		
I <sub>O</sub>	Continuous output current		±25	mA
		V <sub>O</sub> = 0 to V <sub>CC</sub>		
	Continuous current through V <sub>CC</sub> or GND		±50	mA
T <sub>J</sub>	Junction temperature <sup>(3)</sup>		150	°C
T <sub>stg</sub>	Storage temperature	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

(3) Guaranteed by design.

## 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 <sup>(1)</sup> HBM ESD Classification Level 2	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C6	±1000	

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2	5	6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5		V
		V <sub>CC</sub> = 4.5 V	3.15		
		V <sub>CC</sub> = 6 V	4.2		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V		0.5	V
		V <sub>CC</sub> = 4.5 V		1.35	
		V <sub>CC</sub> = 6 V		1.8	
V <sub>I</sub>	Input voltage	0		V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0		V <sub>CC</sub>	V
Δt/Δv	Input transition rise and fall rate	V <sub>CC</sub> = 2 V		1000	ns
		V <sub>CC</sub> = 4.5 V		500	
		V <sub>CC</sub> = 6 V		400	
T <sub>A</sub>	Operating free-air temperature	–40		125	°C

## 6.4 Thermal Information

THERMAL METRIC	SN74HCS00-Q1		UNIT	
	PW (TSSOP)	D (SOIC)		
	14 PINS	14 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	151.7	133.6	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	79.4	89.0	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	94.7	89.5	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	25.2	45.5	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	94.1	89.1	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

## 6.5 Electrical Characteristics

over operating free-air temperature range; typical values measured at  $T_A = 25^\circ\text{C}$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS		$V_{CC}$	Operating free-air temperature ( $T_A$ )						UNIT
					25°C			-40°C to 125°C			
					MIN	TYP	MAX	MIN	TYP	MAX	
$V_{OH}$	High-level output voltage	$V_I = V_{IH}$ or $V_{IL}$	$I_{OH} = -20\ \mu\text{A}$	2 V	1.9	1.998		1.9			V
				4.5 V	4.4	4.499		4.4			
				6 V	5.9	5.999		5.9			
			$I_{OH} = -4\ \text{mA}$	4.5 V	3.98	4.3		3.7			
				6 V	5.48	5.8		5.2			
$V_{OL}$	Low-level output voltage	$V_I = V_{IH}$ or $V_{IL}$	$I_{OL} = 20\ \mu\text{A}$	2 V		0.002	0.1		0.1	V	
				4.5 V		0.001	0.1		0.1		
				6 V		0.001	0.1		0.1		
			$I_{OL} = 4\ \text{mA}$	4.5 V		0.17	0.26		0.4		
				6 V		0.15	0.26		0.4		
$I_I$	Input leakage current	$V_I = V_{CC}$ or 0		6 V		$\pm 0.1$	$\pm 100$		$\pm 1000$	nA	
$I_{CC}$	Supply current	$V_I = V_{CC}$ or 0	$I_O = 0$	6 V				2		40	$\mu\text{A}$
$C_i$	Input capacitance			2 V to 6 V		3	10			10	pF

## 6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		FROM	TO	$V_{CC}$	Operating free-air temperature ( $T_A$ )						UNIT
					25°C			-40°C to 125°C			
					MIN	TYP	MAX	MIN	TYP	MAX	
$t_{pd}$	Propagation delay	A or B	Y	2 V		45	90			135	ns
				4.5 V		9	18		27		
				6 V		8	15		23		
$t_t$	Transition-time		Y	2 V		38	75			110	ns
				4.5 V		8	15		22		
				6 V		6	13		19		

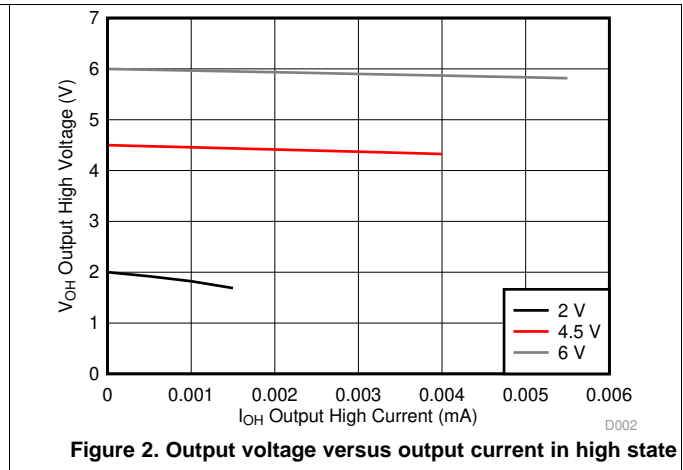
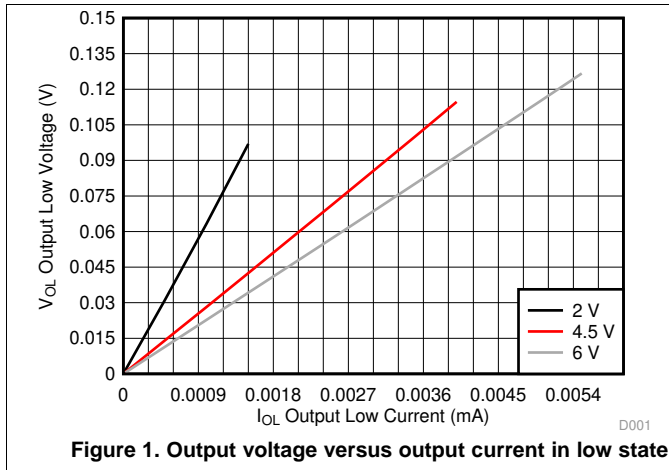
## 6.7 Operating Characteristics

over operating free-air temperature range; typical values measured at  $T_A = 25^\circ\text{C}$  (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{pd}$	Power dissipation capacitance per gate		20		pF

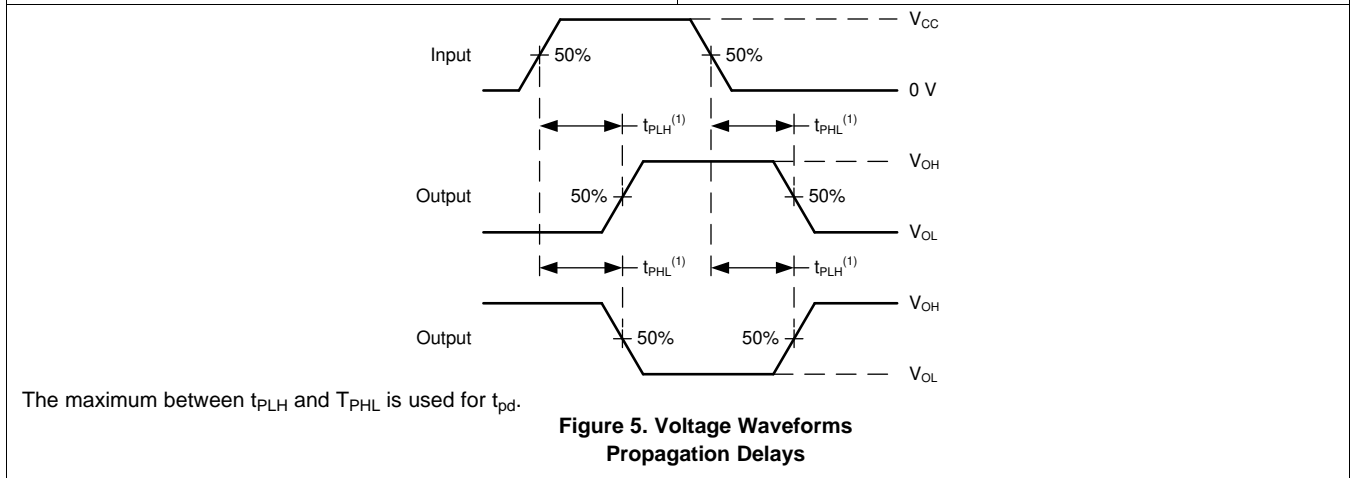
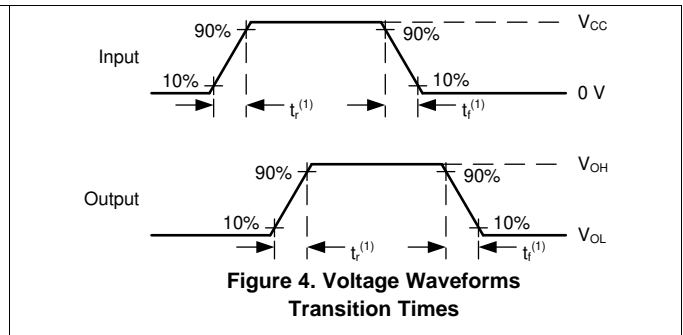
### 6.8 Typical Characteristics

T<sub>A</sub> = 25°C



### 7 Parameter Measurement Information

- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> < 6 ns.
- The outputs are measured one at a time, with one input transition per measurement.

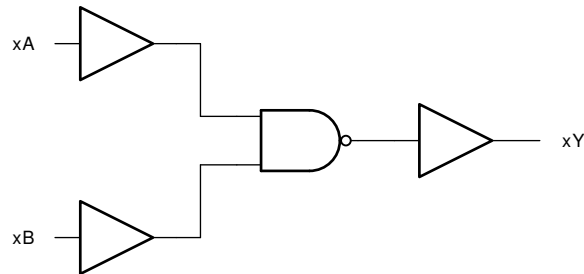


## 8 Detailed Description

### 8.1 Overview

This device contains four independent 2-input NAND gates. Each gate performs the Boolean function  $Y = \overline{A \bullet B}$  in positive logic.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 Balanced CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to over-current. The electrical and thermal limits defined in the [Absolute Maximum Ratings](#) must be followed at all times.

The SN74HC00-Q1 can drive a load with a total capacitance less than or equal to 50 pF connected to a high-impedance CMOS input while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed 70 pF. If larger capacitive loads are required, it is recommended to add a series resistor between the output and the capacitor to limit output current to the values given in the [Absolute Maximum Ratings](#).

#### 8.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor from the input to ground in parallel with the input capacitance given in the [Electrical Characteristics](#). The worst case resistance is calculated with the maximum input voltage, given in the [Absolute Maximum Ratings](#), and the maximum input leakage current, given in the [Electrical Characteristics](#), using ohm's law ( $R = V \div I$ ).

Signals applied to the inputs need to have fast edge rates, as defined by  $\Delta t/\Delta v$  in the [Recommended Operating Conditions](#) to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

**Feature Description (continued)**

**8.3.3 Clamp Diode Structure**

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in Figure 6.

**CAUTION**

Voltages beyond the values specified in the [Absolute Maximum Ratings](#) table can cause damage to the device. The recommended input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.



**Figure 6. Electrical Placement of Clamping Diodes for Each Input and Output**

**8.4 Device Functional Modes**

**Table 1. Function Table**

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H



## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

In this application, two 2-input NAND gates are used to create an active-low SR latch as shown in [Figure 7](#). The two additional gates can be used for a second SR latch, or the inputs can be grounded and both channels left unused.

The SN74HC00-Q1 is used to drive the tamper indicator LED and provide one bit of data to the system controller. When the tamper switch outputs LOW, the output Q becomes HIGH. This output remains HIGH until the system controller addresses the event and sends a LOW signal to the R input which returns the Q output back to LOW.

### 9.2 Typical Application

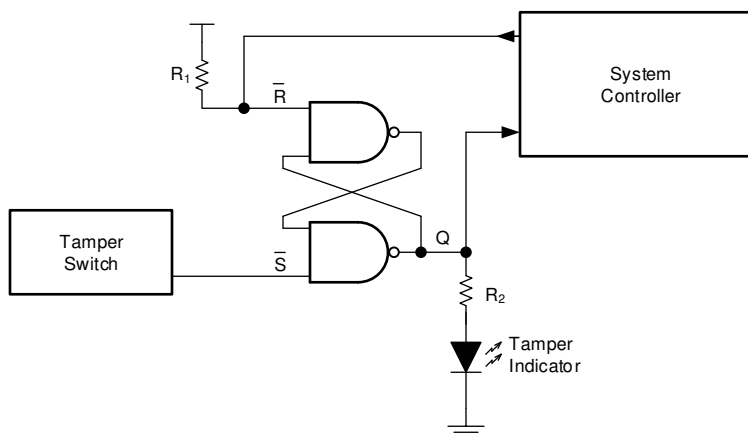


Figure 7. Typical application block diagram

#### 9.2.1 Design Requirements

- Avoid unstable state by not having LOW signals on both inputs

##### 9.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the [Recommended Operating Conditions](#). The supply voltage sets the device's electrical characteristics as described in the [Electrical Characteristics](#).

The supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74HC00-Q1 plus the maximum supply current,  $I_{CC}$ , listed in the [Electrical Characteristics](#). The logic device can only source or sink as much current as it is provided at the supply and ground pins, respectively. Be sure not to exceed the maximum total current through GND or  $V_{CC}$  listed in the [Absolute Maximum Ratings](#).

Total power consumption can be calculated using the information provided in [CMOS Power Consumption and  \$C\_{pd}\$  Calculation](#).

Thermal increase can be calculated using the information provided in [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#).

## Typical Application (continued)

### CAUTION

The maximum junction temperature,  $T_J(\text{max})$  listed in the [Absolute Maximum Ratings](#), is an *additional limitation* to prevent damage to the device. Do not violate any values listed in the [Absolute Maximum Ratings](#). These limits are provided to prevent damage to the device.

### 9.2.1.2 Input Considerations

Unused inputs must be terminated to either  $V_{CC}$  or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the SN74HC00-Q1, as specified in the [Electrical Characteristics](#), and the desired input transition rate. A 10-k $\Omega$  resistor value is often used due to these factors.

The SN74HC00-Q1 has standard CMOS inputs, so input signal edge rates cannot be slow. Slow input edge rates can cause oscillations and damaging shoot-through current. The recommended rates are defined in the [Recommended Operating Conditions](#).

Refer to the [Feature Description](#) for additional information regarding the inputs for this device.

### 9.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the  $V_{OH}$  specification in the [Electrical Characteristics](#). Similarly, the ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the  $V_{OL}$  specification in the [Electrical Characteristics](#).

Unused outputs can be left floating. Do not connect outputs directly to  $V_{CC}$  or ground.

Refer to [Feature Description](#) for additional information regarding the outputs for this device.

## 9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from  $V_{CC}$  to GND. The capacitor needs to be placed physically close to the device and electrically close to both the  $V_{CC}$  and GND pins. An example layout is shown in the [Layout](#).
2. Ensure the capacitive load at the output is  $\leq 70$  pF. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74HC00-Q1 to the receiving device.
3. Ensure the resistive load at the output is larger than  $(V_{CC} / I_O(\text{max})) \Omega$ . This will ensure that the maximum output current from the [Absolute Maximum Ratings](#) is not violated. Most CMOS inputs have a resistive load measured in megaohms; much larger than the minimum calculated above.
4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#)

## 9.2.3 Application Curves

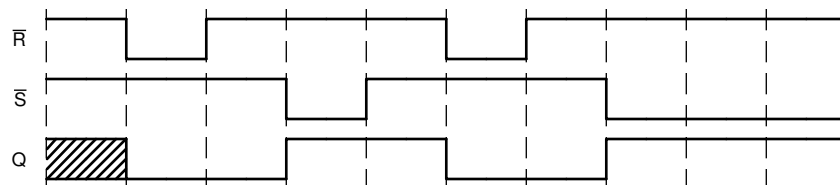


Figure 8. Application timing diagram

## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Recommended Operating Conditions](#). Each  $V_{CC}$  terminal should have a bypass capacitor to prevent power disturbance. A 0.1- $\mu\text{F}$  capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- $\mu\text{F}$  and 1- $\mu\text{F}$  capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in [Figure 9](#).

## 11 Layout

### 11.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

### 11.2 Layout Example

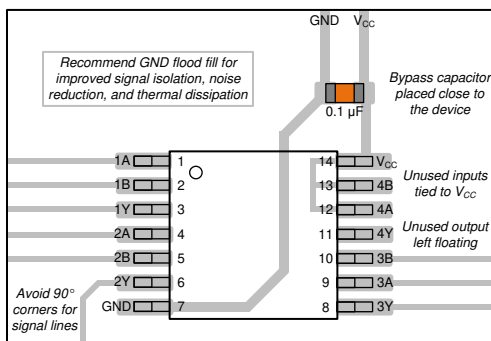


Figure 9. Example layout for the SN74HC00-Q1

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation see the following:

- [HCMOS Design Considerations](#)
- [CMOS Power Consumption and CPD Calculation](#)
- [Designing with Logic](#)

### 12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

### 12.3 Community Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 12.4 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HC00QDRG4Q1	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC00Q	<a href="#">Samples</a>
SN74HC00QDRQ1	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC00Q	<a href="#">Samples</a>
SN74HC00QPWRG4Q1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC00Q	<a href="#">Samples</a>
SN74HC00QPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC00Q	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74HC00-Q1 :**

- Catalog : [SN74HC00](#)
- Military : [SN54HC00](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC00QDRG4Q1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC00QDRQ1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC00QPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC00QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC00QDRG4Q1	SOIC	D	14	2500	356.0	356.0	35.0
SN74HC00QDRQ1	SOIC	D	14	2500	356.0	356.0	35.0
SN74HC00QPWRG4Q1	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74HC00QPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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