

## SN74HCS72-Q1 Automotive Qualified Schmitt-Trigger Input Dual D-Type Negative-Edge-Triggered Flip-Flops With Clear and Preset

### 1 Features

- AEC-Q100 Qualified for automotive applications:
  - Device temperature grade 1:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $T_A$
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C6
- Wide operating voltage range: 2 V to 6 V
- Schmitt-trigger inputs allow for slow or noisy input signals
- Low power consumption
  - Typical  $I_{CC}$  of 100 nA
  - Typical input leakage current of  $\pm 100$  nA
- $\pm 7.8$ -mA output drive at 5 V

### 2 Applications

- [Convert a momentary switch to a toggle switch](#)
- [Input slow edge-rate signals](#)
- [Operate in noisy environments](#)
- Enable CAN Controller Power with wake-up pattern

### 3 Description

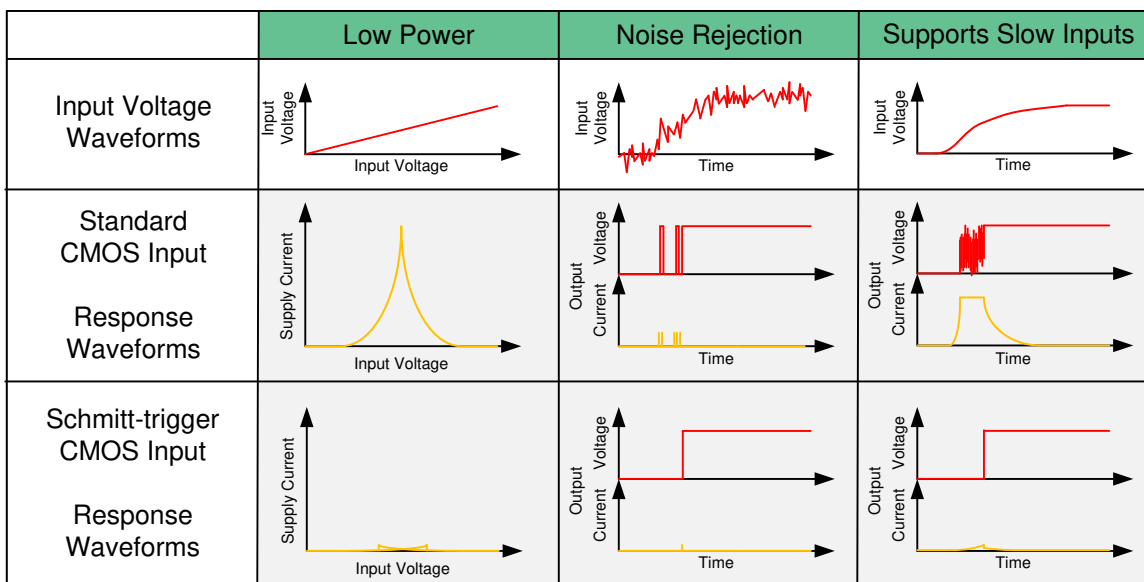
This device contains two independent D-type negative-edge-triggered flip-flops. All inputs include Schmitt-triggers, allowing for slow or noisy input signals. A low level at the preset ( $\overline{\text{PRE}}$ ) input sets the output high. A low level at the clear ( $\overline{\text{CLR}}$ ) input resets the output low. Preset and clear functions are asynchronous and not dependent on the levels of the other inputs. When  $\overline{\text{PRE}}$  and  $\overline{\text{CLR}}$  are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs ( $\text{Q}$ ,  $\overline{\text{Q}}$ ) on the negative-going edge of the clock ( $\overline{\text{CLK}}$ ) pulse. Following the hold-time interval, data at the data (D) input can be changed without affecting the levels at the outputs ( $\text{Q}$ ,  $\overline{\text{Q}}$ ).

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74HCS72QDRQ1	SOIC (14)	8.70 mm x 3.90 mm
SN74HCS72QPWRQ1	TSSOP (14)	5.00 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Benefits of Schmitt-trigger Inputs



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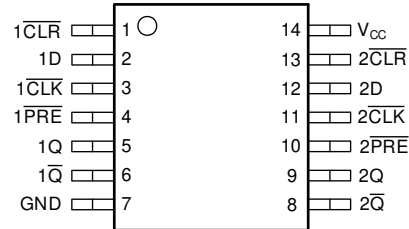
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## 4 Revision History

DATE	REVISION	NOTES
October 2019	*	Initial release.

## 5 Pin Configuration and Functions

**D and PW Package**  
**14-Pin SOIC and TSSOP**  
**Top View**



**Pin Functions**

PIN		TYPE	DESCRIPTION
NAME	NO.		
$1\overline{\text{CLR}}$	1	Input	Clear for channel 1, active low
1D	2	Input	Data for channel 1
$1\overline{\text{CLK}}$	3	Input	Clock for channel 1, falling edge triggered
$1\overline{\text{PRE}}$	4	Input	Preset for channel 1, active low
1Q	5	Output	Output for channel 1
$1\overline{\text{Q}}$	6	Output	Inverted output for channel 1
GND	7	—	Ground
$2\overline{\text{Q}}$	8	Output	Inverted output for channel 2
2Q	9	Output	Output for channel 2
$2\overline{\text{PRE}}$	10	Input	Preset for channel 2, active low
$2\overline{\text{CLK}}$	11	Input	Clock for channel 2, falling edge triggered
2D	12	Input	Data for channel 2
$2\overline{\text{CLR}}$	13	Input	Clear for channel 2, active low
V <sub>CC</sub>	14	—	Positive supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	-0.5	7	V
I <sub>IK</sub>	Input clamp current <sup>(2)</sup>	V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V		±20 mA
I <sub>OK</sub>	Output clamp current <sup>(2)</sup>	V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V		±20 mA
I <sub>O</sub>	Continuous output current	V <sub>O</sub> = 0 to V <sub>CC</sub>		±25 mA
	Continuous current through V <sub>CC</sub> or GND			±50 mA
T <sub>j</sub>	Junction temperature <sup>(3)</sup>			150 °C
T <sub>stg</sub>	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) Guaranteed by design

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 <sup>(1)</sup> HBM ESD Classification Level 2	±4000
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±1000

- (1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2	5	6	V
V <sub>I</sub>	Input voltage	0		V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0		V <sub>CC</sub>	V
Δt/Δv	Input transition rise and fall rate			Unlimited	ns/V
T <sub>A</sub>	Ambient temperature	-40		125	°C

### 6.4 Thermal Information

THERMAL METRIC	SN74HCS72-Q1		UNIT	
	D (SOIC)	PW (TSSOP)		
	14 PINS	14 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	133.6	151.7	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	89	79.4	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	89.5	94.7	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	45.5	25.2	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	89.1	94.1	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

## 6.5 Electrical Characteristics

over operating free-air temperature range; typical values measured at  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		$V_{CC}$	MIN	TYP	MAX	UNIT
$V_{T+}$	Positive switching threshold			2 V	0.7		1.5	V
				4.5 V	1.7		3.15	
				6 V	2.1		4.2	
$V_{T-}$	Negative switching threshold			2 V	0.3		1.0	V
				4.5 V	0.9		2.2	
				6 V	1.2		3.0	
$\Delta V_T$	Hysteresis ( $V_{T+} - V_{T-}$ ) <sup>(1)</sup>			2 V	0.2		1.0	V
				4.5 V	0.4		1.4	
				6 V	0.6		1.6	
$V_{OH}$	High-level output voltage	$V_I = V_{IH}$ or $V_{IL}$	$I_{OH} = -20 \mu\text{A}$	2 V to 6 V	$V_{CC} - 0.1$	$V_{CC} - 0.002$		V
			$I_{OH} = -6 \text{ mA}$	4.5 V	4	4.3		
			$I_{OH} = -7.8 \text{ mA}$	6 V	5.4	5.75		
$V_{OL}$	Low-level output voltage	$V_I = V_{IH}$ or $V_{IL}$	$I_{OL} = 20 \mu\text{A}$	2 V to 6 V		0.002	0.1	V
			$I_{OL} = 6 \text{ mA}$	4.5 V		0.18	0.30	
			$I_{OL} = 7.8 \text{ mA}$	6 V		0.22	0.33	
$I_I$	Input leakage current	$V_I = V_{CC}$ or 0		6 V		$\pm 100$	$\pm 1000$	nA
$I_{CC}$	Supply current	$V_I = V_{CC}$ or 0, $I_O = 0$		6 V		0.1	2	$\mu\text{A}$
$C_i$	Input capacitance			2 V to 6 V			5	pF
$C_{pd}$	Power dissipation capacitance per gate	No load		2 V to 6 V		10		pF

(1) Guaranteed by design.

## 6.6 Switching Characteristics

 $C_L = 50 \text{ pF}$ ; over operating free-air temperature range; typical values measured at  $T_A = 25^\circ\text{C}$  (unless otherwise noted). See [Parameter Measurement Information](#)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	MIN	TYP	MAX	UNIT
$f_{max}$	Max switching frequency			2 V	20	31		MHz
				4.5 V	64	95		
				6 V	74	105		
$t_{pd}$	Propagation delay	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{Q}$	2 V		19	42	ns
				4.5 V		8	19	
				6 V		7	15	
		$\overline{\text{CLK}}$	Q or $\overline{Q}$	2 V		19	42	ns
				4.5 V		8	19	
				6 V		7	15	
$t_t$	Transition-time <sup>(1)</sup>			2 V		9	16	ns
				4.5 V		5	9	
				6 V		4	8	

(1)  $t_t = t_r$  or  $t_f$ , whichever is larger

## 6.7 Timing Characteristics

$C_L = 50$  pF; over operating free-air temperature range; typical values measured at  $T_A = 25^\circ\text{C}$  (unless otherwise noted). See [Parameter Measurement Information](#).

PARAMETER			$V_{CC}$	MIN	TYP	MAX	UNIT
$f_{\text{clock}}$	Clock frequency		2 V			20	MHz
			4.5 V			64	
			6 V			74	
$t_w$	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	2 V	8	7		ns
			4.5 V	7	5		
			6 V	7	5		
	$\overline{\text{CLK}}$ high or low	2 V	10	5		ns	
		4.5 V	9	3			
		6 V	8	2			
$t_{\text{su}}$	Setup time before $\overline{\text{CLK}}$ low	Data	2 V	16	11		ns
			4.5 V	6	1		
			6 V	3	1		
	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive	2 V	7			ns	
		4.5 V	0				
		6 V	0				
$t_h$	Hold time	Data after CLK ↓	2 V	5			ns
			4.5 V	3			
			6 V	2			

### 6.8 Typical Characteristics

T<sub>A</sub> = 25°C

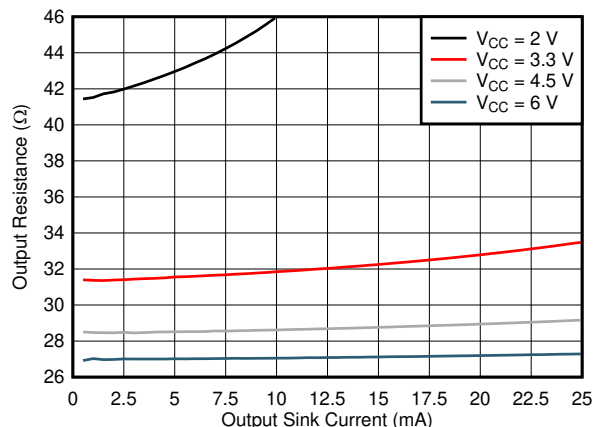


Figure 1. Output driver resistance in LOW state.

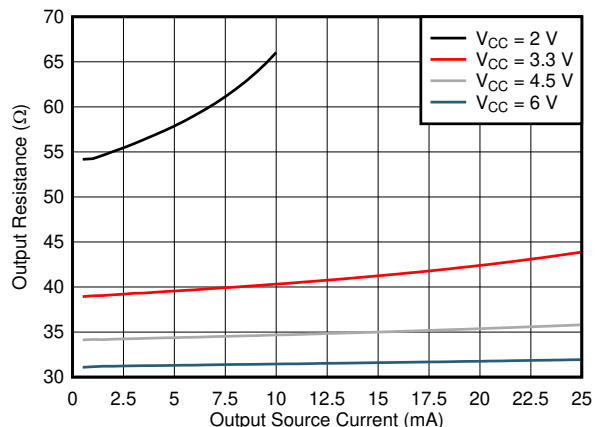


Figure 2. Output driver resistance in HIGH state.

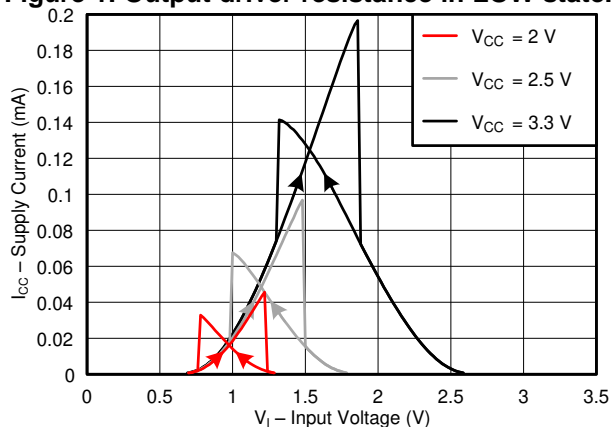


Figure 3. Supply current across input voltage, 2-, 2.5-, and 3.3-V supply

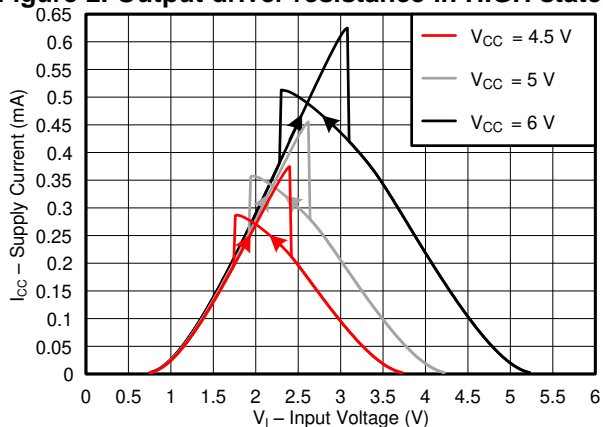


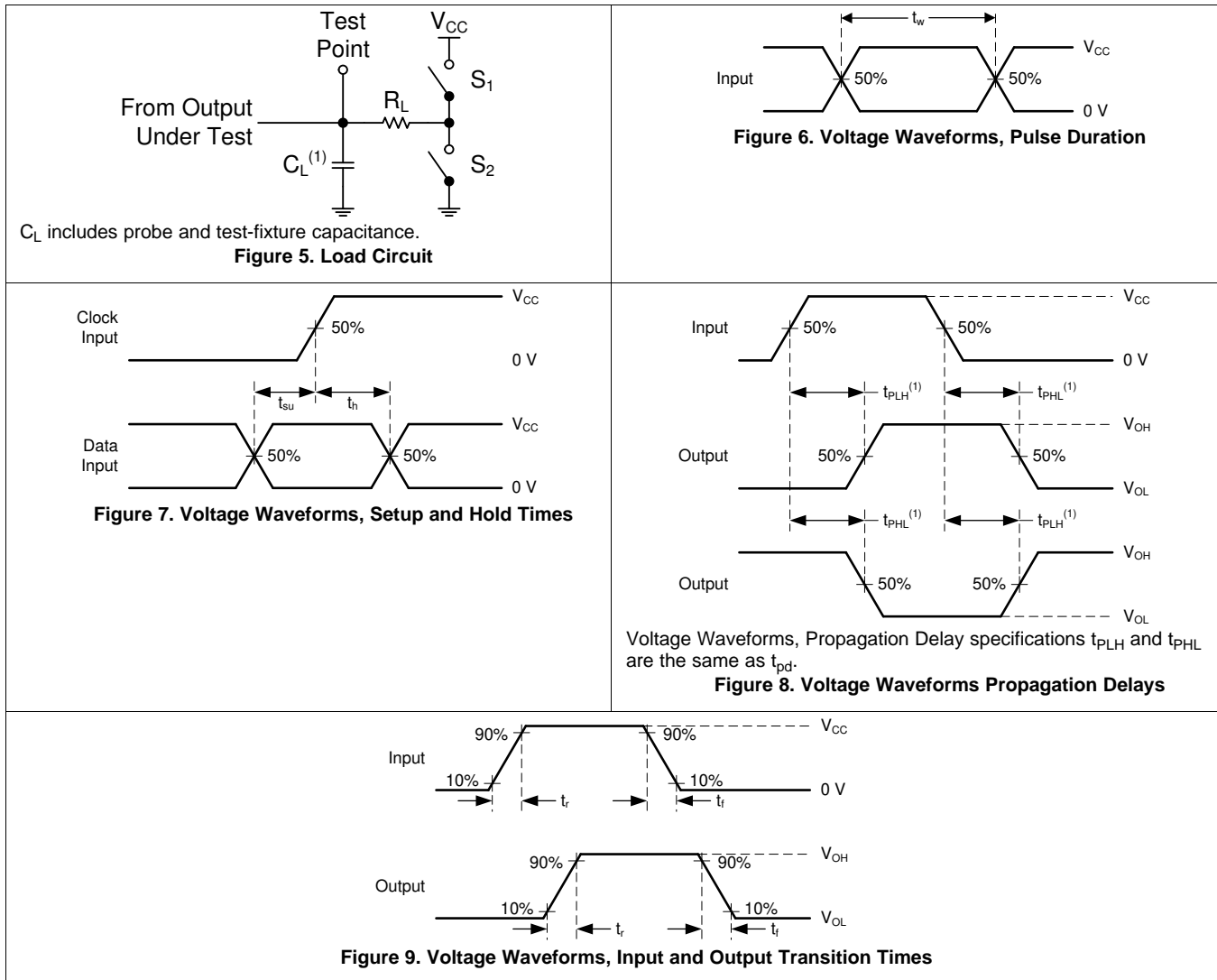
Figure 4. Supply current across input voltage, 4.5-, 5-, and 6-V supply

## 7 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_f < 2.5$  ns.

For clock inputs,  $f_{max}$  is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.





## 8 Detailed Description

### 8.1 Overview

Figure 10 describes the SN74HCS72-Q1. As the SN74HCS72-Q1 is a dual D-Type negative-edge-triggered flip-flop with clear and preset, the diagram below describes one of the two device flip-flops.

### 8.2 Functional Block Diagram

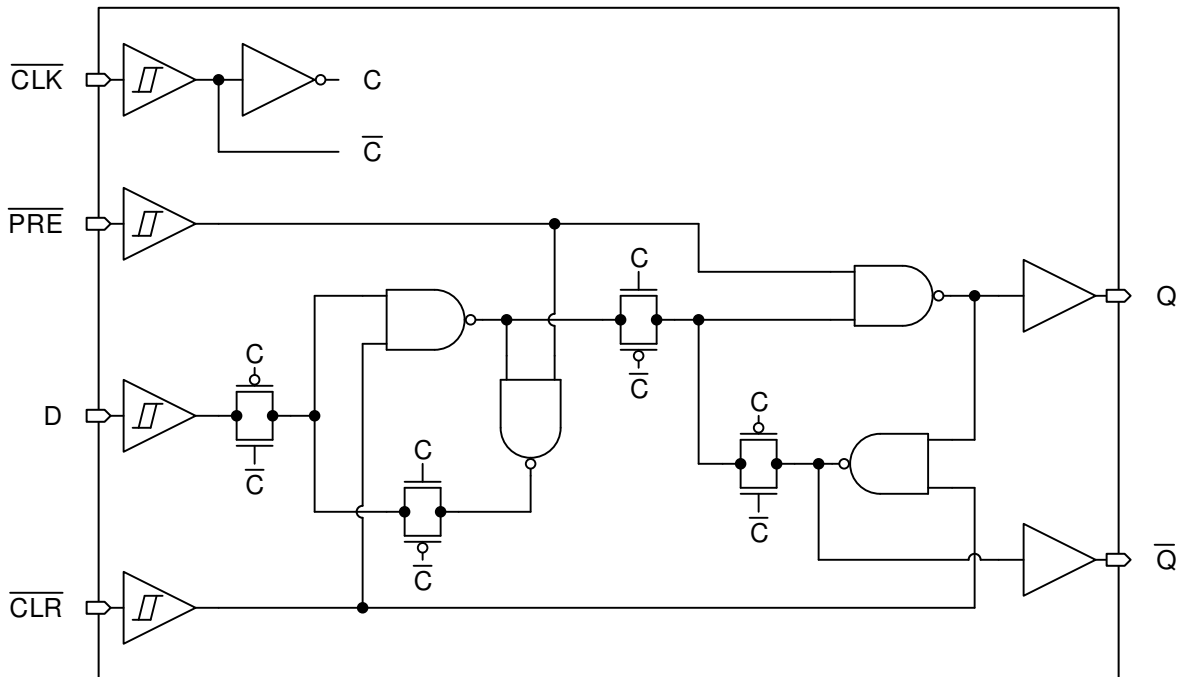


Figure 10. Logic Diagram (Positive Logic) for one channel of SN74HCS72-Q1

### 8.3 Feature Description

#### 8.3.1 Balanced CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to over-current. The electrical and thermal limits defined in the [Absolute Maximum Ratings](#) must be followed at all times.

#### 8.3.2 CMOS Schmitt-Trigger Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the [Electrical Characteristics](#). The worst case resistance is calculated with the maximum input voltage, given in the [Absolute Maximum Ratings](#), and the maximum input leakage current, given in the [Electrical Characteristics](#), using ohm's law ( $R = V \div I$ ).

The Schmitt-trigger input architecture provides hysteresis as defined by  $\Delta V_T$  in the [Electrical Characteristics](#), which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs slowly will also increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see [Understanding Schmitt Triggers](#).

## Feature Description (continued)

### 8.3.3 Positive and Negative Clamping Diodes

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in [Figure 11](#).

**CAUTION**

Voltages beyond the values specified in the [Absolute Maximum Ratings](#) table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

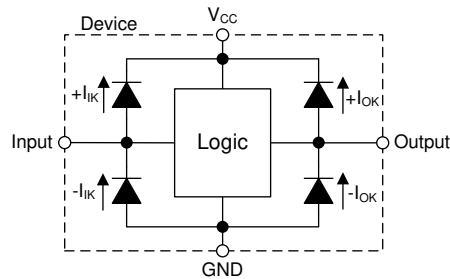


Figure 11. Electrical Placement of Clamping Diodes for Each Input and Output

## 8.4 Device Functional Modes

[Table 1](#) lists the functional modes of the SN74HCS72-Q1.

Table 1. Function Table

INPUTS				OUTPUTS	
$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	$\overline{\text{CLK}}$	D	Q	$\overline{\text{Q}}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H <sup>(1)</sup>	H <sup>(1)</sup>
H	H	↓	H	H	L
H	H	↓	L	L	H
H	H	L	X	Q <sub>0</sub>	$\overline{\text{Q}}_0$
H	H	H	X	Q <sub>0</sub>	$\overline{\text{Q}}_0$

(1) This configuration is nonstable; that is, it does not persist when  $\overline{\text{PRE}}$  or  $\overline{\text{CLR}}$  returns to its inactive (high) level.

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The SN74HCS72-Q1 is an ideal device for taking a CAN wake-up request and converting it to a power supply enable due to its low power consumption and noise rejecting inputs, which eliminate false triggers. CAN communication can occur when the vehicle ignition is off. Therefore, many circuits are designed to work in a standby or low power mode. Because a CAN wake-up request causes the RX pin to pulse LOW, the SN74HCS72-Q1 will trigger off the falling edge enabling the power for the CAN controller. Then the CAN controller powers on for the incoming communication. When communications are finished, the controller sends a reset pulse to the SN74HCS72-Q1 and CAN transceiver putting the circuit back into a standby mode.

### 9.2 Typical Application

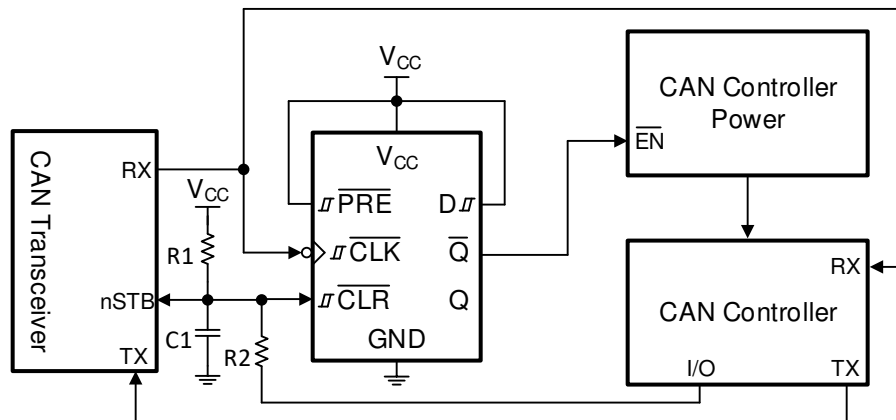


Figure 12. Power Enable Using CAN Wake-up Request

#### 9.2.1 Design Requirements

The SN74HCS72-Q1 device allows flexibility by having complementary outputs for active-high or active-low enables. The supply should be selected such that the device is always powered along with the CAN transceiver. The same supply for both devices is recommended.

With the SN74HCS72-Q1, a power on reset circuit only requires a resistor (R) and capacitor (C) to create a delay. The R and C values create a delay that is approximately  $2.2 \times RC$ . In this application, it is desired to have the output ( $\bar{Q}$ ) in the HIGH state at startup, so R1 and C1 are connected directly to the  $\bar{CLR}$  pin, as shown in Figure 12. A second resistor is needed to limit the current into the CAN controller when it sets the circuit back into standby mode. It is required for the R1 resistor to be at least ten times larger than R2 to avoid a divider circuit ( $R2 \leq 10R1$ ).

The D input can be tied either to  $V_{CC}$  or ground depending on the desired implementation. In this example, it is tied to  $V_{CC}$  to obtain a HIGH signal from  $\bar{Q}$  when a wake-up request occurs.

## Typical Application (continued)

### 9.2.1.1 Output Considerations

In general, the load needs to be considered in the design to determine if the device will have the capability to drive it. For this application, we assume that the flip-flop output is transmitting over a relatively short trace (under 10 cm) to a CMOS input.

Primary load factors to consider:

- Load Capacitance: approximately 15 pF
  - See the [Switching Characteristics](#) section for the capacitive loads tested with this device.
  - Increasing capacitance will proportionally increase output transition times.
  - Decreasing capacitance will proportionally decrease output transition times, and can produce ringing due to very fast transition rates. A 25-Ω resistor can be added in series with the output if ringing needs to be dampened.
- Load Current: expected maximum of 10 μA
  - Leakage current into connected devices.
  - Parasitic current from other components.
  - Resistive load current.
- Output Voltage: see [Electrical Characteristics](#) for output voltage ratings at a given current.
  - Output HIGH ( $V_{OH}$ ) and output LOW ( $V_{OL}$ ) voltage levels affect the input voltage,  $V_{IH}$  and  $V_{IL}$ , respectively, to subsequent devices.

### 9.2.1.2 Input Considerations

The SN74HCS72-Q1 has Schmitt-trigger inputs. Schmitt-trigger inputs have no limitation on transition rate, however the input voltage must be larger than  $V_{T+(max)}$  to be guaranteed to be read as a logic high, and below  $V_{T-(min)}$  to be guaranteed to be read as a logic low, as defined in the [Electrical Characteristics](#). Do not exceed the values specified in the [Absolute Maximum Ratings](#) or the device could be damaged.

### 9.2.1.3 Timing Considerations

The SN74HCS72-Q1 is a clocked device. As such, it requires special timing considerations to ensure normal operation.

Primary timing factors to consider:

- Maximum clock frequency: the maximum operating clock frequency defined in [Timing Characteristics](#) is the maximum frequency at which the device is guaranteed to function. This value refers specifically to the triggering waveform, measuring from one trigger level to the next.
- Pulse duration: ensure that the triggering event duration is larger than the minimum pulse duration, as defined in the [Timing Characteristics](#).
- Setup time: ensure that the data has changed at least one setup time prior to the triggering event, as defined in the [Timing Characteristics](#).
- Hold time: ensure that the data remains in the desired state at least one hold time after the triggering event, as defined in the [Timing Characteristics](#).

## 9.2.2 Detailed Design Procedure

### 1. Recommended Input Conditions:

- Input signals to Schmitt-trigger inputs, like those found on the HCS family of devices, can support unlimited edge rates.
- Input thresholds are listed in the [Electrical Characteristics](#).
- Inputs include positive clamp diodes. Input voltages can exceed the device's supply so long as the clamp current ratings are observed from the [Absolute Maximum Ratings](#). Do not exceed the absolute maximum voltage rating of the device or it could be damaged.

### 2. Recommended Output Conditions:

- Load currents should not exceed the value listed in the [Absolute Maximum Ratings](#).
- Series resistors on the output may be used if the user desires to slow the output edge signal or limit the

## Typical Application (continued)

output current.

### 9.2.3 Application Curve

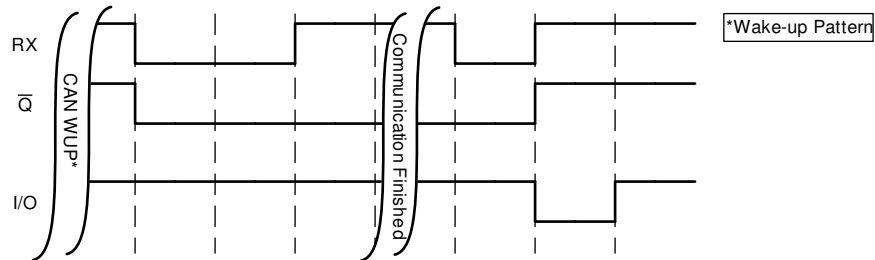


Figure 13. Application timing diagram

## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Absolute Maximum Ratings](#) table. Each  $V_{CC}$  terminal should have a bypass capacitor to prevent power disturbance. For this device, a 0.1- $\mu$ F capacitor is recommended. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- $\mu$ F and 1- $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminals as possible for best results.

## 11 Layout

### 11.1 Layout Guidelines

In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4 channels are used. Such input pins should not be left completely unconnected because the unknown voltages result in undefined operational states.

Specified in [Figure 14](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is recommended to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it disables the output section of the part when asserted. This pin keeps the input section of the I/Os from being disabled and floated.

### 11.2 Layout Example

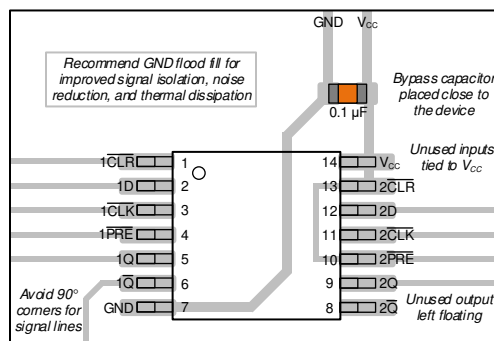


Figure 14. Layout Example

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [Implications of Slow or Floating CMOS Inputs](#) application report
- Texas Instruments, [Reduce Noise and Save Power with the New HCS Logic Family](#) application report
- Texas Instruments, [Understanding Schmitt Triggers](#) application report

### 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.3 Community Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 12.4 Trademarks

E2E is a trademark of Texas Instruments.

### 12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HCS72QDRQ1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS72Q1	<a href="#">Samples</a>
SN74HCS72QPWRQ1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS72Q	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCS72QDRQ1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HCS72QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCS72QDRQ1	SOIC	D	14	2500	367.0	367.0	38.0
SN74HCS72QPWRQ1	TSSOP	PW	14	2000	853.0	449.0	35.0

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211283-3/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/G 08/15

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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