

# SN54166, SN54LS166A, SN74166, SN74LS166A PARALLEL-LOAD 8-BIT SHIFT REGISTERS

OCTOBER 1976 — REVISED MARCH 1988

- Synchronous Load
- Direct Overriding Clear
- Parallel to Serial Conversion

TYPE	TYPICAL CLOCK FREQUENCY	MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'166	35 MHz		360 mW
'LS166A	35 MHz		100 mW

## description

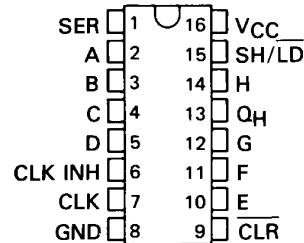
The '166 and 'LS166A 8-bit shift registers are compatible with most other TTL logic families. All '166 and 'LS166A inputs are buffered to lower the drive requirements to one Series 54/74 or Series 54LS/74LS standard load, respectively. Input clamping diodes minimize switching transients and simplify system design.

These parallel-in or serial-in, serial-out shift registers have a complexity of 77 equivalent gates on a monolithic chip. They feature gated clock inputs and an overriding clear input. The parallel-in or serial-in modes are established by the shift/load input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input positive NOR gate permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This, of course, allows the system clock to be free-running and the register can be stopped on command with the other clock input. The clock inhibit input should be changed to the high level only while the clock input is high. A buffered, direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

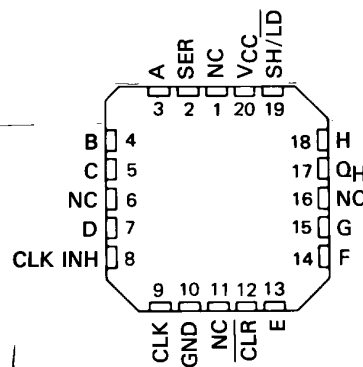
FUNCTION TABLE

CLEAR	INPUTS					INTERNAL OUTPUTS Q <sub>A</sub> Q <sub>B</sub>	OUTPUT Q <sub>H</sub>
	SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A...H		
L	X	X	X	X	X	L L	L
H	X	L	L	X	X	Q <sub>A0</sub> Q <sub>B0</sub>	Q <sub>H0</sub>
H	L	L	↑	X	a...h	a b	h
H	H	L	↑	H	X	H Q <sub>An</sub>	Q <sub>Gn</sub>
H	H	L	↑	L	X	L Q <sub>An</sub>	Q <sub>Gn</sub>
H	X	H	↑	X	X	Q <sub>A0</sub> Q <sub>B0</sub>	Q <sub>H0</sub>

SN54166, SN54LS166A . . . J OR W PACKAGE  
SN74166 . . . N PACKAGE  
SN74LS166A . . . D OR N PACKAGE  
(TOP VIEW)

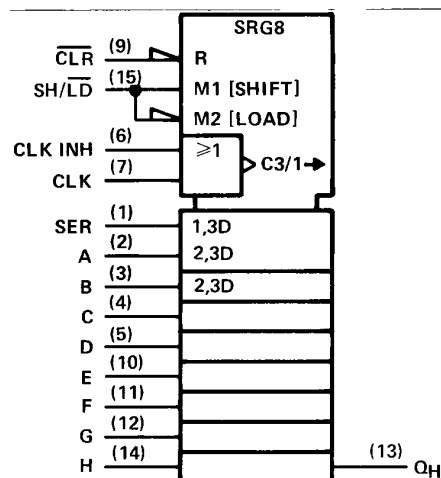


SN54LS166A . . . FK PACKAGE  
(TOP VIEW)



NC - No internal connection

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for D, J, N, and W packages.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS  
INSTRUMENTS

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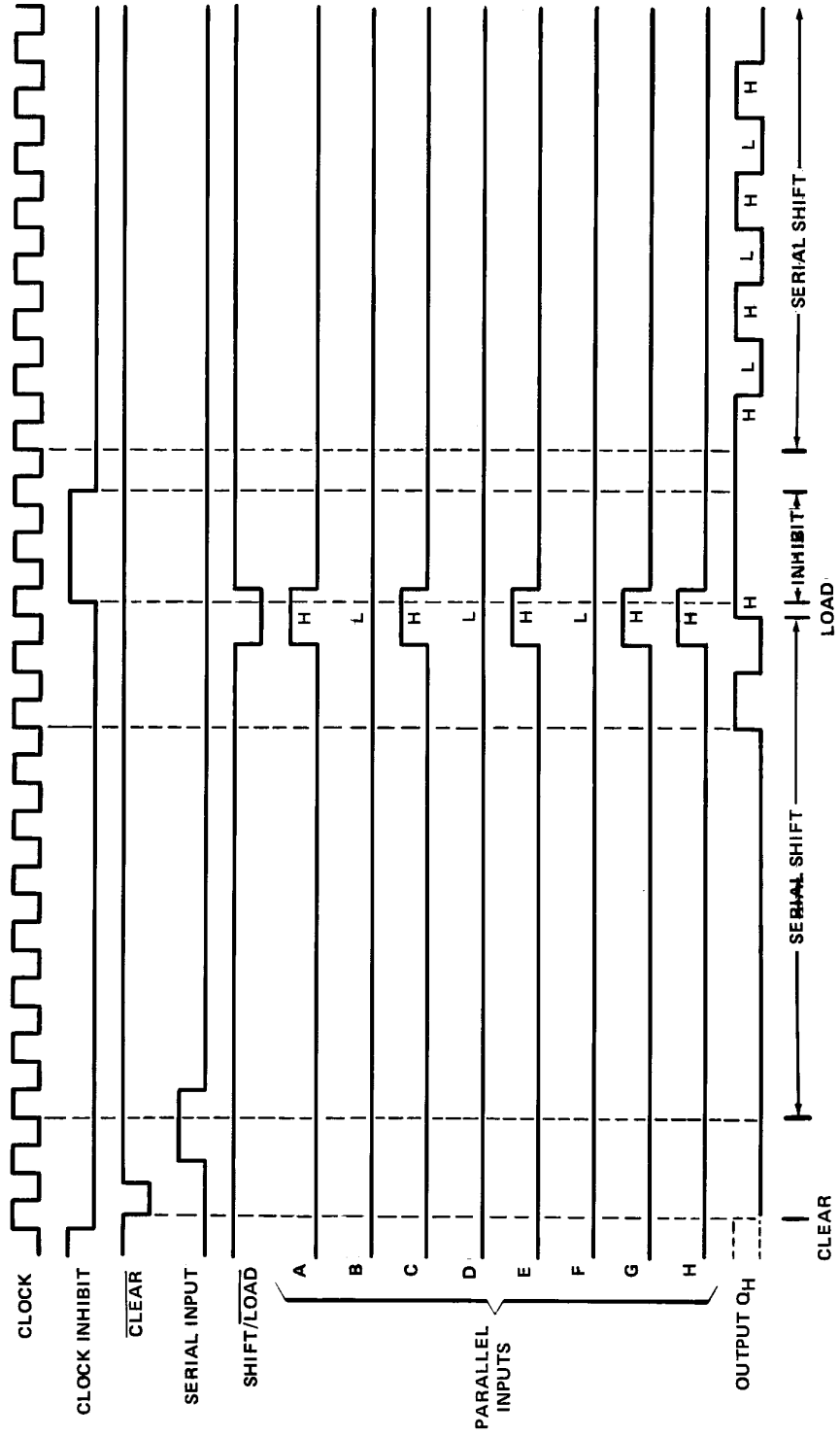
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TTL Devices

**SN54166, SN54LS166A, SN74166, SN74LS166A  
PARALLEL-LOAD 8-BIT SHIFT REGISTERS**

typical clear, shift, load, inhibit, and shift sequences



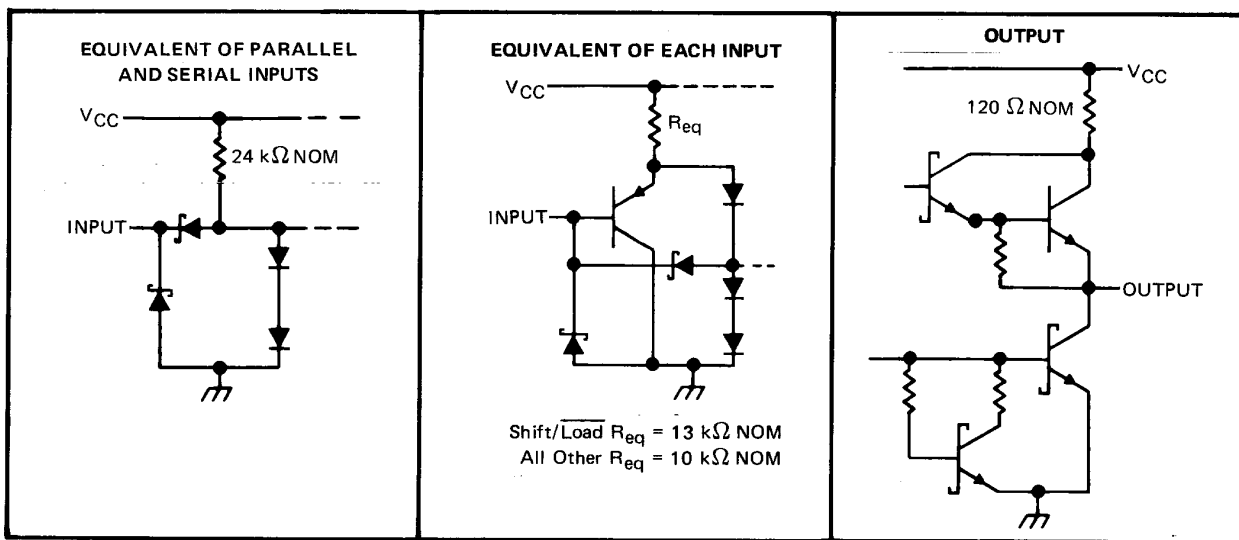
SN54166, SN54LS166A, SN74166, SN74LS166A  
PARALLEL-LOAD 8-BIT SHIFT REGISTERS

schematics of inputs and outputs

'166



'LS166A

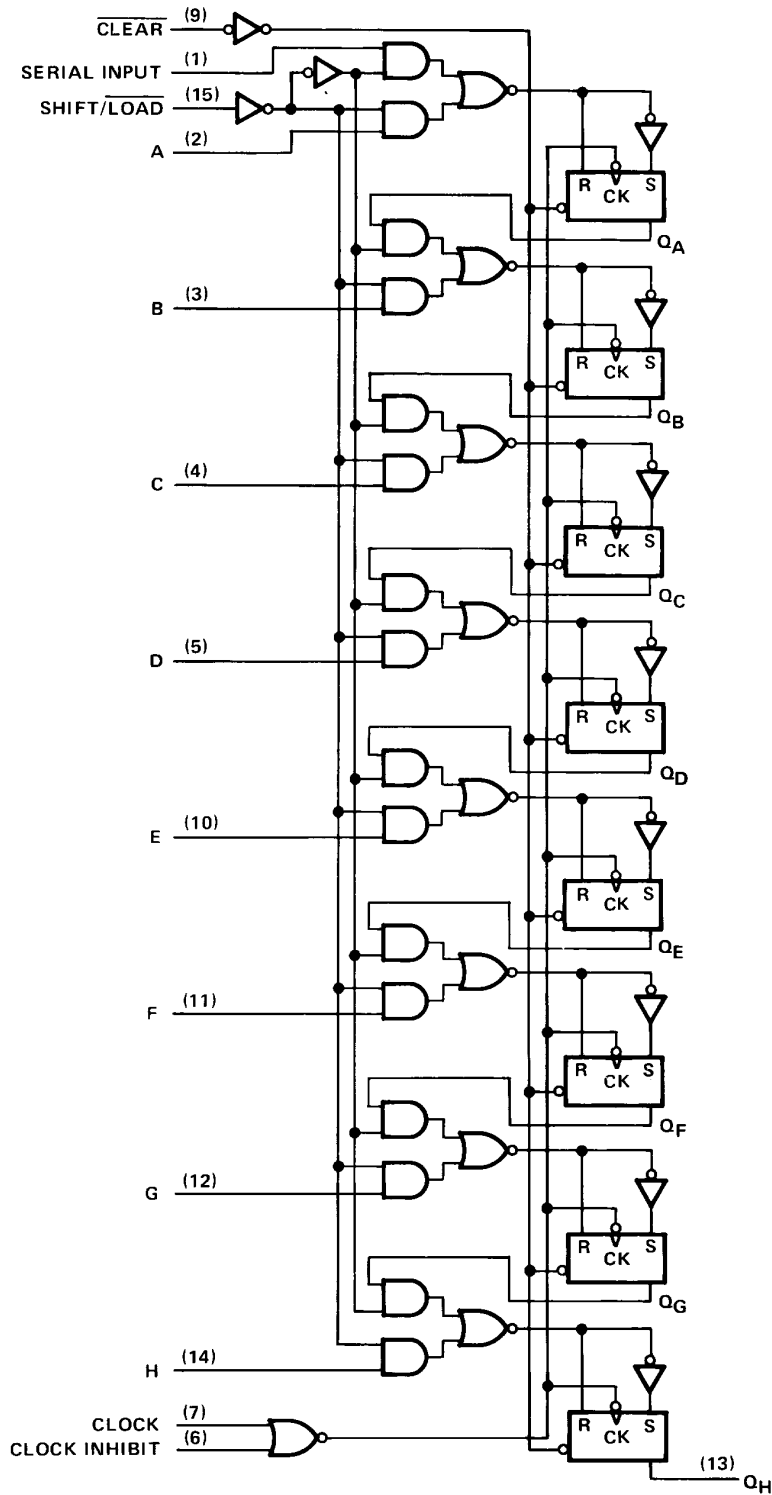


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TTL Devices

**SN54166, SN54LS166A, SN74166, SN74LS166A**  
**PARALLEL-LOAD 8-BIT SHIFT REGISTERS**

logic diagram (positive logic)



Pin numbers shown are for D, J, N, and W packages.

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TTL Devices

# SN54166, SN74166 PARALLEL-LOAD 8-BIT SHIFT REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54166 (see Note 2)	-55°C to 125°C
SN74166	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

	SN54166			SN74166			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$			-800			-800	$\mu$ A
Low-level output current, $I_{OL}$			16			16	mA
Clock frequency, $f_{clock}$	0	25		0	25		MHz
Width of clock or clear pulse, $t_W$ (see Figure 1)	20			20			ns
Mode-control setup time, $t_{SU}$	30			30			ns
Data setup time, $t_{SU}$ (see Figure 1)	20			20			ns
Hold time at any input, $t_H$ (see Figure 1)	0			0			ns
Operating free-air temperature, $T_A$ (see Note 2)	-55	125		0	70		°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>†</sup>	SN54166			SN74166			UNIT
		MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX	
$V_{IH}$ High-level input voltage		2			2			V
$V_{IL}$ Low-level input voltage				0.8			0.8	V
$V_{IK}$ Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5			-1.5	V
$V_{OH}$ High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu\text{A}$	2.4	3.4		2.4	3.4		V
$V_{OL}$ Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$	0.2	0.4		0.2	0.4		V
$I_I$ Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
$I_{IH}$ High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40			40	$\mu$ A
$I_{IL}$ Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6			-1.6	mA
$I_{OS}$ Short-circuit output current <sup>§</sup>	$V_{CC} = \text{MAX}$	-20	-57		-18	-57		mA
$I_{CC}$ Supply current	$V_{CC} = \text{MAX}$ , See Note 3	90	127		90	127		mA

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup>All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

<sup>§</sup>Not more than one output should be shorted at a time.

NOTES: 1. Voltage values are with respect to network ground terminal.

2. An SN54166 in the W package operating at free-air temperatures above 113°C requires a heat-sink that provides a thermal resistance from case to free air,  $R_{\theta CA}$ , of not more than 48°C/W.

3. With all outputs open, 4.5 V applied to the serial input, all other inputs except the clock grounded,  $I_{CC}$  is measured after a momentary ground, then 4.5 V, is applied to the clock.

switching characteristics,  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{max}$ Maximum clock frequency		25	35		MHz
$t_{PHL}$ Propagation delay time, high-to-low-level output from clear			23	35	ns
$t_{PHL}$ Propagation delay time, high-to-low-level output from clock	$C_L = 15 \text{ pF}, R_L = 400 \Omega,$ See Figure 1		20	30	ns
$t_{PLH}$ Propagation delay time, low-to-high-level output from clock			17	26	ns

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TTL Devices

# SN54LS166A, SN74LS166A PARALLEL-LOAD 8-BIT SHIFT REGISTERS

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS166A	-55°C to 125°C
SN74LS166A	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

## recommended operating conditions

		SN54LS166A			SN74LS166A			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.7			0.8	V
$I_{OH}$	High-level output current			-0.4			-0.4	mA
$I_{OL}$	Low-level output current			4			8	mA
$f_{clock}$	Clock frequency	0		25	0		25	MHz
$t_w$	Width of clear pulse (See Figure 1)	20			20			ns
$t_w$	Width of clock pulse (See Figure 1)	25			25			
$t_{su}$	Mode-control setup time	30			30			ns
$t_{su}$	Data setup time (See Figure 1)	20			20			ns
$t_h$	Hold time at any input (See Figure 1 and Note 4)	0			0			ns
$T_A$	Operating free air temperature	-55		125	0		70	°C

NOTE 4: The hold time limit of 0 ns applies only if the rise time is less than or equal to 10 ns.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS166A			SN74LS166A			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
$V_{IK}$	$V_{CC} = \text{MIN}$ , $I_I = -18 \text{ mA}$			-1.5			-1.5	V
$V_{OH}$	$V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ , $V_{IL} = \text{MAX}$ , $I_{OH} = -0.4 \text{ mA}$	2.5	3.4		2.7	3.4		V
$V_{OL}$	$V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ , $V_{IL} = \text{MAX}$	$I_{OL} = 4 \text{ mA}$		0.25	0.4	0.25	0.4	V
		$I_{OL} = 8 \text{ mA}$				0.35	0.5	
$I_I$	$V_{CC} = \text{MAX}$ , $V_I = 7 \text{ V}$			0.1			0.1	mA
$I_{IH}$	$V_{CC} = \text{MAX}$ , $V_I = 2.7 \text{ V}$			20			20	µA
$I_{IL}$	$V_{CC} = \text{MAX}$ , $V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
$I_{OS} §$	$V_{CC} = \text{MAX}$	-20		-100	-20		-100	mA
$I_{CC}$	$V_{CC} = \text{MAX}$ , See Note 5		20	32		20	32	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

§Not more than one output should be shorted at a time, and duration for short-circuit should not exceed one second.

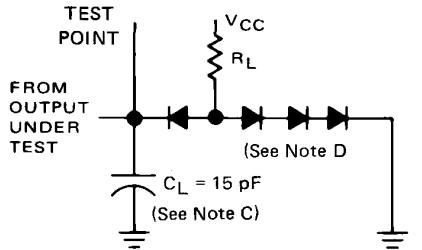
NOTE 5: With all outputs open, 4.5 V applied to the serial input and all other inputs except the clock grounded,  $I_{CC}$  is measured after a momentary ground, than 4.5 V, is applied to clock.

## switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$f_{max}$ Maximum clock frequency	$C_L = 15 \text{ pF}$ , $R_L = 2 \text{ k}\Omega$ , See Figure 1	25	35		MHz	
$t_{PHL}$ Propagation delay time, high-to-low-level output from clear			19	30	ns	
$t_{PHL}$ Propagation delay time, high-to-low-level output from clock			7	14	25	ns
$t_{PLH}$ Propagation delay time, low-to-high-level output from clock			5	11	20	ns

# SN54166, SN54LS166A, SN74166, SN74LS166A PARALLEL-LOAD 8-BIT SHIFT REGISTERS

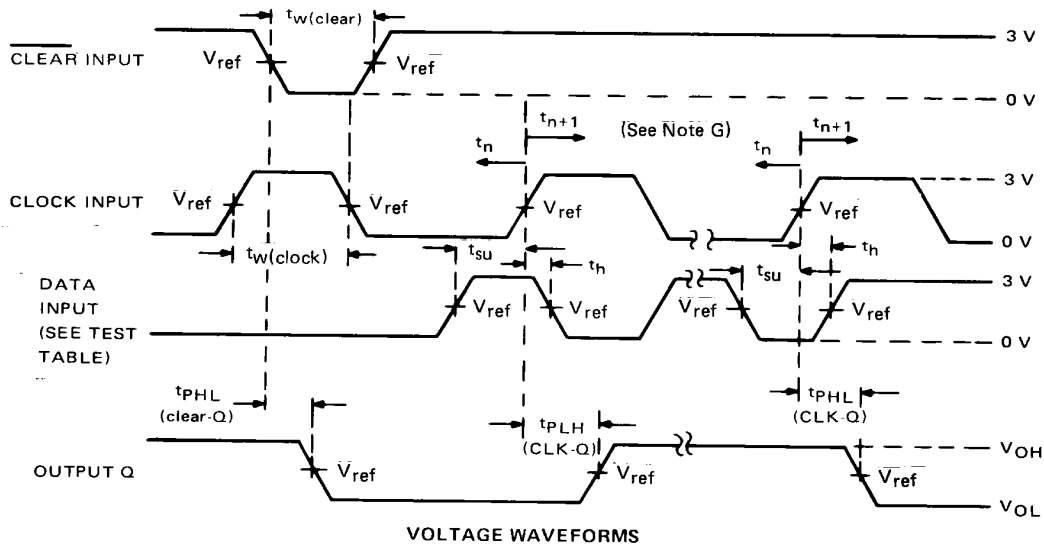
## PARAMETER MEASUREMENT INFORMATION



LOAD FOR OUTPUT UNDER TEST

TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	SHIFT/LOAD	OUTPUT TESTED (SEE NOTE F)
H	0 V	$Q_H$ at $t_{n+1}$
Serial Input	4.5 V	$Q_H$ at $t_{n+8}$



VOLTAGE WAVEFORMS

- NOTE: A. All pulse generators have the following characteristics:  $Z_{out} \approx 50\Omega$ ; for '166,  $t_r \leq 7$  ns and  $t_f \leq 7$  ns; for 'LS166A,  $t_r \leq 15$  ns and  $t_f \leq 6$  ns.
- B. The clock pulse has the following characteristics:  $t_w(\text{clock}) \leq 20$  ns and  $\text{PRR} = 1$  MHz. The clear pulse has the following characteristics:  $t_w(\text{clear}) \leq 20$  ns and  $t_{\text{hold}} = 0$  ns. When testing  $f_{\text{max}}$ , vary the clock PRR.
- C.  $C_L$  includes probe and jig capacitance.
- D. All diodes are 1N3064, 1N916, or equivalent.
- E. A clear pulse is applied prior to each test.
- F. Propagation delay times ( $t_{PLH}$  and  $t_{PHL}$ ) are measured at  $t_{n+1}$ . Proper shifting of data is verified at  $t_{n+8}$  with a functional test.
- G.  $t_n$  = bit time before clocking transition  
 $t_{n+1}$  = bit time after one clocking transition  
 $t_{n+8}$  = bit time after eight clocking transitions
- H. For '166  $V_{ref} = 1.5$  V; for 'LS166A  $V_{ref} = 1.3$  V.

FIGURE 1

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">5962-9558301QE A</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9558301QE A SNJ54166J
<a href="#">5962-9558301QF A</a>	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9558301QF A SNJ54166W
<a href="#">5962-9558301QFA</a>	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9558301QF A SNJ54166W
<a href="#">8001701EA</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8001701EA SNJ54LS166AJ
<a href="#">8001701EA</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8001701EA SNJ54LS166AJ
<a href="#">8001701FA</a>	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8001701FA SNJ54LS166AW
<a href="#">8001701FA</a>	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8001701FA SNJ54LS166AW
<a href="#">JM38510/30609B2A</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 30609B2A
<a href="#">JM38510/30609B2A</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 30609B2A
<a href="#">JM38510/30609BEA</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 30609BEA
<a href="#">JM38510/30609BEA</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 30609BEA
<a href="#">SN54166J</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54166J
<a href="#">SN54166J</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54166J
<a href="#">SN54LS166AJ</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS166AJ
<a href="#">SN54LS166AJ</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS166AJ
<a href="#">SN74LS166AD</a>	Obsolete	Production	SOIC (D)   16	-	-	Call TI	Call TI	0 to 70	LS166A
<a href="#">SN74LS166AD</a>	Obsolete	Production	SOIC (D)   16	-	-	Call TI	Call TI	0 to 70	LS166A
<a href="#">SN74LS166ADR</a>	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS166A
<a href="#">SN74LS166ADR</a>	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS166A



Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74LS166AN</a>	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS166AN
<a href="#">SN74LS166AN</a>	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS166AN
<a href="#">SN74LS166ANSR</a>	Active	Production	SOP (NS)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS166A
<a href="#">SN74LS166ANSR</a>	Active	Production	SOP (NS)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS166A
<a href="#">SNJ54166J</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9558301QE A SNJ54166J
<a href="#">SNJ54166J</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9558301QE A SNJ54166J
<a href="#">SNJ54166W</a>	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9558301QF A SNJ54166W
<a href="#">SNJ54166W</a>	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9558301QF A SNJ54166W
<a href="#">SNJ54LS166AFK</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS 166AFK
<a href="#">SNJ54LS166AFK</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS 166AFK
<a href="#">SNJ54LS166AJ</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8001701EA SNJ54LS166AJ
<a href="#">SNJ54LS166AJ</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8001701EA SNJ54LS166AJ
<a href="#">SNJ54LS166AW</a>	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8001701FA SNJ54LS166AW
<a href="#">SNJ54LS166AW</a>	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8001701FA SNJ54LS166AW

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54LS166A, SN74LS166A :**

- Catalog : [SN74LS166A](#)
- Military : [SN54LS166A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS166ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LS166ANSR	SOP	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS166ADR	SOIC	D	16	2500	353.0	353.0	32.0
SN74LS166ANSR	SOP	NS	16	2000	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9558301QFA	W	CFP	16	25	506.98	26.16	6220	NA
8001701FA	W	CFP	16	25	506.98	26.16	6220	NA
JM38510/30609B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
M38510/30609B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN74LS166AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS166AN	N	PDIP	16	25	506	13.97	11230	4.32
SNJ54166W	W	CFP	16	25	506.98	26.16	6220	NA
SNJ54LS166AFK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LS166AW	W	CFP	16	25	506.98	26.16	6220	NA



# PACKAGE OUTLINE

## NS0016A

### SOP - 2.00 mm max height

SOP



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#### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

# EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP2-F16

## GENERIC PACKAGE VIEW

**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

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