

**SN5420, SN54LS20, SN54S20,  
SN7420, SN74LS20, SN74S20**  
**DUAL 4-INPUT POSITIVE-NAND GATES**  
DECEMBER 1983—REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

**description**

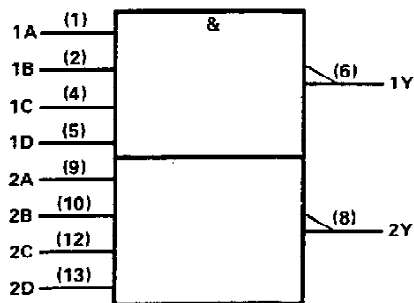
These devices contain two independent 4-input NAND gates.

The SN5420, SN54LS20, and SN54S20 are characterized for operation over the full military range of -55°C to 125°C. The SN7420, SN74LS20, and SN74S20 are characterized for operation from 0°C to 70°C.

**FUNCTION TABLE (each gate)**

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

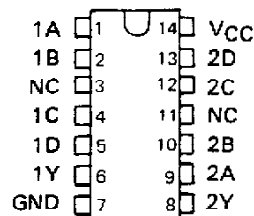
**logic symbol†**



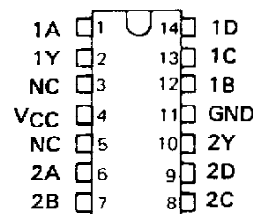
†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

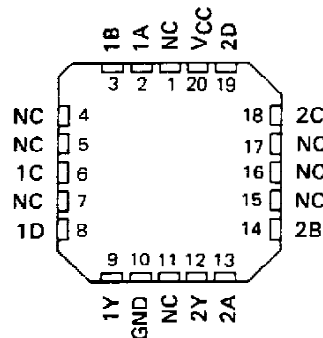
SN5420 . . . J PACKAGE  
SN54LS20, SN54S20 . . . J OR W PACKAGE  
SN7420 . . . N PACKAGE  
SN74LS20, SN74S20 . . . D OR N PACKAGE  
(TOP VIEW)



SN5420 . . . W PACKAGE  
(TOP VIEW)

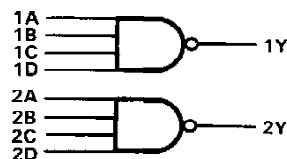


SN54LS20, SN54S20 . . . FK PACKAGE  
(TOP VIEW)



NC - No internal connection

**logic diagram**



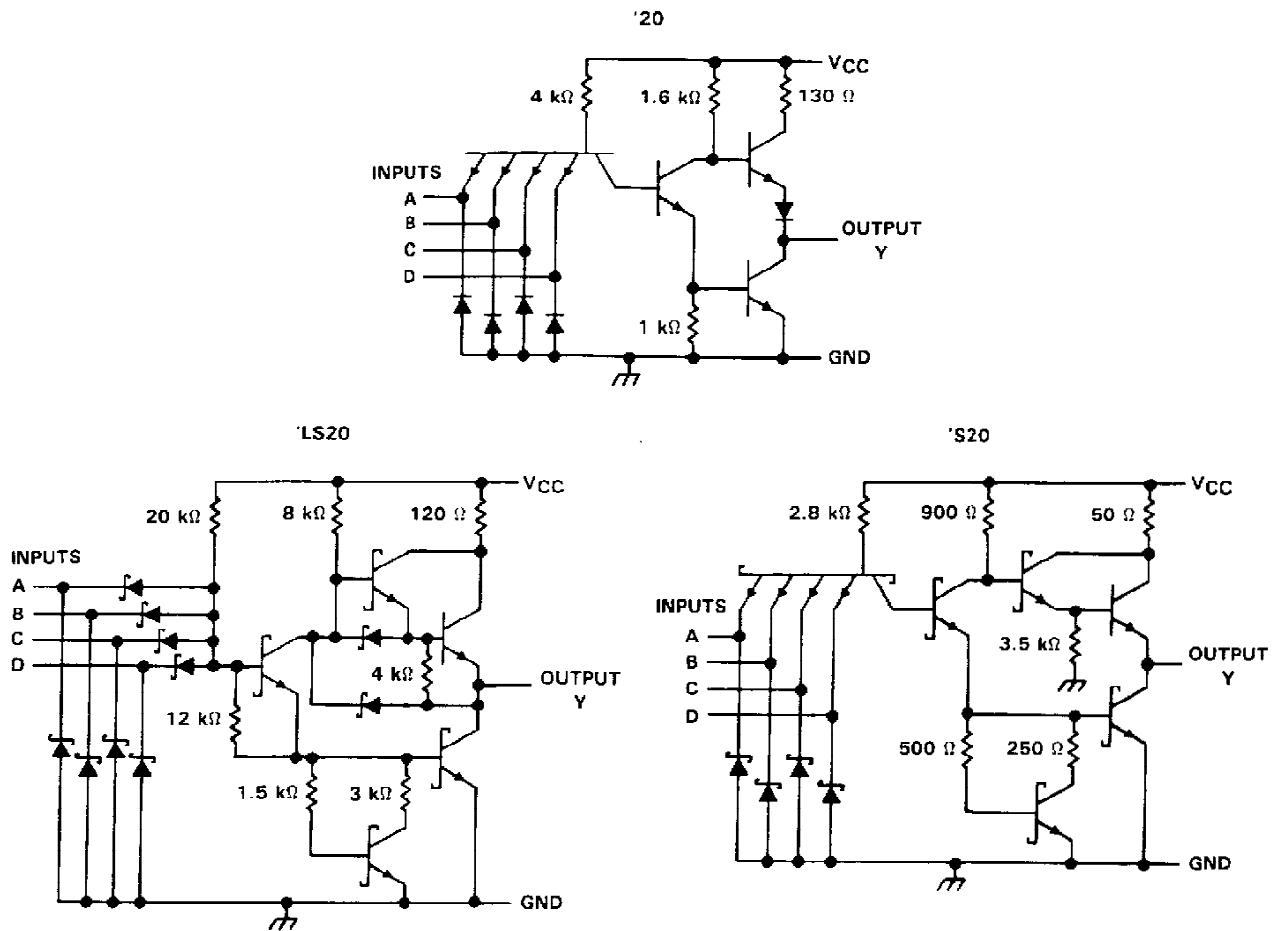
positive logic  $Y = \overline{A \cdot B \cdot C \cdot D}$  or  $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



**SN5420, SN54LS20, SN54S20,  
SN7420, SN74LS20, SN74S20  
DUAL 4-INPUT POSITIVE-NAND GATES**

schematics (each gate)



Resistor values shown are nominal.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage, V <sub>CC</sub> (see Note 1) .....	7 V
Input voltage: '20, 'S20 .....	5.5 V
'LS20 .....	7 V
Operating free-air temperature range: SN54' .....	-55°C to 125°C
SN74' .....	0°C to 70°C
Storage temperature range .....	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminals.

**SN5420, SN7420**  
**DUAL 4-INPUT POSITIVE-NAND GATES**

**recommended operating conditions**

	SN5420			SN7420			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub> Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub> High-level input voltage	2			2			V
V <sub>IL</sub> Low-level input voltage			0.8			0.8	V
I <sub>OH</sub> High-level output current			-0.4			-0.4	mA
I <sub>OL</sub> Low-level output current			16			16	mA
T <sub>A</sub> Operating free-air temperature	-55		125	0		70	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS †	SN5420			SN7420			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = MIN, I <sub>I</sub> = -12 mA			-1.5			-1.5	V
V <sub>OH</sub>	V <sub>CC</sub> = MIN, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -0.4 mA	2.4	3.4		2.4	3.4		V
V <sub>OL</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 16 mA		0.2	0.4		0.2	0.4	V
I <sub>I</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V			1			1	mA
I <sub>IH</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.4 V			40			40	μA
I <sub>IL</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V			-1.6			-1.6	mA
I <sub>OS</sub> §	V <sub>CC</sub> = MAX	-20		-55	-18		-55	mA
I <sub>CCH</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0 V		2	4		2	4	mA
I <sub>CCL</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 4.5 V		6	11		6	11	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time.

**switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see note 2)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	Any	Y	R <sub>L</sub> = 400 Ω, C <sub>L</sub> = 15 pF		12	22	ns
t <sub>PHL</sub>					8	15	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



# SN54LS20, SN74LS20 DUAL 4-INPUT POSITIVE-NAND GATES

## recommended operating conditions

	SN54LS20			SN74LS20			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub> Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub> High-level input voltage	2			2			V
V <sub>IL</sub> Low-level input voltage			0.7			0.8	V
I <sub>OH</sub> High-level output current			-0.4			-0.4	mA
I <sub>OL</sub> Low-level output current			4			8	mA
T <sub>A</sub> Operating free-air temperature	-55		125	0		70	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS20			SN74LS20			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA			-1.5			-1.5	V
V <sub>OH</sub>	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, I <sub>OH</sub> = -0.4 mA	2.5	3.4		2.7	3.4		V
V <sub>OL</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 4 mA		0.25	0.4			0.4	V
	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 8 mA					0.25	0.5	
I <sub>I</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V			0.1			0.1	mA
I <sub>IH</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V			20			20	μA
I <sub>IL</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V			-0.4			-0.4	mA
I <sub>OS</sub> §	V <sub>CC</sub> = MAX	-20		-100	-20		-100	mA
I <sub>CCH</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0 V		0.4	0.8		0.4	0.8	mA
I <sub>CCL</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 4.5 V		1.2	2.2		1.2	2.2	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

## switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	Any	Y	R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 15 pF		9	15	ns
t <sub>PHL</sub>					10	15	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

  
TEXAS  
INSTRUMENTS

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

**SN54S20, SN74S20**  
**DUAL 4-INPUT POSITIVE-NAND GATES**

**recommended operating conditions**

	SN54S20			SN74S20			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub> Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub> High-level input voltage	2			2			V
V <sub>IL</sub> Low-level input voltage			0.8			0.8	V
I <sub>OH</sub> High-level output current			-1			-1	mA
I <sub>OL</sub> Low-level output current			20			20	mA
T <sub>A</sub> Operating free-air temperature	-55		125	0		70	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS †	SN54S20			SN74S20			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA			-1.2			-1.2	V
V <sub>OH</sub>	V <sub>CC</sub> = MIN, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -1 mA	2.5	3.4		2.7	3.4		V
V <sub>OL</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 20 mA			0.5			0.5	V
I <sub>I</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V			1			1	mA
I <sub>IH</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V			50			50	µA
I <sub>IL</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5 V			-2			-2	mA
I <sub>OS</sub> §	V <sub>CC</sub> = MAX	-40		-100	-40		-100	mA
I <sub>CCH</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0 V		5	8		5	8	mA
I <sub>CCL</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 4.5 V		10	18		10	18	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

**switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see note 2)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	A, B, C or D	Y	R <sub>L</sub> = 280 Ω, C <sub>L</sub> = 15 pF		3	4.5	ns
t <sub>PHL</sub>					3	5	ns
t <sub>PLH</sub>			R <sub>L</sub> = 280 Ω, C <sub>L</sub> = 50 pF		4.5		ns
t <sub>PHL</sub>					5		ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
JM38510/07006BCA	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/07006BCA
JM38510/07006BDA	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/07006BDA
JM38510/07006BDA	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/07006BDA
JM38510/30007B2A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/30007B2A
JM38510/30007B2A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/30007B2A
JM38510/30007BCA	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/30007BCA
JM38510/30007BCA	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/30007BCA
JM38510/30007BDA	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/30007BDA
JM38510/30007BDA	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/30007BDA
SN54LS20J	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS20J
SN54LS20J	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS20J
SN54S20J	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54S20J
SN54S20J	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54S20J
SN74LS20D	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	0 to 70	LS20
SN74LS20D	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	0 to 70	LS20
SN74LS20DR	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS20
SN74LS20DR	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS20
SN74LS20N	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS20N
SN74LS20N	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS20N
SN74LS20NSR	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS20
SN74LS20NSR	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS20
SN74S20D	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	S20

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74S20D</a>	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	S20
<a href="#">SN74S20N</a>	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74S20N
<a href="#">SN74S20N</a>	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74S20N
<a href="#">SNJ54LS20FK</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS20FK
<a href="#">SNJ54LS20FK</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS20FK
<a href="#">SNJ54LS20J</a>	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS20J
<a href="#">SNJ54LS20J</a>	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS20J
<a href="#">SNJ54LS20W</a>	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS20W
<a href="#">SNJ54LS20W</a>	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS20W
<a href="#">SNJ54S20J</a>	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54S20J
<a href="#">SNJ54S20J</a>	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54S20J
<a href="#">SNJ54S20W</a>	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54S20W
<a href="#">SNJ54S20W</a>	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54S20W

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54LS20, SN54S20, SN74LS20, SN74S20 :**

- Catalog : [SN74LS20](#), [SN74S20](#)
- Military : [SN54LS20](#), [SN54S20](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS20DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LS20NSR	SOP	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS20DR	SOIC	D	14	2500	356.0	356.0	35.0
SN74LS20NSR	SOP	NS	14	2000	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
JM38510/07006BDA	W	CFP	14	25	506.98	26.16	6220	NA
JM38510/30007B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/30007BDA	W	CFP	14	25	506.98	26.16	6220	NA
M38510/07006BDA	W	CFP	14	25	506.98	26.16	6220	NA
M38510/30007B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
M38510/30007BDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74LS20N	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS20NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74S20D	D	SOIC	14	50	506.6	8	3940	4.32
SN74S20N	N	PDIP	14	25	506	13.97	11230	4.32
SN74S20N	N	PDIP	14	25	506	13.97	11230	4.32
SN74S20NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74S20NE4	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54LS20FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LS20W	W	CFP	14	25	506.98	26.16	6220	NA

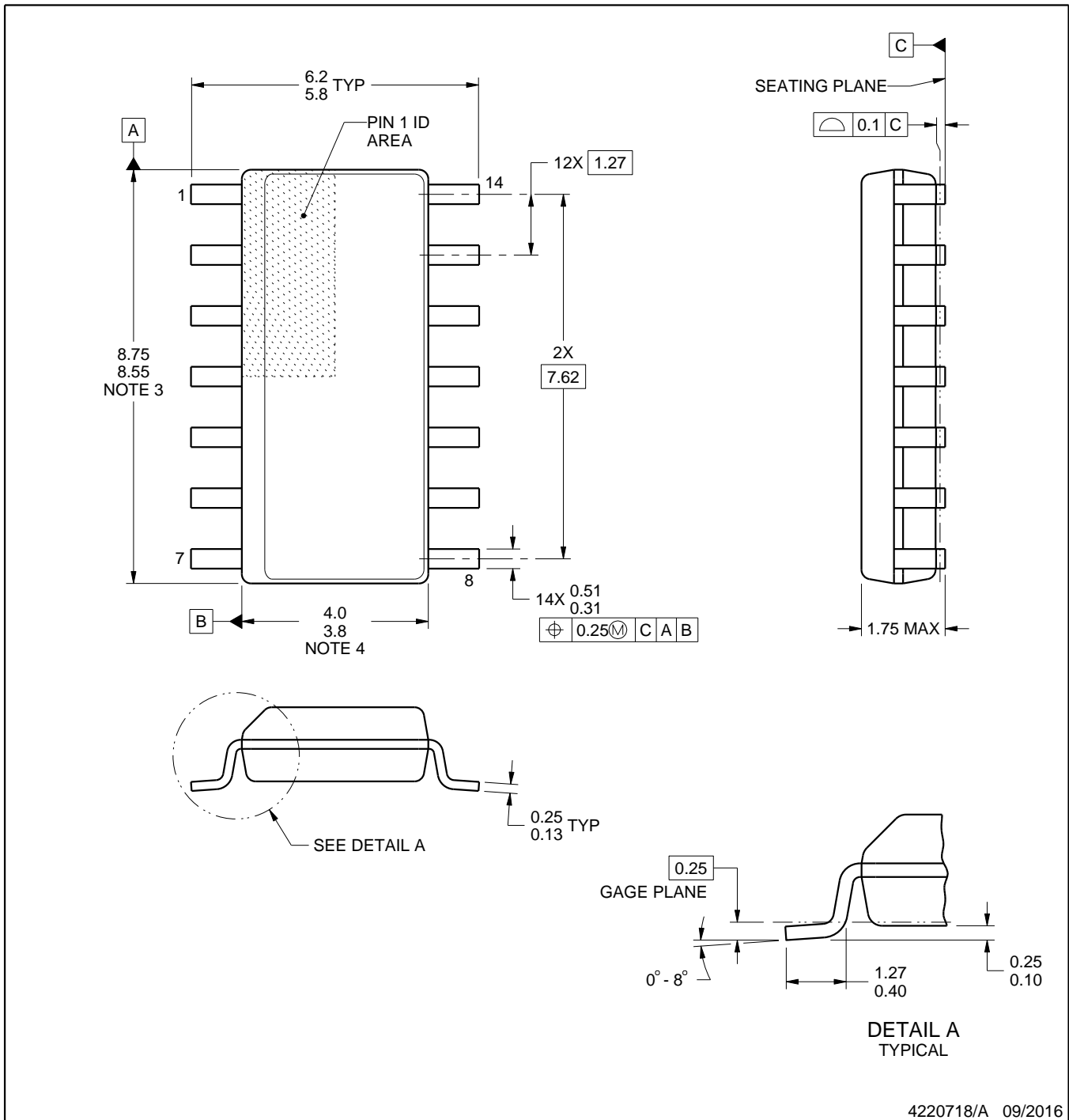
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# PACKAGE OUTLINE

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

- All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

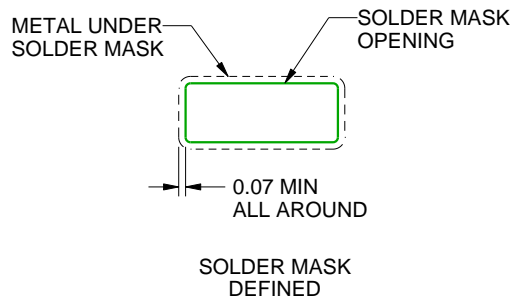
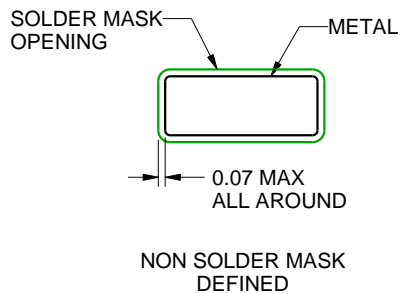
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F14



## GENERIC PACKAGE VIEW

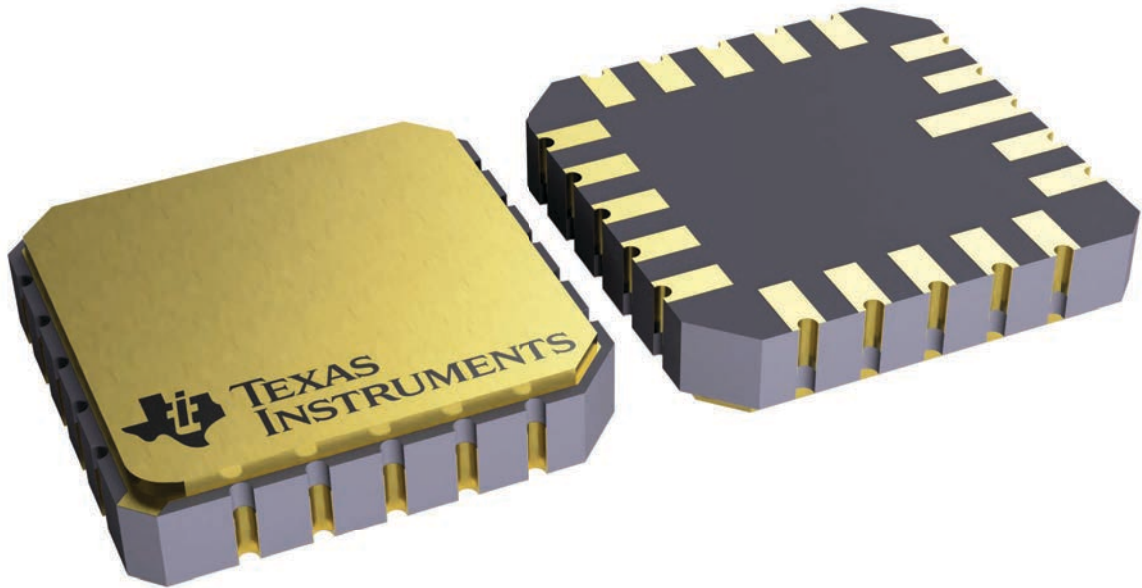
**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

J 14

**GENERIC PACKAGE VIEW**  
**CDIP - 5.08 mm max height**  
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

J0014A



# PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

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