

# SN5485, SN54LS85, SN54S85 SN7485, SN74LS85, SN74S85 4-BIT MAGNITUDE COMPARATORS

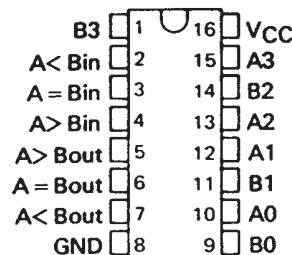
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TYPE	TYPICAL POWER DISSIPATION	TYPICAL DELAY (4-BIT WORDS)
'85	275 mW	23 ns
'LS85	52 mW	24 ns
'S85	365 mW	11 ns

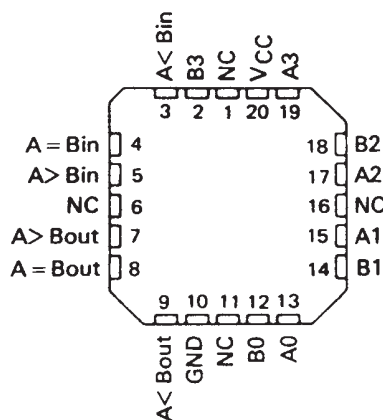
## description

These four-bit magnitude comparators perform comparison of straight binary and straight BCD (8-4-2-1) codes. Three fully decoded decisions about two 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The  $A > B$ ,  $A < B$ , and  $A = B$  outputs of a stage handling less-significant bits are connected to the corresponding  $A > B$ ,  $A < B$ , and  $A = B$  inputs of the next stage handling more-significant bits. The stage handling the least-significant bits must have a high-level voltage applied to the  $A = B$  input. The cascading paths of the '85, 'LS85, and 'S85 are implemented with only a two-gate-level delay to reduce overall comparison times for long words. An alternate method of cascading which further reduces the comparison time is shown in the typical application data.

SN5485, SN54LS85, SN54S85 . . . J OR W PACKAGE  
SN7485 . . . N PACKAGE  
SN74LS85, SN74S85 . . . D OR N PACKAGE  
(TOP VIEW)



SN54LS85, SN54S85 . . . FK PACKAGE  
(TOP VIEW)



NC - No internal connection

FUNCTION TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B2	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A2 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L

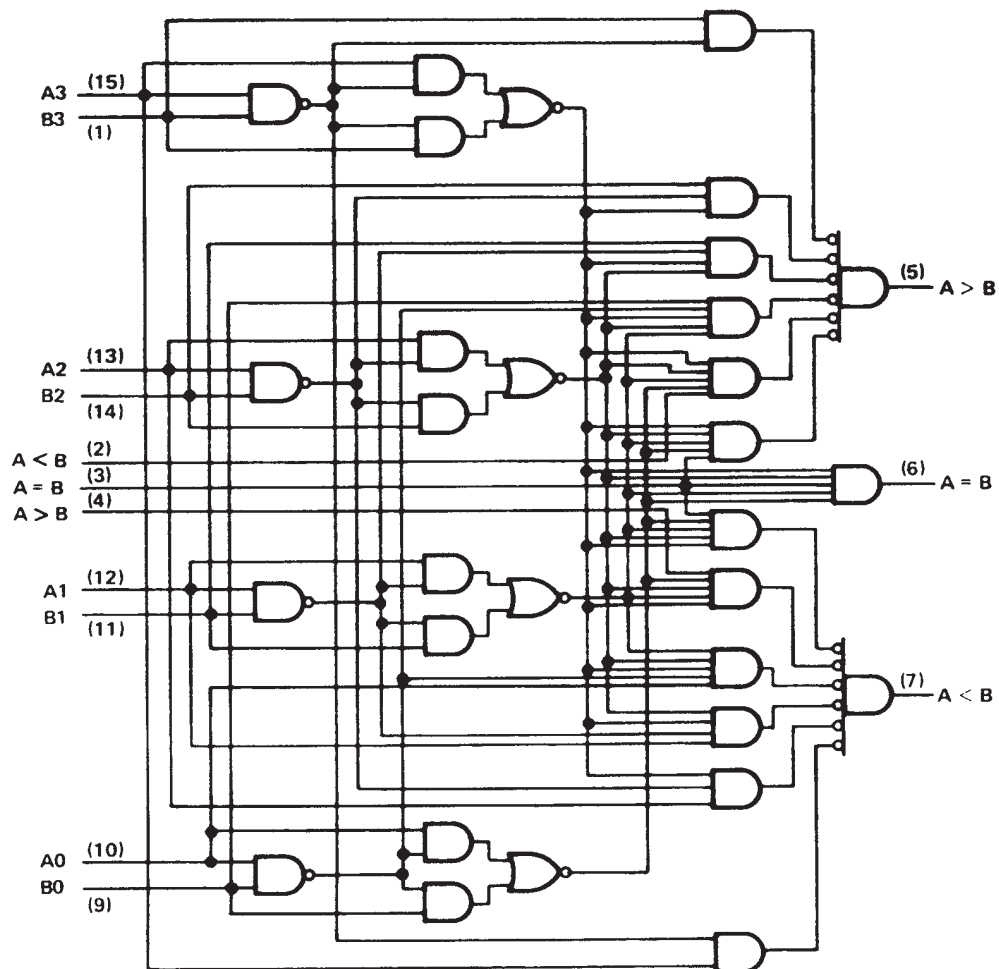
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



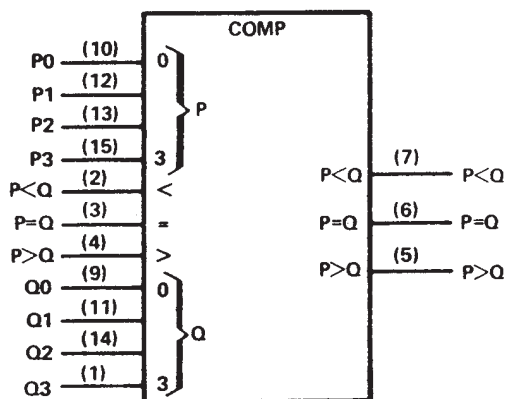
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logic diagrams (positive logic)



logic symbol †

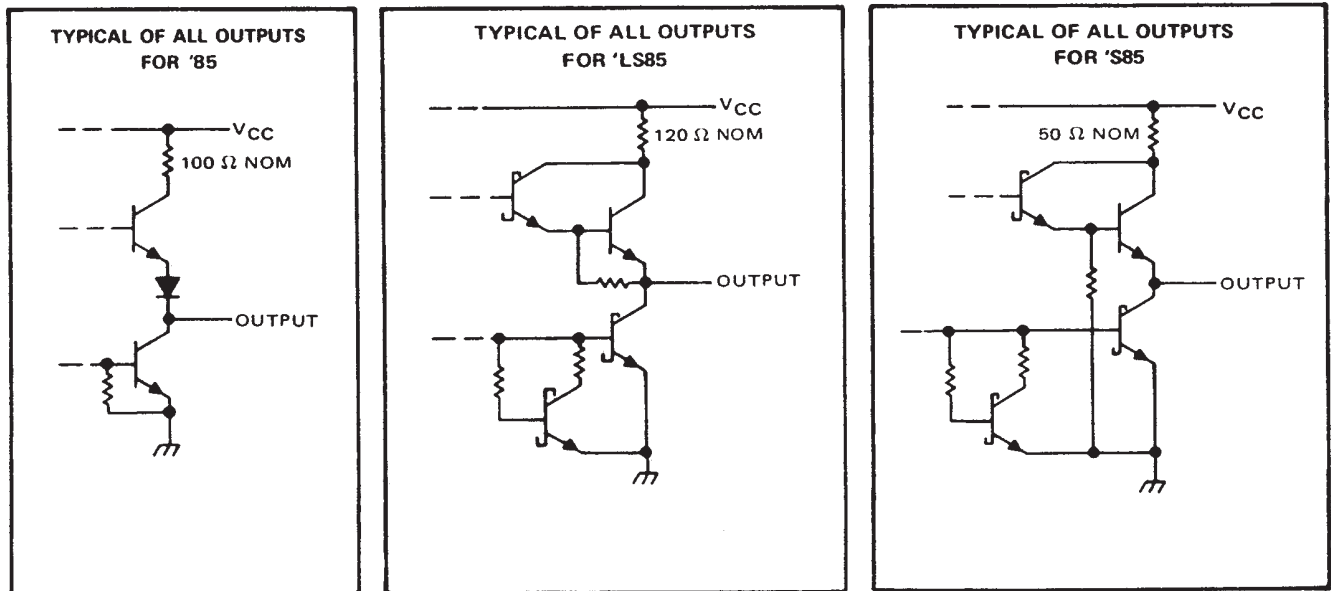
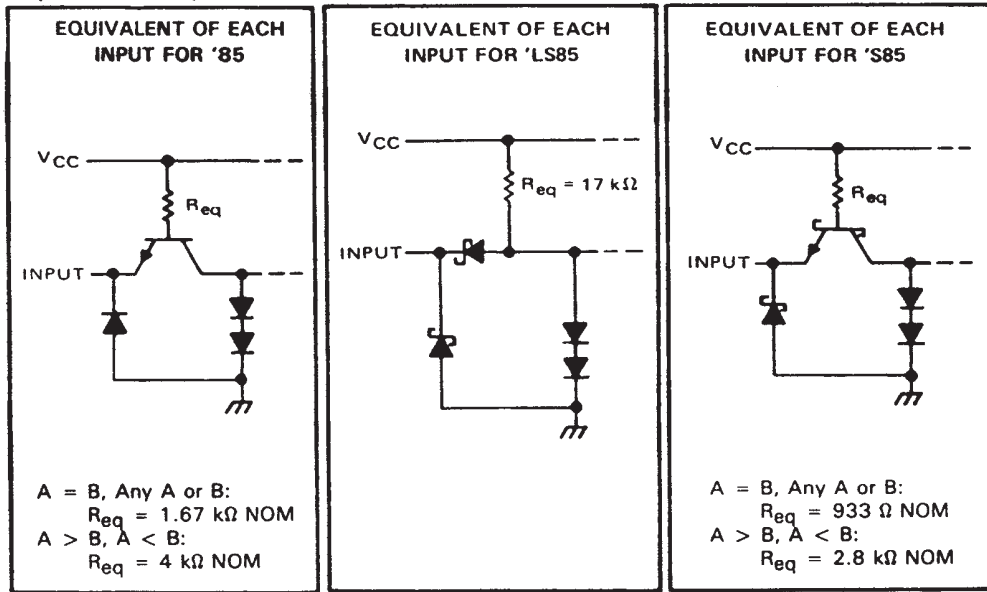


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
 Pin numbers shown are for D, J, N, and W packages.



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schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN54' SN54S'	SN54LS'	SN74' SN74S'	SN74LS'	UNIT
Supply voltage, $V_{CC}$ (see Note 1)	7	7	7	7	V
Input voltage	5.5	7	5.5	7	V
Interemitter voltage (see Note 2)	5.5		5.5		V
Operating free-air temperature range	-55 to 125		-0 to 70		°C
Storage temperature range	-65 to 150		-65 to 150		°C

- NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.  
 2. This is the voltage between two emitters of a multiple-emitter input transistor. This rating applies to each A input in conjunction with its respective B input of the '85 and 'S85.

**SN5485, SN54LS85, SN54S85  
SN7485, SN74LS85, SN74S85  
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**recommended operating conditions**

	SN5485			SN7485			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$	-400			-400			$\mu A$
Low-level output current, $I_{OL}$	16			16			mA
Operating free-air temperature, $T_A$	-55			125			$^{\circ}C$

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$V_{IH}$	High-level input voltage		2			V
$V_{IL}$	Low-level input voltage				0.8	V
$V_{IK}$	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5	V
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OH} = -400 \mu A$	2.4	3.4		V
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 16 \text{ mA}$	0.2	0.4		V
$I_I$	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
$I_{IH}$	High-level input current	A < B, A > B inputs			40	$\mu A$
		all other inputs			120	
$I_{IL}$	Low-level input current	A < B, A > B inputs			-1.6	mA
		all other inputs			-4.8	
$I_{OS}$	Short-circuit output current§	$V_{CC} = \text{MAX}, V_O = 0$	SN5485	-20	-55	mA
			SN7485	-18	-55	
$I_{CC}$	Supply current	$V_{CC} = \text{MAX},$ See Note 4		55	88	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}C$ .

§ Not more than one output should be shorted at a time.

NOTE 4:  $I_{CC}$  is measured with outputs open, A = B grounded, and all other inputs at 4.5 V.

**switching characteristics,  $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}C$**

PARAMETER¶	FROM INPUT	TO OUTPUT	NUMBER OF GATE LEVELS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	Any A or B data input	A < B, A > B	1	$C_L = 15 \text{ pF}, R_L = 400 \Omega,$ See Note 5		7		ns
			2			12		
		3			17	26		
		4			23	35		
$t_{PHL}$	Any A or B data input	A < B, A > B	1			11		ns
			2			15		
		3			20	30		
		4			20	30		
$t_{PLH}$	A < B or A = B	A > B	1			7	11	ns
$t_{PHL}$	A < B or A = B	A > B	1			11	17	ns
$t_{PLH}$	A = B	A = B	2		13	20	ns	
$t_{PHL}$	A = B	A = B	2		11	17	ns	
$t_{PLH}$	A > B or A = B	A < B	1		7	11	ns	
$t_{PHL}$	A > B or A = B	A < B	1		11	17	ns	

¶  $t_{PLH}$  = propagation delay time, low-to-high-level output

$t_{PHL}$  = propagation delay time, high-to-low-level output

NOTE 5: Load circuits and voltage waveforms are shown in Section 1.



**recommended operating conditions**

	SN54LS85			SN74LS85			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$			-400			-400	$\mu$ A
Low-level output current, $I_{OL}$			4			8	mA
Operating free-air temperature, $T_A$	-55		125	0		70	$^{\circ}$ C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS <sup>†</sup>	SN54LS85		SN74LS85		UNIT
			MIN	TYP <sup>‡</sup>	MAX	MIN	
$V_{IH}$	High-level input voltage		2		2		V
$V_{IL}$	Low-level input voltage			0.7		0.7	V
$V_{IK}$	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$		-1.5		-1.5	V
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$	2.5	3.4	2.7	3.4	V
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}, I_{OL} = 4 \text{ mA}$	0.25	0.4	0.25	0.4	V
		$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 8 \text{ mA}$			0.35	0.5	
$I_I$	Input current at maximum input voltage	A < B, A > B inputs	0.1		0.1		mA
		all other inputs	0.3		0.3		
$I_{IH}$	High-level input current	A < B, A > B inputs	20		20		$\mu$ A
		all other inputs	60		60		
$I_{IL}$	Low-level input current	A < B, A > B inputs	-0.4		-0.4		mA
		all other inputs	-1.2		-1.2		
$I_{OS}$	Short-circuit output current <sup>§</sup>	$V_{CC} = \text{MAX}$	-20	-100	-20	-100	mA
$I_{CC}$	Supply current	$V_{CC} = \text{MAX}, \text{ See Note 4}$	10.4	20	10.4	20	mA

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup>All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$ .

<sup>§</sup>Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 4:  $I_{CC}$  is measured with outputs open, A = B grounded, and all other inputs at 4.5 V.

**switching characteristics,  $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$**

PARAMETER <sup>†</sup>	FROM INPUT	TO OUTPUT	NUMBER OF GATE LEVELS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	Any A or B data input	A < B, A > B	1	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega, \text{ See Note 5}$		14		ns
			2			19		
			3			24	36	
			4			27	45	
$t_{PHL}$	Any A or B data input	A < B, A > B	1			11		ns
			2			15		
			3			20	30	
			4			23	45	
$t_{PLH}$	A < B or A = B	A > B	1			14	22	ns
$t_{PHL}$	A < B or A = B	A > B	1			11	17	ns
$t_{PLH}$	A = B	A = B	2			13	20	ns
$t_{PHL}$	A = B	A = B	2			13	26	ns
$t_{PLH}$	A > B or A = B	A < B	1		14	22	ns	
$t_{PHL}$	A > B or A = B	A < B	1		11	17	ns	

<sup>†</sup> $t_{PLH}$  = propagation delay time, low-to-high-level output

$t_{PHL}$  = propagation delay time, high-to-low-level output

NOTE 5: Load circuits and voltage waveforms are shown in Section 1.

**SN5485, SN54LS85, SN54S85  
SN7485, SN74LS85, SN74S85  
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**recommended operating conditions**

	SN54S85			SN74S85			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$			-1			-1	mA
Low-level output current, $I_{OL}$			20			20	mA
Operating free-air temperature, $T_A$	-55		125	0		70	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$V_{IH}$	High-level input voltage		2			V
$V_{IL}$	Low-level input voltage				0.8	V
$V_{IK}$	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.2	V
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -1 \text{ mA}$	SN54S85 2.5	3.4		V
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 20 \text{ mA}$			0.5	V
$I_I$	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
$I_{IH}$	High-level input current	A < B, A > B inputs	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$		50	$\mu\text{A}$
		all other inputs			150	
$I_{IL}$	Low-level input current	A < B, A > B inputs	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$		-2	mA
		all other inputs			-6	
$I_{OS}$	Short-circuit output current§	$V_{CC} = \text{MAX}$	-40		-100	mA
$I_{CC}$	Supply current	$V_{CC} = \text{MAX}$ , See Note 4		73	115	mA
		$V_{CC} = \text{MAX}, T_A = 125^\circ\text{C}$ , See Note 4	SN54S85W			

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 4:  $I_{CC}$  is measured with outputs open, A = B grounded, and all other inputs at 4.5 V.

**switching characteristics,  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$**

PARAMETER¶	FROM INPUT	TO OUTPUT	NUMBER OF GATE LEVELS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	Any A or B data input	A < B, A > B	1	$C_L = 15 \text{ pF}, R_L = 280 \Omega,$ See Note 5		5		ns
			2		7.5			
		3	10.5		16			
		4	12		18			
$t_{PHL}$	Any A or B data input	A < B, A > B	1		5.5		ns	
			2		7			
		3	11		16.5			
		4	11		16.5			
$t_{PLH}$	A < B or A = B	A > B	1			5	7.5	ns
$t_{PHL}$	A < B or A = B	A > B	1			5.5	8.5	ns
$t_{PLH}$	A = B	A = B	2		7	10.5	ns	
$t_{PHL}$	A = B	A = B	2		5	7.5	ns	
$t_{PLH}$	A > B or A = B	A < B	1		5	7.5	ns	
$t_{PHL}$	A > B or A = B	A < B	1		5.5	8.5	ns	

¶  $t_{PLH}$  = propagation delay time, low-to-high-level output

$t_{PHL}$  = propagation delay time, high-to-low-level output

NOTE 5: Load circuits and voltage waveforms are shown in Section 1.





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SN7485, SN74LS85, SN74S85  
**4-BIT MAGNITUDE COMPARATORS**

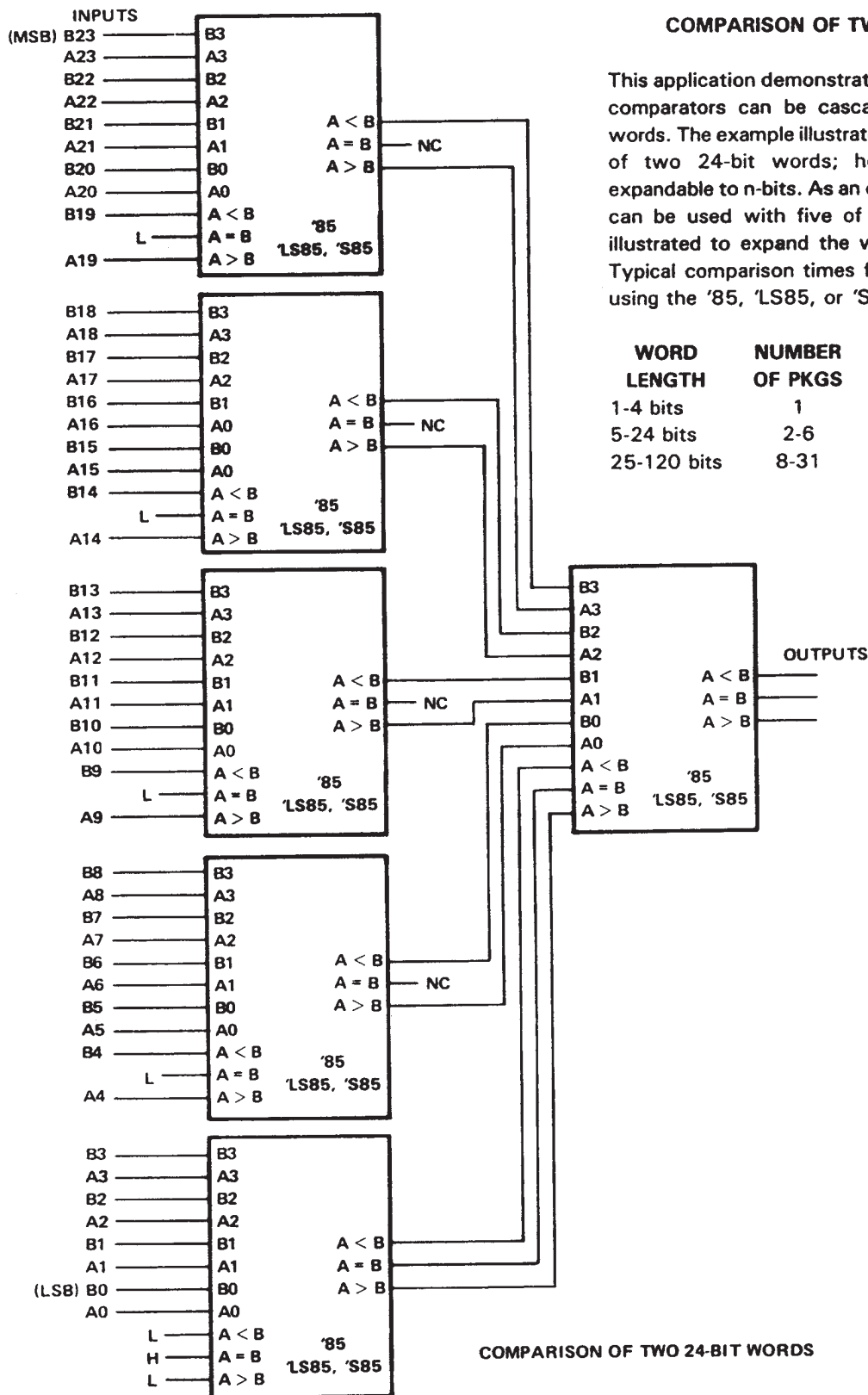
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**TYPICAL APPLICATION DATA**

**COMPARISON OF TWO N-BIT WORDS**

This application demonstrates how these magnitude comparators can be cascaded to compare longer words. The example illustrated shows the comparison of two 24-bit words; however, the design is expandable to n-bits. As an example, one comparator can be used with five of the 24-bit comparators illustrated to expand the word length to 120-bits. Typical comparison times for various word lengths using the '85, 'LS85, or 'S85 are:

WORD LENGTH	NUMBER OF PKGS	'85	'LS85	'S85
1-4 bits	1	23 ns	24 ns	11 ns
5-24 bits	2-6	46 ns	48 ns	22 ns
25-120 bits	8-31	69 ns	72 ns	33 ns



**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">5962-9754701Q2A</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9754701Q2A SNJ54LS 85FK
<a href="#">5962-9754701QEA</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9754701QE A SNJ54LS85J
<a href="#">5962-9754701QFA</a>	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9754701QF A SNJ54LS85W
<a href="#">JM38510/08201BEA</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 08201BEA
<a href="#">JM38510/31101B2A</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 31101B2A
<a href="#">JM38510/31101BEA</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 31101BEA
<a href="#">JM38510/31101BFA</a>	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 31101BFA
<a href="#">SN54LS85J</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS85J
<a href="#">SN54S85J</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54S85J
<a href="#">SN74LS85D</a>	Obsolete	Production	SOIC (D)   16	-	-	Call TI	Call TI	0 to 70	LS85
<a href="#">SN74LS85DR</a>	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS85
<a href="#">SN74LS85N</a>	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS85N
<a href="#">SN74LS85NSR</a>	Active	Production	SOP (NS)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS85
<a href="#">SN74S85D</a>	Active	Production	SOIC (D)   16	40   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	S85
<a href="#">SN74S85N</a>	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74S85N
<a href="#">SNJ54LS85FK</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9754701Q2A SNJ54LS 85FK
<a href="#">SNJ54LS85J</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9754701QE A SNJ54LS85J



Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SNJ54LS85W</a>	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9754701QF A SNJ54LS85W
<a href="#">SNJ54S85FK</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54S 85FK
<a href="#">SNJ54S85J</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54S85J

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54LS85, SN54S85, SN74LS85, SN74S85 :**

- Catalog : [SN74LS85](#), [SN74S85](#)
- Military : [SN54LS85](#), [SN54S85](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

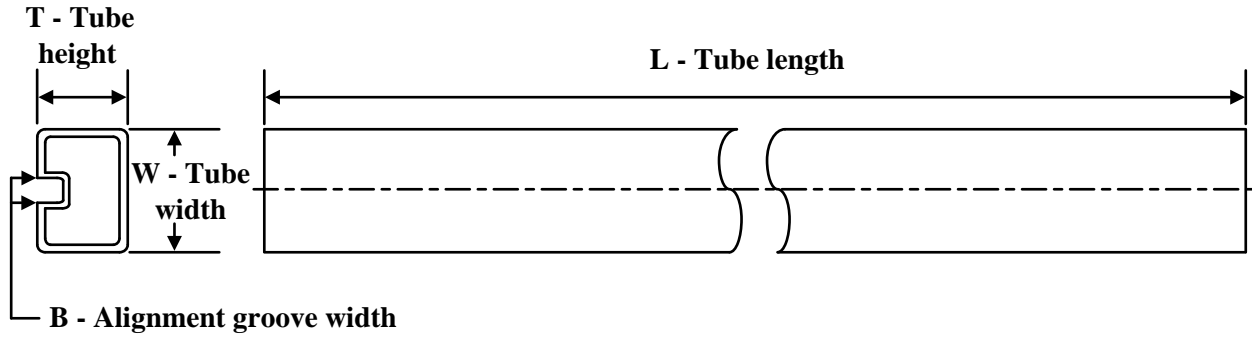

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS85DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LS85NSR	SOP	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS85DR	SOIC	D	16	2500	340.5	336.1	32.0
SN74LS85NSR	SOP	NS	16	2000	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9754701Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9754701QFA	W	CFP	16	25	506.98	26.16	6220	NA
JM38510/31101B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/31101BFA	W	CFP	16	25	506.98	26.16	6220	NA
M38510/31101B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
M38510/31101BFA	W	CFP	16	25	506.98	26.16	6220	NA
SN74LS85N	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS85N	N	PDIP	16	25	506	13.97	11230	4.32
SN74S85D	D	SOIC	16	40	507	8	3940	4.32
SN74S85N	N	PDIP	16	25	506	13.97	11230	4.32
SN74S85N	N	PDIP	16	25	506	13.97	11230	4.32
SNJ54LS85FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LS85W	W	CFP	16	25	506.98	26.16	6220	NA
SNJ54S85FK	FK	LCCC	20	55	506.98	12.06	2030	NA

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.



# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP2-F16

## GENERIC PACKAGE VIEW

**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - (C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.



# PACKAGE OUTLINE

## NS0016A

### SOP - 2.00 mm max height

SOP



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#### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



# EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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