TEXAS INSTRUMENTS

SN74LV04A

SCLS388K –SEPTEMBER 1997–REVISED DECEMBER 2014

SN74LV04A Hex Inverters

1 Features

- 2-V to 5.5-V V_{CC} Operation
- Max t_{pd} of 6.5 ns at 5 V
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2.3 V at V_{CC} = 3.3 V, T_A = 25°C
- Support Mixed-Mode Voltage Operation on All Ports
- I_{off} Supports Partial-Power-Down Mode Operation
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model
  - 200-V Machine Model
  - 1000-V Charged-Device Model

2 Applications

- Power Sub-Station Controls
- Ethernet Switches
- Flow Meters
- I/O Modules; Digital PLC/DCS Inputs
- Servers
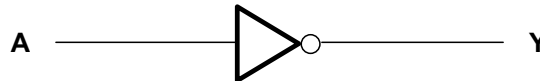- Tests and Measurement

3 Description

This hex inverter is designed for 2-V to 5.5-V V_{CC} operation. The SN74LV04A device contains six independent inverters. This device perform the Boolean function $Y = \overline{A}$.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LV04A	TVSOP (14)	3.60 mm x 4.40 mm
	SOIC (14)	8.65 mm x 3.91 mm
	VQFN (14)	3.50 mm x 3.50 mm
	SSOP (14)	6.20 mm x 5.30 mm
	TSSOP (14)	5.00 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic

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5 Revision History

Changes from Revision J (April 2005) to Revision K   **Page**

- Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. 1
- Deleted *Ordering Information* table. 1
- Changed MAX operating temperature to 125°C in *Recommended Operating Conditions* table. 5

6 Pin Configuration and Functions

**SN74LV04A . . . D, DB, DGV, NS,
OR PW PACKAGE
(TOP VIEW)**

1A	1	14 V_{CC}
1Y	2	13 6A
2A	3	12 6Y
2Y	4	11 5A
3A	5	10 5Y
3Y	6	9 4A
GND	7	8 4Y
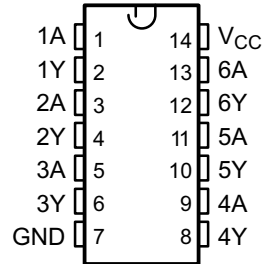
**SN74LV04A . . . RGY PACKAGE
(TOP VIEW)**

	1A	V_{CC}	
	1	14	
1Y	2	13	6A
2A	3	12	6Y
2Y	4	11	5A
3A	5	10	5Y
3Y	6	9	4A
	7	8	
	GND	4Y	
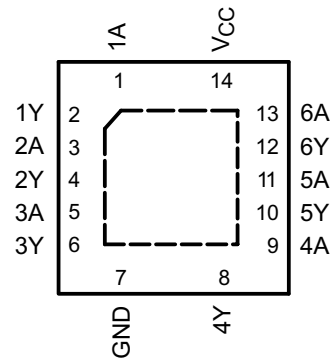
Pin Functions

PIN			TYPE	DESCRIPTION
NAME	**SN74LV04A**			
	D, DB, DGV, NS, PW	**RGY**		
1A	1	1	I	1A Input
1Y	2	2	O	1Y Output
2A	3	3	I	2A Input
2Y	4	4	O	2Y Output
3A	5	5	I	3A Input
3Y	6	6	O	3Y Output
4Y	8	8	O	4Y Output
4A	9	9	I	4A Input
5Y	10	10	O	5Y Output
5A	11	11	I	5A Input
6Y	12	12	O	6Y Output
6A	13	13	I	6A Input
GND	7	7	—	Ground Pin
V_{CC}	14	14	—	Power Pin

Product Folder Links: *SN74LV04A*

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	7	V
V_I	Input voltage range[2]		−0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state[2]		−0.5	7	V
V_O	Output voltage range[2][3]		−0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		−20	mA
I_{OK}	Output clamp current	$V_O < 0$		−50	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 5.5-V maximum.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Product Folder Links: *SN74LV04A*

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 2.3 V to 2.7 V	V_{CC} × 0.7		
		V_{CC} = 3 V to 3.6 V	V_{CC} × 0.7		
		V_{CC} = 4.5 V to 5.5 V	V_{CC} × 0.7		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 2.3 V to 2.7 V		V_{CC} × 0.3	
		V_{CC} = 3 V to 3.6 V		V_{CC} × 0.3	
		V_{CC} = 4.5 V to 5.5 V		V_{CC} × 0.3	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		−50	µA
		V_{CC} = 2.3 V to 2.7 V		−2	mA
		V_{CC} = 3 V to 3.6 V		−6	
		V_{CC} = 4.5 V to 5.5 V		−12	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	µA
		V_{CC} = 2.3 V to 2.7 V		2	mA
		V_{CC} = 3 V to 3.6 V		6	
		V_{CC} = 4.5 V to 5.5 V		12	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V		200	ns/V
		V_{CC} = 3 V to 3.6 V		100	
		V_{CC} = 4.5 V to 5.5 V		20	
T_A	Operating free-air temperature		−40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

7.4 Thermal Information

	THERMAL METRIC[1]	SN74LV04A						UNIT
		D	DB	DGV	NS	PW	RGY	
		14 PINS						
$R_{\theta JA}$	Junction-to-ambient thermal resistance	94.9	107.4	130.4	91.4	122.6	57.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.3	59.9	53.4	49.0	51.3	70.4	
$R_{\theta JB}$	Junction-to-board thermal resistance	49.2	54.7	63.5	50.2	64.4	33.6	
ψ_{JT}	Junction-to-top characterization parameter	20.7	21.0	7.3	15.3	6.8	.3.5	
ψ_{JB}	Junction-to-board characterization parameter	48.9	51.2	62.8	49.8	63.8	33.7	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	—	—	14.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V$_{CC}$	T$_A$ = 25°C			−40°C to 85°C		−40°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V$_{OH}$	I$_{OH}$ = −50 µA	2 V to 5.5 V	V$_{CC}$ − 0.1			V$_{CC}$ − 0.1		V$_{CC}$ − 0.1		V
	I$_{OH}$ = −2 mA	2.3 V	2			2		2		
	I$_{OH}$ = −6 mA	3 V	2.48			2.48		2.48		
	I$_{OH}$ = −12 mA	4.5 V	3.8			3.8		3.8		
V$_{OL}$	I$_{OL}$ = 50 µA	2 V to 5.5 V			0.1		0.1		0.1	V
	I$_{OL}$ = 2 mA	2.3 V			0.4		0.4		0.4	
	I$_{OL}$ = 6 mA	3 V			0.44		0.44		0.44	
	I$_{OL}$ = 12 mA	4.5 V			0.55		0.55		0.55	
I$_I$	V$_I$ = 5.5 V or GND	0 to 5.5 V			±1		±1		±1	µA
I$_{CC}$	V$_I$ = V$_{CC}$ or GND, I$_O$ = 0	5.5 V			20		20		20	µA
I$_{off}$	V$_I$ or V$_O$ = 0 to 5.5 V	0			5		5		5	µA
C$_i$	V$_I$ = V$_{CC}$ or GND	3.3 V		2.3						pF
		5 V		2.3						

7.6 Switching Characteristics, V$_{CC}$ = 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T$_A$ = 25°C			−40°C to 85°C		−40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t$_{pd}$	A	Y	C$_L$ = 15 pF		7.1[1]	11.7[1]	1	14	1	15	ns
			C$_L$ = 50 pF		10	15.5	1	18	1	19	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

7.7 Switching Characteristics, V$_{CC}$ = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T$_A$ = 25°C			−40°C to 85°C		−40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t$_{pd}$	A	Y	C$_L$ = 15 pF		5.1[1]	7.1[1]	1	8.5	1	9.5	ns
			C$_L$ = 50 pF		7.3	10.6	1	12	1	13	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

7.8 Switching Characteristics, V$_{CC}$ = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T$_A$ = 25°C			−40°C to 85°C		−40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t$_{pd}$	A	Y	C$_L$ = 15 pF		3.6[1]	5.5[1]	1	6.5	1	7.5	ns
			C$_L$ = 50 pF		5.1	7.5	1	8.5	1	9.5	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

Product Folder Links: *SN74LV04A*

7.9 Noise Characteristics[1]

V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C

PARAMETER		SN74LV04A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.3	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.1	−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		3.1		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

(1) Characteristics are for surface-mount packages only.

7.10 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF,	f = 10 MHz	3.3 V	9.6	pF
				5 V	11.4	

7.11 Typical Characteristics
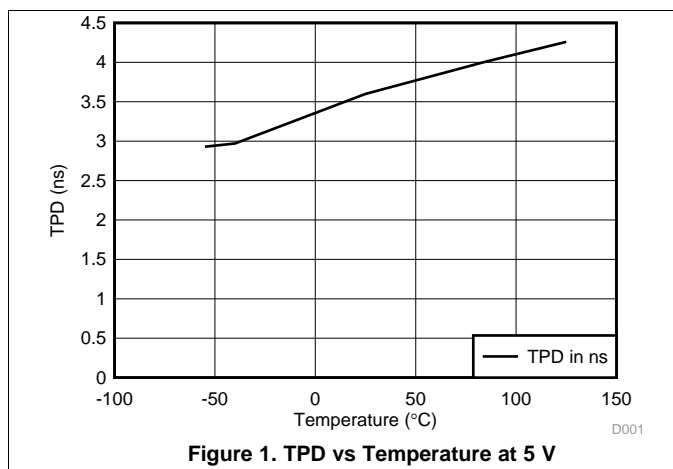
Figure 1. TPD vs Temperature at 5 V
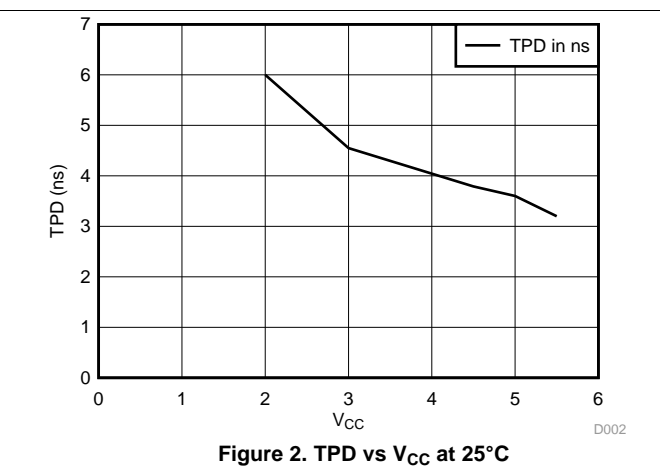
Figure 2. TPD vs V_{CC} at 25°C

8 Parameter Measurement Information

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS

VOLTAGE WAVEFORMS PULSE DURATION

VOLTAGE WAVEFORMS SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
  B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
  D. The outputs are measured one at a time, with one input transition per measurement.
  E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
  F. t_{PZL} and t_{PZH} are the same as t_{en}.
  G. t_{PHL} and t_{PLH} are the same as t_{pd}.
  H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

Product Folder Links: *SN74LV04A*

9 Detailed Description

9.1 Overview

These hex inverters are designed for 2-V to 5.5-V V_{CC} operation. The SN74LV04A devices contain six independent inverters. These devices perform the Boolean function $Y = \overline{A}$.

These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

The inputs are high impedance when $V_{CC} = 0V$.

9.2 Functional Block Diagram
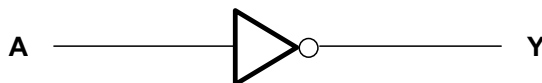
Figure 4. Logic Diagram Each Inverter (Positive Logic)

9.3 Feature Description

- Wide operating voltage range
  - Operates from 2 V to 5.5 V
- Allows down-voltage translation
  - Inputs accept voltages to 5.5 V
- I_{off} feature
  - Supports Live Insertion, Partial Power DownMode, and Back Drive Protection

9.4 Device Functional Modes

Table 1. Function Table
(Each Inverter)

INPUT A	OUTPUT Y
H	L
L	H

Product Folder Links: *SN74LV04A*

10 Application and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

SN74LV04A is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize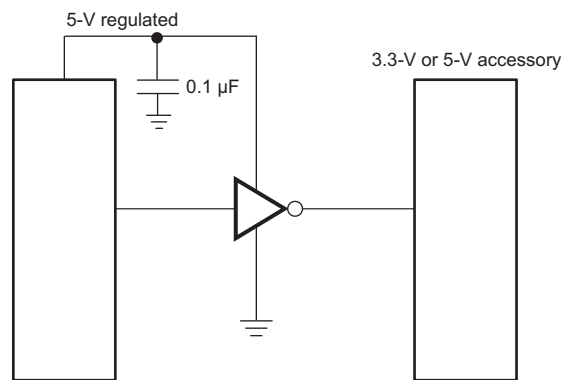 overshoot and undershoot on the outputs. The inputs can accept voltages to 5.5 V at any valid V_{CC} making it Ideal for down translation.

10.2 Typical Application

Figure 5. Typical Application Schematic

10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

10.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - For rise time and fall time specifications, see Δt/ΔV in the *Recommended Operating Conditions* table.
   - For specified High and low levels, see V_{IH} and V_{IL} in the *Recommended Operating Conditions* table.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
2. Recommend Output Conditions
   - Load currents should not exceed 25 mA per output and 50 mA total for the part.
   - Outputs should not be pulled above V_{CC}.

Product Folder Links: *SN74LV04A*

Typical Application (continued)

10.2.3 Application Curves
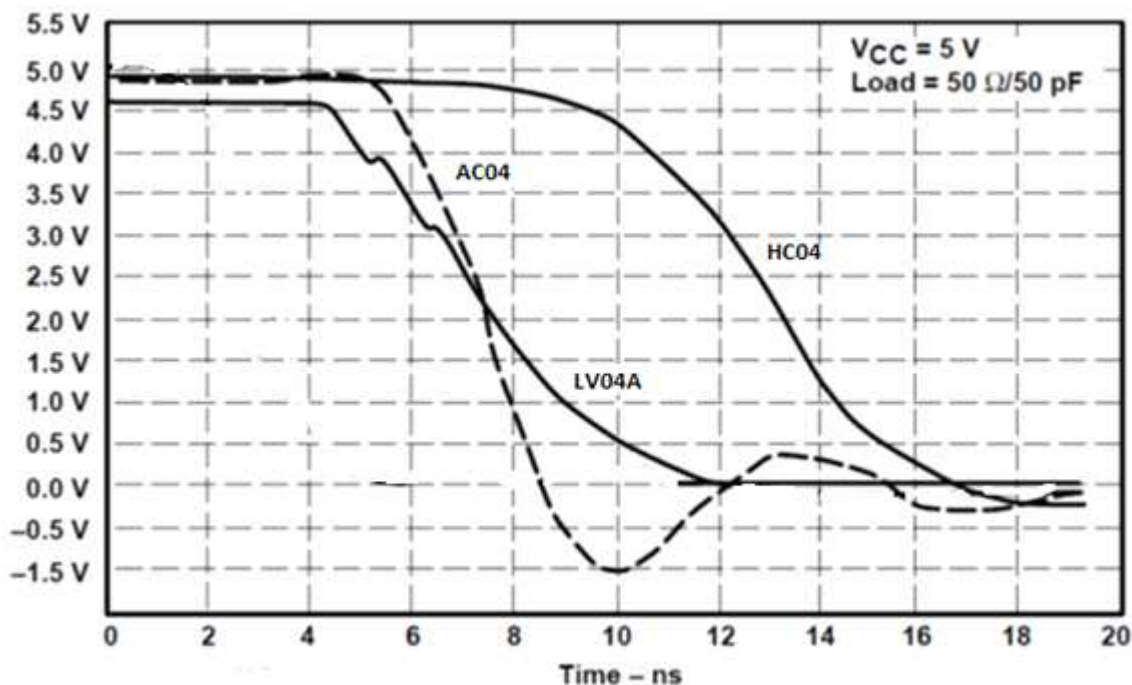
Figure 6. Typical Application Curve

11 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µF is recommended. If there are multiple V_{CC} pins, 0.01 µF or 0.022 µF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

12 Layout

12.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 7 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

12.2 Layout Example
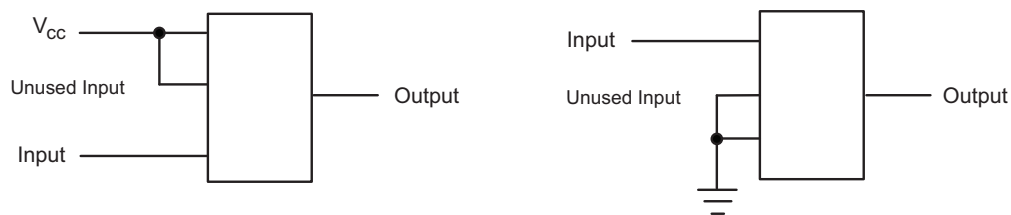
Figure 7. Layout Diagram

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74LV04A	Click here	Click here	Click here	Click here	Click here

13.2 Trademarks

All trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12   *Submit Documentation Feedback*

Product Folder Links: *SN74LV04A*

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV04ADBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV04A	Samples
SN74LV04ADGVR	ACTIVE	TVSOP	DGV	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV04A	Samples
SN74LV04ADGVRE4	ACTIVE	TVSOP	DGV	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV04A	Samples
SN74LV04ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LV04A	Samples
SN74LV04ANSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV04A	Samples
SN74LV04APWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LV04A	Samples
SN74LV04APWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV04A	Samples
SN74LV04ARGYR	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LV04A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LV04A :

● Enhanced Product : SN74LV04A-EP

NOTE: Qualified Version Definitions:

● Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV04ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LV04ADGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV04ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV04ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV04ADR	SOIC	D	14	2500	330.0	16.4	6.6	9.3	2.1	8.0	16.0	Q1
SN74LV04ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LV04APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV04APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV04APWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV04APWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV04ARGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV04ADBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74LV04ADGVR	TVSOP	DGV	14	2000	356.0	356.0	35.0
SN74LV04ADR	SOIC	D	14	2500	356.0	356.0	35.0
SN74LV04ADR	SOIC	D	14	2500	353.0	353.0	32.0
SN74LV04ADR	SOIC	D	14	2500	366.0	364.0	50.0
SN74LV04ANSR	SO	NS	14	2000	367.0	367.0	38.0
SN74LV04APWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LV04APWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74LV04APWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LV04APWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LV04ARGYR	VQFN	RGY	14	3000	356.0	356.0	35.0

RGY (S−PVQFN−N14)   PLASTIC QUAD FLATPACK NO−LEAD

$\frac{3,65}{3,35}$ A

B

13   9

14   8

$\frac{3,65}{3,35}$

1   7

2   6

Pin 1 Index Area
Top and Bottom

F

$\frac{1,00}{0,80}$

0,20 Nominal
Lead Frame

Seating Plane

⌓ 0,08 C

$\frac{0,05}{0,00}$
Seating Height

C

2,00

0,50

14X $\frac{0,50}{0,30}$

2   6

1   7
THERMAL PAD

1,50   SIZE AND SHAPE
SHOWN ON SEPRATE SHEET

14   8

13   9

14X $\frac{0,30}{0,18}$

⊕ | 0,10 Ⓜ C A B
  | 0,05 Ⓜ C

Bottom View

4203539−2/I   06/2011

NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   QFN (Quad Flatpack No−Lead) package configuration.
         D.   The package thermal pad must be soldered to the board for thermal and mechanical performance.
         E.   See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
    F.   Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated.
         The Pin 1 identifiers are either a molded, marked, or metal feature.
         G.   Package complies to JEDEC MO−241 variation BA.

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RGY (S−PVQFN−N14)   PLASTIC QUAD FLATPACK NO−LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

Exposed Thermal Pad

2,05±0,10

2,05±0,10

Bottom View

Exposed Thermal Pad Dimensions

4206353−2/P   03/14

NOTE: All linear dimensions are in millimeters

RGY (S-PVQFN-N14)   PLASTIC QUAD FLATPACK NO-LEAD

Example Board Layout

4,30

4,30
2,60
1,50
2,05
2,05

Note D

8x0,50   0.28

Example Stencil Design
0.125mm Stencil Thickness
(Note E)

4,25

4,25
2,65
1,50

0,82 SQ
0,50

0,80 x 14 PL.

8x0,50   0,23 x 14 PL.

64% solder coverage by printed
area on center thermal pad

Non Solder Mask
Defined Pad

Example
Solder Mask Opening
(Note F)

0,08
R0,14
0,85

0,07
0,28

All Around

Example
Pad Geometry
(Note C)

Example Via Layout Design
may vary depending on constraints
(Note D, F)

1,00

1,00

6xØ0,3

4208122-2/P   03/14

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack
QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets
for specific thermal information, via requirements, and recommended board layout.
These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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NS (R-PDSO-G)**   PLASTIC SMALL-OUTLINE PACKAGE
14-PINS SHOWN

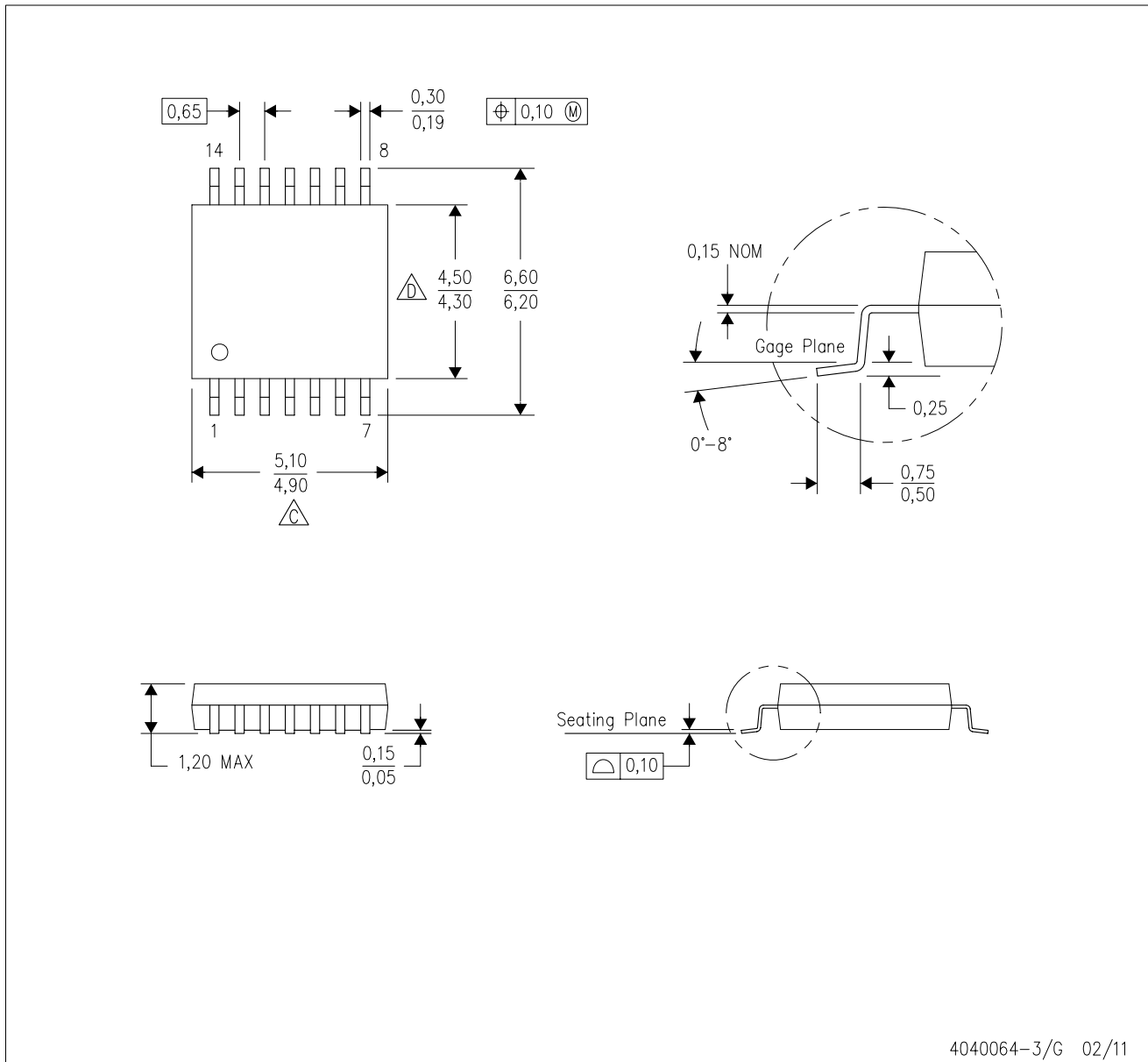| DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

PINS ** DIM	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
                    14/16/20/56 Pins – MO-194

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D (R−PDSO−G14)   PLASTIC SMALL OUTLINE

0.344 (8,75)
0.337 (8,55)
C

14   8

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)   D

1   7

Pin 1
Index Area

0.050 (1,27)   0.020 (0,51)
                      0.012 (0,31)

⊕ 0.010 (0,25) M

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−5/M   06/11

NOTES: A. All linear dimensions are in inches (millimeters).
          B. This drawing is subject to change without notice.
          C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
              not exceed 0.006 (0,15) each side.
          D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
          E. Reference JEDEC MS−012 variation AB.

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PW (R−PDSO−G14)   PLASTIC SMALL OUTLINE

0,65   0,30 / 0,19   ⊕ 0,10 Ⓜ

14   8

D   4,50 / 4,30   6,60 / 6,20

1   7

5,10 / 4,90
Ⓒ

0,15 NOM

Gage Plane

0°−8°   0,25

0,75 / 0,50

1,20 MAX   0,15 / 0,05

Seating Plane   0,10

4040064−3/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B. This drawing is subject to change without notice.
         Ⓒ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
             not exceed 0,15 each side.
         Ⓓ Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
         E. Falls within JEDEC MO−153

DB (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

	PINS **	14	16	20	24	28	30	38
DIM								
A MAX		6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN		5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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