

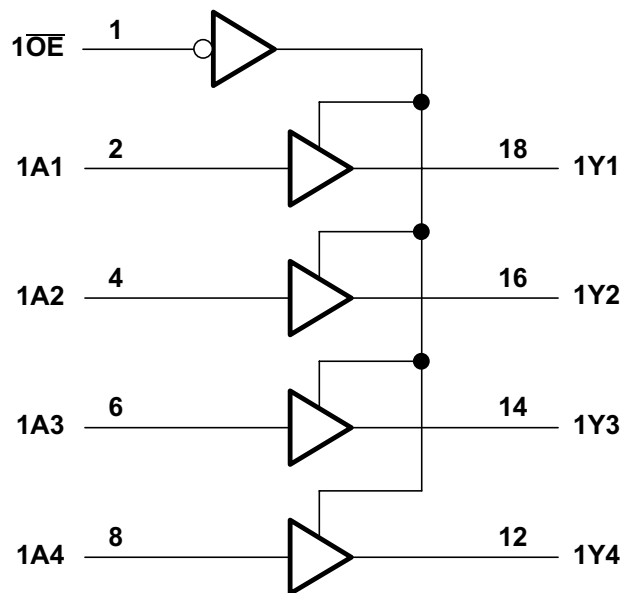
# SN74LV244B-EP Enhanced Product, 2-V to 5.5-V, Low-Noise, Octal Drivers With 3-State Outputs

## 1 Features

- 2 V to 5.5 V  $V_{CC}$  operation
- Supports mixed-mode voltage operation on all ports
- $I_{off}$  supports partial-power-down mode operation
- Latch-up performance exceeds 250 mA per JESD 17
- Operating ambient temperature:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Supports defense, aerospace, and medical applications:
  - Controlled baseline
  - One assembly and test site
  - One fabrication site
  - Extended product life cycle
  - Product traceability

## 2 Applications

- [Enable or disable a digital signal](#)
- [Eliminate slow or noisy input signals](#)
- [Hold a signal during controller reset](#)
- [Debounce a switch](#)



## 3 Description

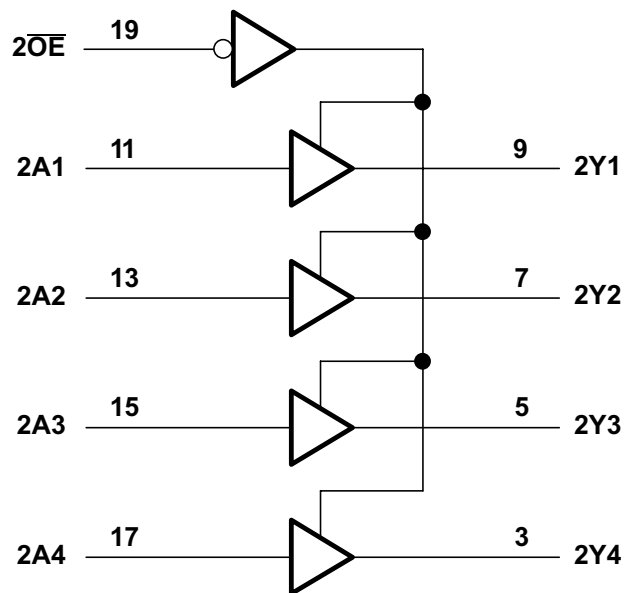
The SN74LV244B-EP octal buffers and line drivers are designed for 2 V to 5.5 V  $V_{CC}$  operation.

The device is configured into two banks of four drivers, each controlled by its own output enable pin. This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
SN74LV244B-EP	DW (SOIC, 20)	12.8 mm × 10.3 mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.



Logic Diagram (Positive Logic)



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## 4 Revision History

DATE	REVISION	NOTES
August 2023	*	Initial Release

## 5 Pin Configuration and Functions

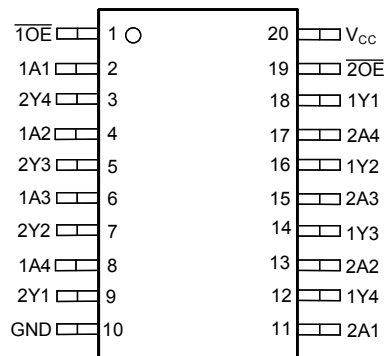


Figure 5-1. SN74LV244B-EP: DW Package, 20-Pin SOIC (Top View)

Table 5-1. Pin Functions

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
1OE	1	I	Bank 1, output enable, active low
1A1	2	I	Bank 1, channel 1 input
2Y4	3	O	Bank 2, channel 4 output
1A2	4	I	Bank 1, channel 2 input
2Y3	5	O	Bank 2, channel 3 output
1A3	6	I	Bank 1, channel 3 input
2Y2	7	O	Bank 2, channel 2 output
1A4	8	I	Bank 1, channel 4 input
2Y1	9	O	Bank 2, channel 1 output
GND	10	G	Ground
2A1	11	I	Bank 2, channel 1 input
1Y4	12	O	Bank 1, channel 4 output
2A2	13	I	Bank 2, channel 2 input
1Y3	14	O	Bank 1, channel 3 output
2A3	15	I	Bank 2, channel 3 input
1Y2	16	O	Bank 1, channel 2 output
2A4	17	I	Bank 2, channel 4 input
1Y1	18	O	Bank 1, channel 1 output
2OE	19	I	Bank 2, output enable, active low
V <sub>CC</sub>	20	P	Positive supply

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	-0.5	7	V
V <sub>I</sub>	Input voltage <sup>(2)</sup>	-0.5	7	V
V <sub>O</sub>	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	7	V
V <sub>O</sub>	Output voltage <sup>(2)</sup> <sup>(3)</sup>	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0	-20	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0	-50	mA
I <sub>O</sub>	Continuous output current	V <sub>O</sub> = 0 to V <sub>CC</sub>	±35	mA
	Continuous current through V <sub>CC</sub> or GND		±70	mA
T <sub>stg</sub>	Storage temperature	-65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 5.5 V maximum.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup>	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5	V
		V <sub>CC</sub> = 2.3 V to 5.5 V	V <sub>CC</sub> × 0.7	
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V	0.5	V
		V <sub>CC</sub> = 2.3 V to 5.5 V	V <sub>CC</sub> × 0.3	
V <sub>I</sub>	Input voltage	0	5.5	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2 V	–50	μA
		V <sub>CC</sub> = 2.3 V to 2.7 V	–2	
		V <sub>CC</sub> = 3 V to 3.6 V	–6	
		V <sub>CC</sub> = 4.5 V to 5.5 V	–12	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2 V	50	μA
		V <sub>CC</sub> = 2.3 V to 2.7 V	2	
		V <sub>CC</sub> = 3 V to 3.6 V	6	
		V <sub>CC</sub> = 4.5 V to 5.5 V	12	
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 2.3 V to 2.7 V	200	ns/V
		V <sub>CC</sub> = 3 V to 3.6 V	100	
		V <sub>CC</sub> = 4.5 V to 5.5 V	20	
T <sub>A</sub>	Operating free-air temperature	–55	125	°C

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND for proper device operation. See [Implications of Slow or Floating CMOS Inputs](#).

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74LV244B-EP	
		DW (SOIC)	
		20 PINS	
			UNIT
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	102.3	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	69.6	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	70.8	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	46.4	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	70.4	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).

## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted).

PARAMETER		V <sub>CC</sub>	MIN	TYP	MAX	UNIT
V <sub>OH</sub>	I <sub>OH</sub> = –50 mA	2 V to 5.5 V	V <sub>CC</sub> – 0.1			V
	I <sub>OH</sub> = –2 mA	2.3 V	2			
	I <sub>OH</sub> = –6 mA	3 V	2.48			
	I <sub>OH</sub> = –12 mA	4.5 V	3.8			
V <sub>OL</sub>	I <sub>OL</sub> = 50 mA	2 V to 5.5 V	0.1			V
	I <sub>OL</sub> = 2 mA	2.3 V	0.4			
	I <sub>OL</sub> = 6 mA	3 V	0.44			
	I <sub>OL</sub> = 12 mA	4.5 V	0.55			
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V	±1			μA
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V	±5			μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V	20			μA
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V	0 V	5			μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	2.3			pF

## 6.6 Switching Characteristics, V<sub>CC</sub> = 2.5 V ± 0.2 V

over operating free-air temperature range (unless otherwise noted), (see [Figure 7-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAP	25°C			–55°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t <sub>pd</sub>	A	Y	C <sub>L</sub> = 15 pF		7.5	12.5	1		15	ns
t <sub>en</sub>	$\overline{OE}$	Y	C <sub>L</sub> = 15 pF		8.9	14.6	1		17	ns
t <sub>dis</sub>	$\overline{OE}$	Y	C <sub>L</sub> = 15 pF		9.1	14.1	1		16	ns
t <sub>pd</sub>	A	Y	C <sub>L</sub> = 50 pF		9.5	15.3	1		18	ns
t <sub>en</sub>	$\overline{OE}$	Y	C <sub>L</sub> = 50 pF		10.8	17.8	1		21	ns
t <sub>dis</sub>	$\overline{OE}$	Y	C <sub>L</sub> = 50 pF		13.4	19.2	1		21	ns
t <sub>sk(o)</sub>			C <sub>L</sub> = 50 pF			2			2	ns

## 6.7 Switching Characteristics, V<sub>CC</sub> = 3.3 V ± 0.3 V

over operating free-air temperature range (unless otherwise noted), (see [Figure 7-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAP	25°C			–55°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t <sub>pd</sub>	A	Y	C <sub>L</sub> = 15 pF		5.4	8.4	1		10	ns
t <sub>en</sub>	$\overline{OE}$	Y	C <sub>L</sub> = 15 pF		6.3	10.6	1		12.5	ns
t <sub>dis</sub>	$\overline{OE}$	Y	C <sub>L</sub> = 15 pF		7.6	11.7	1		13	ns
t <sub>pd</sub>	A	Y	C <sub>L</sub> = 50 pF		6.8	11.9	1		13.5	ns
t <sub>en</sub>	$\overline{OE}$	Y	C <sub>L</sub> = 50 pF		7.8	14.1	1		16	ns
t <sub>dis</sub>	$\overline{OE}$	Y	C <sub>L</sub> = 50 pF		11	16	1		18	ns
t <sub>sk(o)</sub>			C <sub>L</sub> = 50 pF			1.5			1.5	ns

## 6.8 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted), (see [Figure 7-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAP	25°C			-55°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
$t_{pd}$	A	Y	$C_L = 15\text{ pF}$		3.9	5.5	1		6.5	ns
$t_{en}$	$\overline{OE}$	Y	$C_L = 15\text{ pF}$		4.5	7.3	1		8.5	ns
$t_{dis}$	$\overline{OE}$	Y	$C_L = 15\text{ pF}$		6.5	12.2	1		13.5	ns
$t_{pd}$	A	Y	$C_L = 50\text{ pF}$		4.9	7.5	1		8.5	ns
$t_{en}$	OE	Y	$C_L = 50\text{ pF}$		5.6	9.3	1		10.5	ns
$t_{dis}$	$\overline{OE}$	Y	$C_L = 50\text{ pF}$		8.8	14.2	1		15.5	ns
$t_{sk(o)}$			$C_L = 50\text{ pF}$			1			1	ns

## 6.9 Noise Characteristics

$V_{CC} = 3.3\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$ <sup>(1)</sup>

		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic		0.55		V
$V_{OL(V)}$	Quiet output, minimum dynamic		-0.5		V
$V_{OH(V)}$	Quiet output, minimum dynamic		2.9		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

(1) Characteristics are for surface-mount packages only.

## 6.10 Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	$V_{CC}$	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	$C_L = 50\text{ pF}$ $f = 10\text{ MHz}$	3.3 V	14	pF
		5 V	16	

## 6.11 Typical Characteristics

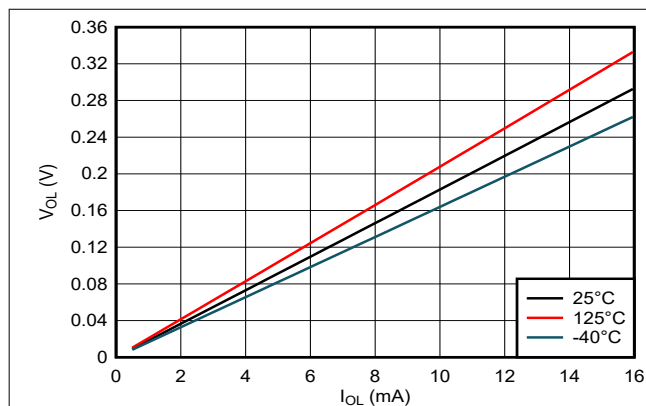


Figure 6-1. Output Voltage vs Current in LOW State; 5-V Supply

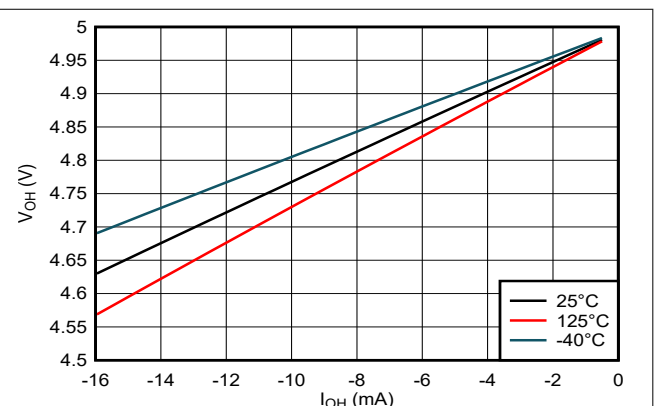
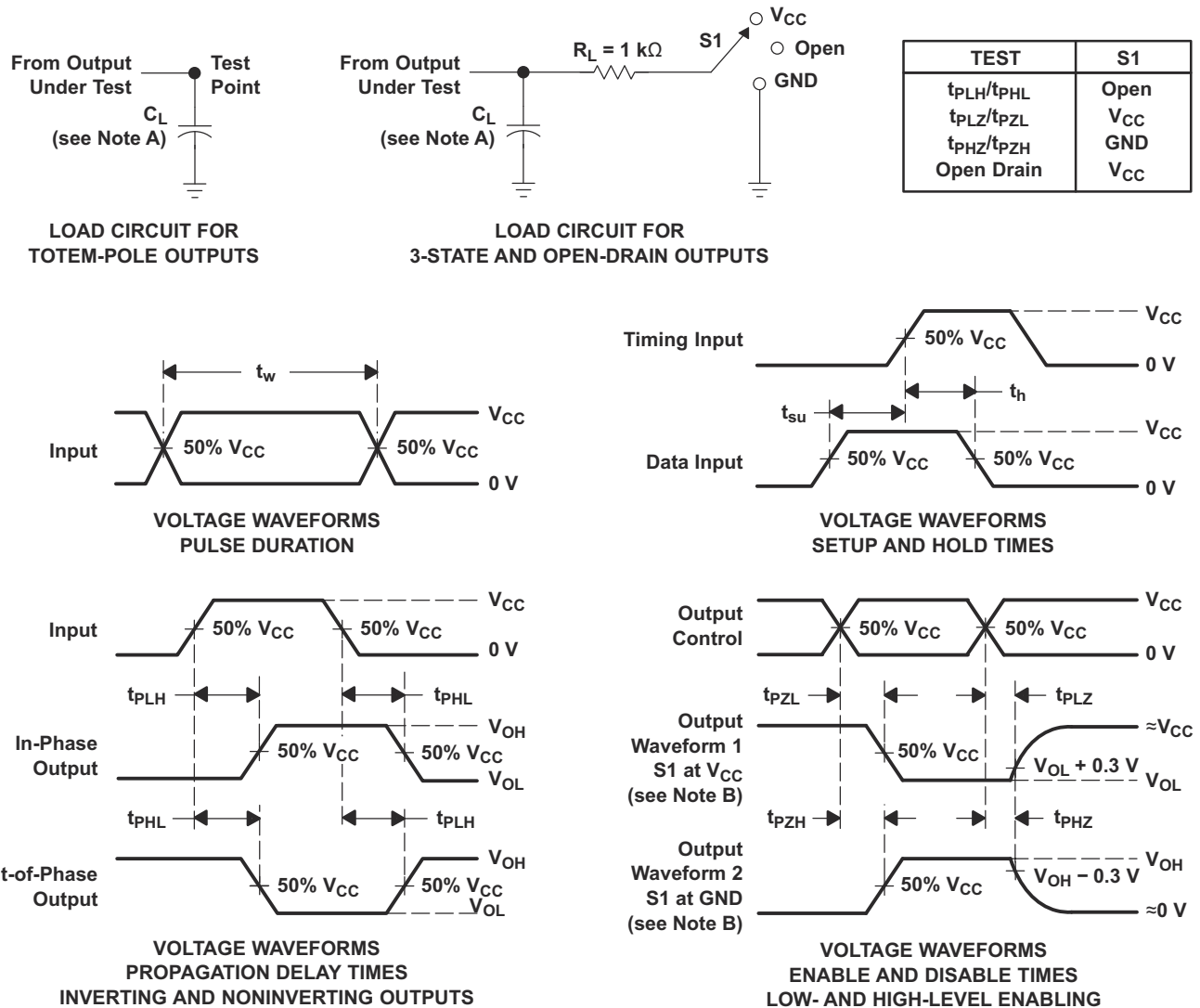


Figure 6-2. Output Voltage vs Current in HIGH State; 5-V Supply

## 7 Parameter Measurement Information



- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 3 \text{ ns}$ , and  $t_f \leq 3 \text{ ns}$ .
- D. The outputs are measured one at a time, with one input transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

**Figure 7-1. Load Circuit and Voltage Waveforms**



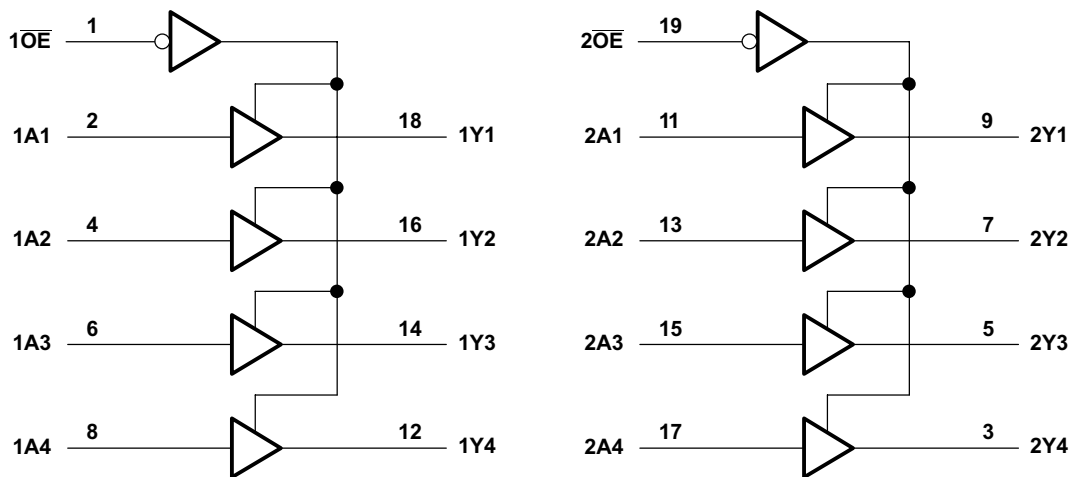
## 8 Detailed Description

### 8.1 Overview

The SN74LV244B-EP octal buffers and line drivers are designed for 2 V to 5.5 V  $V_{CC}$  operation.

The device is configured into two banks of four drivers, each controlled by its own output enable pin. This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law ( $R = V \div I$ ).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in [Implications of Slow or Floating CMOS Inputs](#).

Do not leave standard CMOS inputs floating at any time during operation. Unused inputs must be terminated at  $V_{CC}$  or GND. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; a 10-k $\Omega$  resistor, however, is recommended and will typically meet all requirements.

#### 8.3.2 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs. Driving high, driving low, and high impedance are the three states that these outputs can be in. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device can drive larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance mode, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10-kΩ resistor can be used to meet these requirements.

Unused 3-state CMOS outputs should be left disconnected.

### 8.3.3 Partial Power Down ( $I_{off}$ )

This device includes circuitry to disable all outputs when the supply pin is held at 0 V. When disabled, the outputs will neither source nor sink current, regardless of the input voltages applied. The amount of leakage current at each output is defined by the  $I_{off}$  specification in the *Electrical Characteristics* table.

### 8.3.4 Clamp Diode Structure

Figure 8-1 shows the inputs and outputs to this device have negative clamping diodes only.

**CAUTION**

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

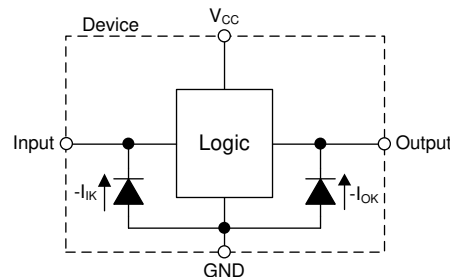


Figure 8-1. Electrical Placement of Clamping Diodes for Each Input and Output

## 8.4 Device Functional Modes

Table 8-1 list the functional modes of the SN74LV244B-EP.

Table 8-1. Function Table

INPUTS <sup>(1)</sup>		OUTPUTS
$\overline{OE}$	A	Y
L	L	L
L	H	H
H	X	Z

(1) H = High Voltage Level, L = Low Voltage Level, X = Do Not Care, Z = High-Impedance State

## 9 Application and Implementation

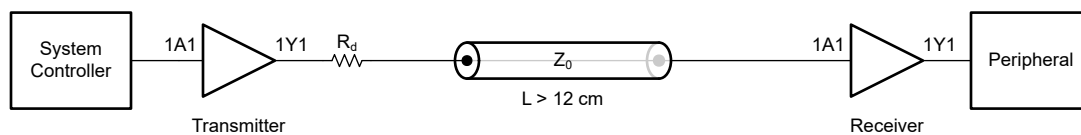
### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

The SN74LV244B-EP can be used to drive signals over relatively long traces or transmission lines. To reduce ringing caused by impedance mismatches between the driver, transmission line, and receiver, a series damping resistor placed in series with the transmitter's output can be used. The plot in the *Application Curve* section shows the received signal with three separate resistor values. Just a small amount of resistance can make a significant impact on signal integrity in this type of application.

### 9.2 Typical Application



**Figure 9-1. Typical Application Block Diagram**

#### 9.2.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74LV244B-EP plus the maximum static supply current,  $I_{CC}$ , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Be sure to not exceed the maximum total current through  $V_{CC}$  listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LV244B-EP plus the maximum supply current,  $I_{CC}$ , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Be sure to not exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74LV244B-EP can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50 pF.

The SN74LV244B-EP can drive a load with total resistance described by  $R_L \geq V_O / I_O$ , with the output voltage and current defined in the *Electrical Characteristics* table with  $V_{OH}$  and  $V_{OL}$ . When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the  $V_{CC}$  pin.

Total power consumption can be calculated using the information provided in [CMOS Power Consumption and Cpd Calculation](#).

Thermal increase can be calculated using the information provided in [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#).

### CAUTION

The maximum junction temperature,  $T_{J(max)}$  listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

## 9.2.2 Input Considerations

Input signals must cross  $V_{IL(max)}$  to be considered a logic LOW, and  $V_{IH(min)}$  to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either  $V_{CC}$  or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LV244B-EP (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10-k $\Omega$  resistor value is often used due to these factors.

The SN74LV244B-EP has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

## 9.2.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the  $V_{OH}$  specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the  $V_{OL}$  specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

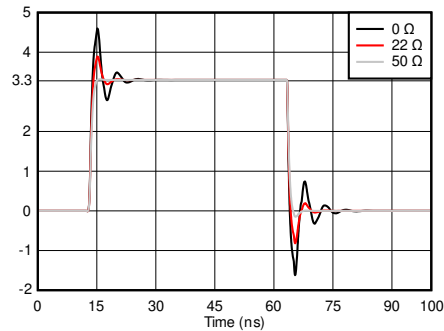
Unused outputs can be left floating. Do not connect outputs directly to  $V_{CC}$  or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

## 9.2.4 Detailed Design Procedure

1. Add a decoupling capacitor from  $V_{CC}$  to GND. The capacitor needs to be placed physically close to the device and electrically close to both the  $V_{CC}$  and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is  $\leq 50$  pF. This is not a hard limit; it will, however, optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74LV244B-EP to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than  $(V_{CC} / I_{O(max)}) \Omega$ , which will not violate the maximum output current from the *Absolute Maximum Ratings*. Most CMOS inputs have a resistive load measured in M $\Omega$ ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#).

## 9.2.5 Application Curves



**Figure 9-2. Simulated Signal Integrity at the Receiver With Different Damping Resistor ( $R_d$ ) Values**

## 9.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Absolute Maximum Ratings* section. Each  $V_{CC}$  terminal must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1- $\mu\text{F}$  capacitor; if there are multiple  $V_{CC}$  terminals, then TI recommends a 0.01- $\mu\text{F}$  or 0.022- $\mu\text{F}$  capacitor for each power terminal. Multiple bypass capacitors can be paralleled to reject different frequencies of noise. Frequencies of 0.1  $\mu\text{F}$  and 1  $\mu\text{F}$  are commonly used in parallel. The bypass capacitor must be installed as close as possible to the power terminal for best results.

## 9.4 Layout

### 9.4.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

### 9.4.2 Layout Example

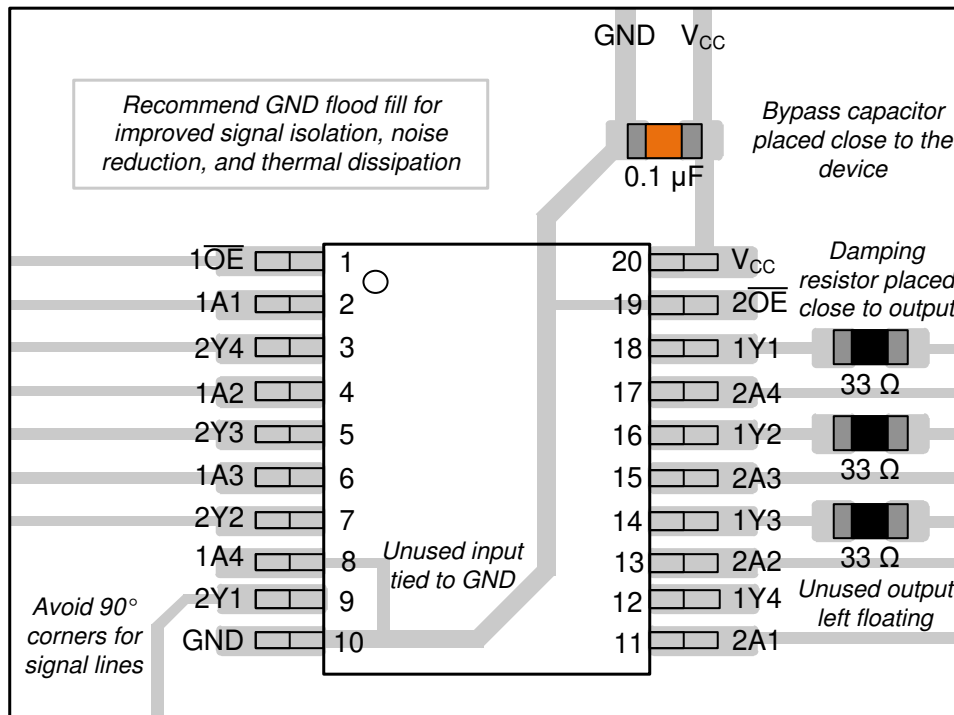


Figure 9-3. Layout Example for the SN74LV244B-EP in the PW Package

## 10 Device and Documentation Support

### 10.1 Documentation Support

#### 10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [CMOS Power Consumption and Cpd Calculation](#)
- Texas Instruments, [Introduction to Logic](#)
- Texas Instruments, [Power-Up Behavior of Clocked Devices](#)
- Texas Instruments, [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#)

#### 10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on [ti.com](#). In the upper right-hand corner, click the *Alert me* button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

#### 10.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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#### 10.4 Trademarks

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#### 10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV244BMDWREP	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LV244BMEP	<a href="#">Samples</a>
V62/23625-01XE	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		LV244BMEP	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

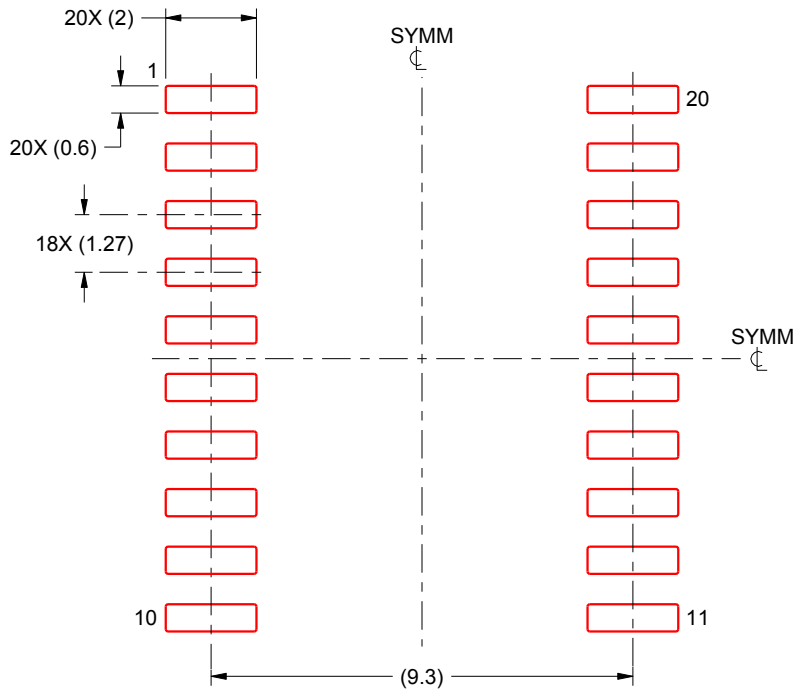
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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