

SN74LV373A Octal Transparent D-Type Latches With 3-State Outputs

1 Features

- V_{CC} operation of 2 V to 5.5 V
- Maximum t_{pd} of 8.5 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2.3 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Voltage Operation on All Ports
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17

2 Applications

- Printers
- Network Switches
- Tests and Measurements
- Wireless Infrastructure
- Motor Controls
- Server Motherboards

3 Description

The SN74LV373A device is an octal transparent D-type latch designed for 2 V to 5.5 V V_{CC} operation.

Package Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LV373A	VQFN (20)	4.50 x 3.50 mm
	SSOP (20)	7.50 x 5.30 mm
	TSSOP (20)	6.50 x 4.40 mm
	TVSOP (20)	5.00 x 4.40 mm
	SOIC (20)	12.80 x 7.50 mm
	SO (20)	12.60 mm x 5.30 mm

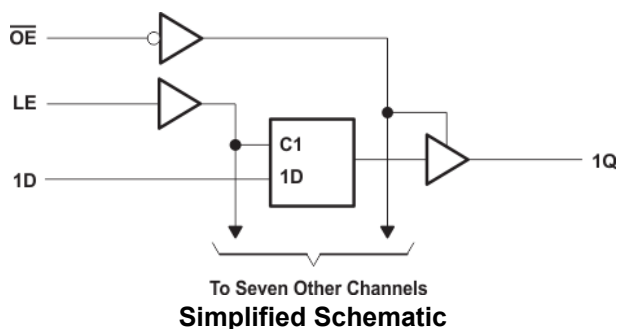


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4 Pin Configuration and Functions

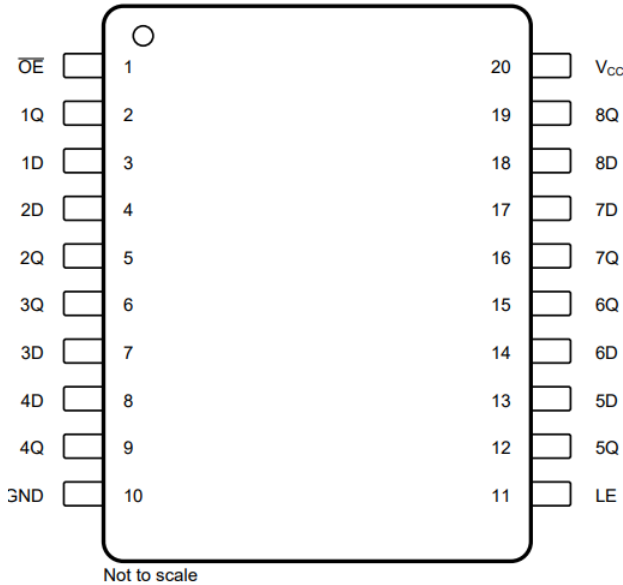


Figure 4-1. DB, DGV, DW, NS, or PW 20-Pin SSOP, TVSOP, SOIC, SO, or TSSOP Top View

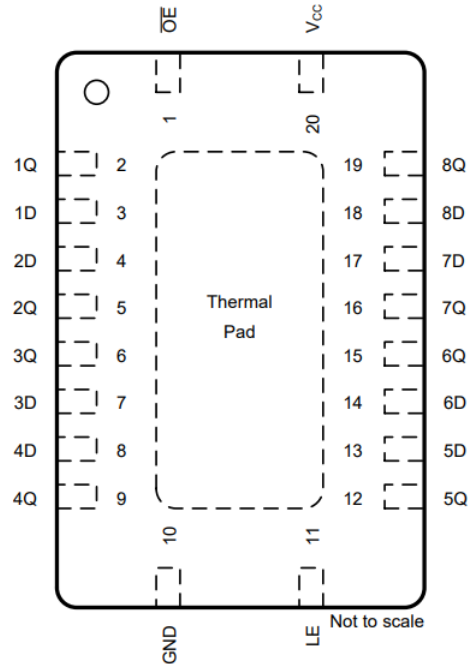


Figure 4-2. RGY Package 20-Pin VQFN Top View

Table 4-1. Pin Functions

NO.	PIN		TYPE	DESCRIPTION
	SSOP, TVSOP, SOIC, SO, or TSSOP	VQFN		
1	\overline{OE}	\overline{OE}	I	Output Enable
2	1Q	1Q	O	1Q Output
3	1D	1D	I	1D Input
4	2D	2D	I	2D Input
5	2Q	2Q	O	2Q Output
6	3Q	3Q	O	3Q Output
7	3D	3D	I	3D Input
8	4D	4D	I	4D Input
9	4Q	4Q	O	4Q Output
10	GND	GND	—	Ground Pin
11	LE	LE	I	Latch Enable
12	5Q	5Q	O	5Q Output
13	5D	5D	I	5D Input
14	6D	6D	I	6D Input
15	6Q	6Q	O	6Q Output
16	7Q	7Q	O	7Q Output
17	7D	7D	I	7D Input
18	8D	8D	I	8D Input
19	8Q	8Q	O	8Q Output
20	V _{CC}	V _{CC}	—	Power Pin
—	—	Thermal Pad	—	Thermal Pad, normally tied to GND

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	-0.5	7	V
V _I	Input voltage ⁽²⁾	-0.5	7	V
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	7	V
V _O	Output voltage ⁽²⁾ (3)	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0	-20	mA
I _{OK}	Output clamp current	V _O < 0	-50	mA
I _O	Continuous output current	V _O = 0 to V _{CC}	±35	mA
	Continuous channel current through V _{CC} or GND		±70	mA
T _{stg}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [Section 5.3](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 5.5-V maximum.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±3000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±2000	
		Machine Model (MM)	±200	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT	
V _{CC}	Supply voltage	2	5.5	V	
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5	V	
		V _{CC} = 2.3 V ± 2.7 V	V _{CC} × 0.7		
		V _{CC} = 3 V ± 3.6 V	V _{CC} × 0.7		
		V _{CC} = 4.5 V ± 5.5 V	V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5	V	
		V _{CC} = 2.3 V ± 2.7 V	V _{CC} × 0.3		
		V _{CC} = 3 V ± 3.6 V	V _{CC} × 0.3		
		V _{CC} = 4.5 V ± 5.5 V	V _{CC} × 0.3		
V _I	Input voltage	0	5.5	V	
V _O	Output voltage	High or low state	0	V _{CC}	V
		3-state	0	5.5	
I _{OH}	High-level output current	V _{CC} = 2 V	-50	μA	
		V _{CC} = 2.3 V ± 2.7 V	-2		
		V _{CC} = 3 V ± 3.6 V	-8	mA	
		V _{CC} = 4.5 V ± 5.5 V	-16		
I _{OL}	Low-level output current	V _{CC} = 2 V	50	μA	
		V _{CC} = 2.3 V ± 2.7 V	2		
		V _{CC} = 3 V ± 3.6 V	8	mA	
		V _{CC} = 4.5 V ± 5.5 V	16		
Δt/Δv	Input transition rise or fall	V _{CC} = 2.3 V ± 2.7 V	200	ns/V	
		V _{CC} = 3 V ± 3.6 V	100		
		V _{CC} = 4.5 V ± 5.5 V	20		
T _A	Operating free-air temperature	-40	125	°C	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs (SCBA004)*.

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74LV373A						UNIT
		DB (SSOP)	DGV (TVSOP)	DW (SOIC)	NS (SO)	PW (TSSOP)	RGY (VQFN)	
		20 PINS						
R _{θJA}	Junction-to-ambient thermal resistance	94.5	116.2	79.2	76.7	128.2	34.8	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	56.4	31.2	43.7	43.2	70.5	42.9	°C/W
R _{θJB}	Junction-to-board thermal resistance	49.7	57.7	47.0	44.2	79.3	12.4	°C/W
ψ _{JT}	Junction-to-top characterization parameter	18.5	0.9	18.6	16.8	23.4	0.8	°C/W
ψ _{JB}	Junction-to-board characterization parameter	49.3	57.0	46.5	43.8	78.9	12.5	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	—	—	—	—	—	7.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			–40°C to +85°C		–40°C to +125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = –50 μA	2 V to 5.5 V	V _{CC} – 0.1			V _{CC} – 0.1		V _{CC} – 0.1		V
	I _{OH} = –2 mA	2.3 V	2			2		2		
	I _{OH} = –8 mA	3 V	2.48			2.48		2.48		
	I _{OH} = –16 mA	4.5 V	3.8			3.8		3.8		
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V				0.1		0.1		V
	I _{OL} = 2 mA	2.3 V				0.4		0.4		
	I _{OL} = 8 mA	3 V				0.44		0.44		
	I _{OL} = 16 mA	4.5 V				0.55		0.55		
I _I	V _I = 5.5 V or GND	0 V to 5.5 V				±1		±1		μA
I _{OZ}	V _I = V _{CC} or GND	5.5 V				±5		±5		μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V				20		20		μA
I _{off}	V _I or V _O = 0 to V _{CC}	0				5		5		μA
C _i	V _I = V _{CC} or GND	3.3 V	2.9							pF

5.6 Timing Requirements, V_{CC} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 6-1](#))

			T _A = 25°C		–40°C to +85°C		–40°C to +125°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration, LE high		6		6.5		6.5		ns
t _{su}	Setup time, data before LE↓	High or low	4.5		5		5.5		ns
t _h	Hold time, data after LE↓	High or low	1.5		1.5		2		ns

5.7 Timing Requirements, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 6-1](#))

			T _A = 25°C		–40°C to +85°C		–40°C to +125°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration, LE high		5		5		5		ns
t _{su}	Setup time, data before LE↓	High or low	4		4		4.5		ns
t _h	Hold time, data after LE↓	High or low	1		1		1.5		ns

5.8 Timing Requirements, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 6-1](#))

			T _A = 25°C		–40°C to +85°C		–40°C to +125°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration, LE high		5		5		5		ns
t _{su}	Setup time, data before LE↓	High or low	4		4		4.5		ns
t _h	Hold time, data after LE↓	High or low	1		1		1.5		ns

5.9 Switching Characteristics, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			$-40^\circ\text{C to } +85^\circ\text{C}$		$-40^\circ\text{C to } +125^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	$C_L = 15\text{ pF}$	8.3 ⁽¹⁾	15.2 ⁽¹⁾		1	17	1	18.5	ns
	LE	Q		9.1 ⁽¹⁾	15.7 ⁽¹⁾		1	19	1	20.5	
t_{en}	\overline{OE}	Q		8.9 ⁽¹⁾	15.8 ⁽¹⁾		1	19	1	20	
t_{dis}	\overline{OE}	Q		6.2 ⁽¹⁾	12.6 ⁽¹⁾		1	15	1	16.5	
t_{pd}	D	Q	$C_L = 50\text{ pF}$	10.4	18		1	21	1	22.5	ns
	LE	Q		11.1	18.6		1	22	1	23.5	
t_{en}	\overline{OE}	Q		10.9	18.8		1	22	1	23.5	
t_{dis}	\overline{OE}	Q		8.3	17.4		1	19	1	20.5	
$t_{sk(o)}$							2		2		2

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

5.10 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			$-40^\circ\text{C to } +85^\circ\text{C}$		$-40^\circ\text{C to } +125^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	$C_L = 15\text{ pF}$	5.8 ⁽¹⁾	11.4 ⁽¹⁾		1	13.5	1	14.5	ns
	LE	Q		6.4 ⁽¹⁾	11 ⁽¹⁾		1	13	1	14	
t_{en}	\overline{OE}	Q		6.3 ⁽¹⁾	11.4 ⁽¹⁾		1	13.5	1	14.5	
t_{dis}	\overline{OE}	Q		4.7 ⁽¹⁾	10 ⁽¹⁾		1	12	1	12.5	
t_{pd}	D	Q	$C_L = 50\text{ pF}$	7.3	14.9		1	17	1	18	ns
	LE	Q		7.8	14.5		1	16.5	1	17.5	
t_{en}	\overline{OE}	Q		7.7	14.9		1	17	1	18	
t_{dis}	\overline{OE}	Q		6	13.2		1	15	1	15.5	
$t_{sk(o)}$							1.5		1.5		1.5

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

5.11 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			$-40^\circ\text{C to } +85^\circ\text{C}$		$-40^\circ\text{C to } +125^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	$C_L = 15\text{ pF}$	4.1 ⁽¹⁾	7.2 ⁽¹⁾		1	8.5	1	9.5	ns
	LE	Q		4.5 ⁽¹⁾	7.2 ⁽¹⁾		1	8.5	1	9.5	
t_{en}	\overline{OE}	Q		4.5 ⁽¹⁾	8.1 ⁽¹⁾		1	9.5	1	10.5	
t_{dis}	\overline{OE}	Q		3.3 ⁽¹⁾	7.2 ⁽¹⁾		1	8.5	1	9	
t_{pd}	D	Q	$C_L = 50\text{ pF}$	5.1	9.2		1	10.5	1	11.5	ns
	LE	Q		5.5	9.2		1	10.5	1	11.5	
t_{en}	\overline{OE}	Q		5.5	10.1		1	11.5	1	12.5	
t_{dis}	\overline{OE}	Q		4	9.2		1	10.5	1	11	
$t_{sk(o)}$							1		1		1

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

5.12 Noise Characteristics

$V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ ⁽¹⁾

PARAMETER		SN74LV373A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.6	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		-0.6	-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		2.9		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

(1) Characteristics are for surface-mount packages only.

5.13 Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	$C_L = 50\text{ pF}$	$f = 10\text{ MHz}$	3.3 V	17.4	pF
					5 V	19.5	

5.14 Typical Characteristics

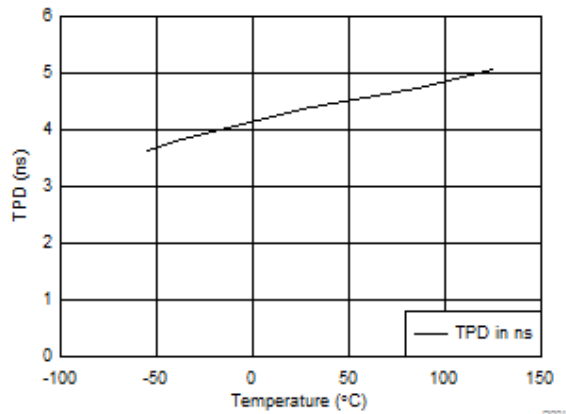


Figure 5-1. TPD vs Temperature at 5 V

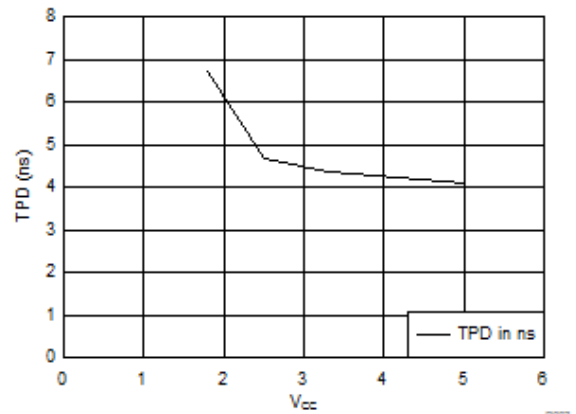
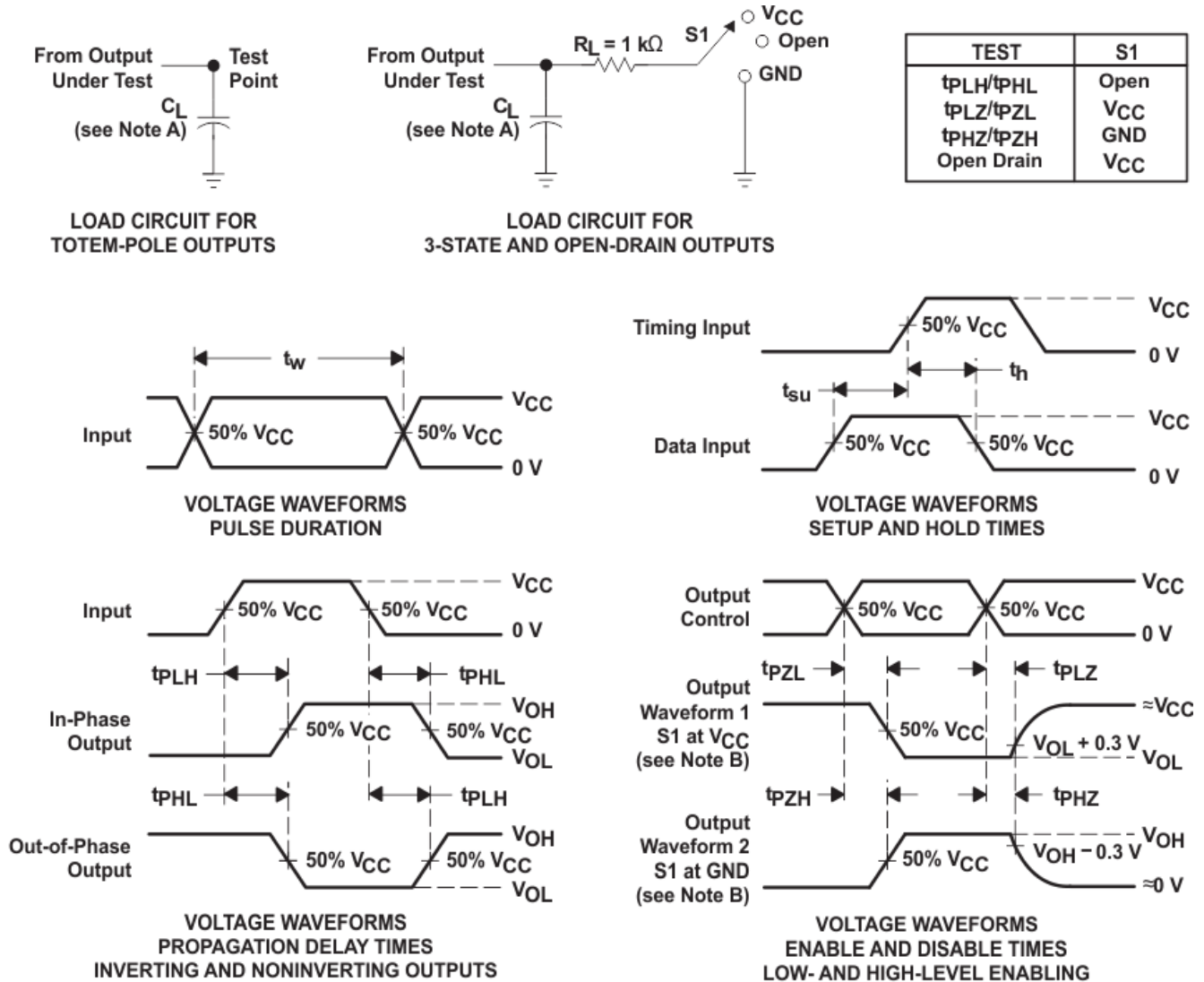


Figure 5-2. TPD vs V_{CC} at 25°C

6 Parameter Measurement Information

6.1



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 D. The outputs are measured one at a time, with one input transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PHL} and t_{PLH} are the same as t_{pd} .
 H. All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

The SN74LV373A device is an octal transparent D-type latch designed for 2 V to 5.5 V V_{CC} operation.

When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

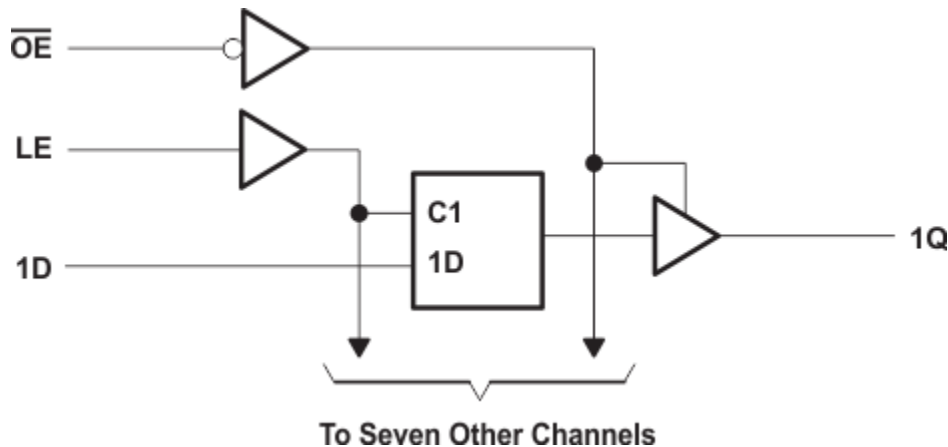
At power-up, the state of the Q outputs are not predictable until the first valid clock.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pull-up components.

\overline{OE} does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

7.2 Functional Block Diagram



7.3 Feature Description

- Wide operating voltage range
 - Operates from 2 V to 5.5 V
- Allows down-voltage translation
 - Inputs accept voltages to 5.5 V
- Slow edges reduce output ringing

7.4 Device Functional Modes

Table 7-1 shows the functional modes of SN74LV373A.

**Table 7-1. Function Table
(Each Latch)**

INPUTS			OUTPUT
OE	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN74LV540A device is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs are tolerant to 5.5 V at any valid V_{CC} . This feature makes it ideal for translating down to the V_{CC} level. Figure 8-2 shows the reduction in ringing compared to higher drive parts such as AC.

8.2 Typical Application

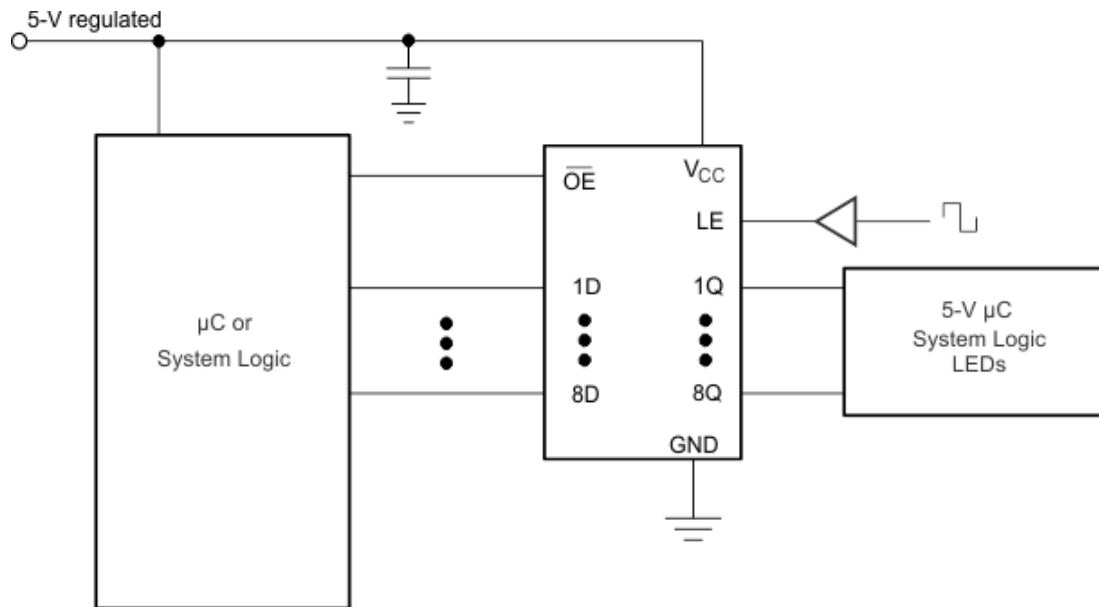


Figure 8-1. Typical Application Schematic

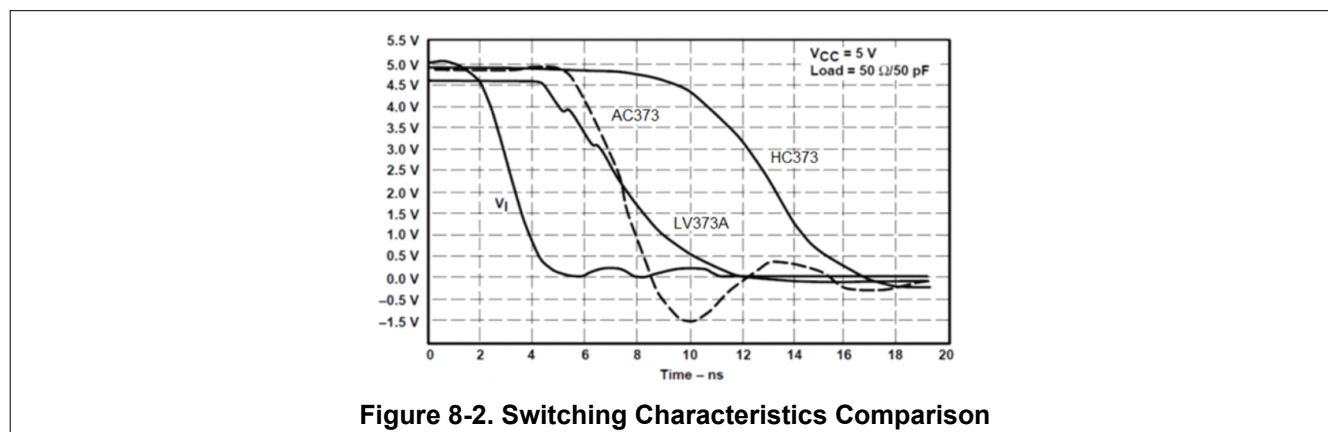
8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

8.2.2 Detailed Design Procedure

- Recommended Input Conditions
 - For rise time and fall time specifications, see $\Delta t/\Delta V$ in the [Section 5.3](#) table.
 - For specified High and low levels, see V_{IH} and V_{IL} in the [Section 5.3](#) table.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC} .
- Recommend Output Conditions
 - Load currents should not exceed 35 mA per output and 70 mA total for the part.
 - Outputs should not be pulled above V_{CC} .

8.2.3 Application Curves



Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Section 5.3](#) table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended. If there are multiple V_{CC} pins, 0.01 μF or 0.022 μF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

8.3 Layout

8.3.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [Figure 8-3](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

8.3.2 Layout Example

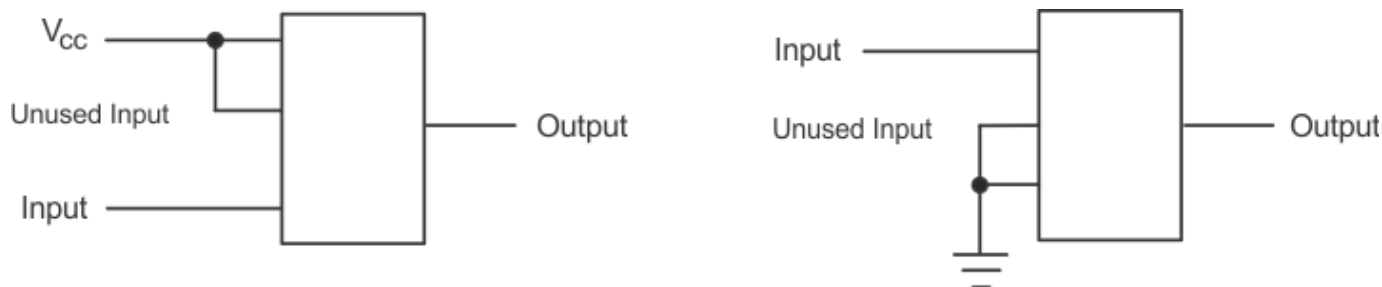


Figure 8-3. Layout Diagram

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Community Resources

9.3 Trademarks

All trademarks are the property of their respective owners.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision M (December 2022) to Revision N (December 2023)	Page
<ul style="list-style-type: none"> • Updated thermal values for PW package from RθJA = 102.4 to 128.2, RθJC(top) = 36.5 to 70.5, RθJB = 53.6 to 79.3, ΨJT = 2.4 to 23.4, ΨJB = 52.9 to 78.9, all values in °C/W..... 	5
Changes from Revision L (August 2016) to Revision M (December 2022)	Page
<ul style="list-style-type: none"> • Updated the format for tables, figures, and cross-references throughout the document..... 	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LV373ADBR	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV373A
SN74LV373ADGSR	Active	Production	VSSOP (DGS) 20	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L373A
SN74LV373ADGVR	Active	Production	TVSOP (DGV) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV373A
SN74LV373ADW	Obsolete	Production	SOIC (DW) 20	-	-	Call TI	Call TI	-40 to 125	LV373A
SN74LV373ADWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV373A
SN74LV373ANSR	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV373A
SN74LV373APW	Obsolete	Production	TSSOP (PW) 20	-	-	Call TI	Call TI	-40 to 125	LV373A
SN74LV373APWR	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV373A
SN74LV373APWRG4	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV373A
SN74LV373APWT	Obsolete	Production	TSSOP (PW) 20	-	-	Call TI	Call TI	-40 to 125	LV373A
SN74LV373ARGYR	Active	Production	VQFN (RGY) 20	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LV373A

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LV373A :

- Automotive : [SN74LV373A-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV373ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LV373ADGSR	VSSOP	DGS	20	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
SN74LV373ADGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV373ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LV373ANSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LV373APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LV373APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LV373APWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LV373ARGYR	VQFN	RGY	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV373ADBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74LV373ADGSR	VSSOP	DGS	20	5000	353.0	353.0	32.0
SN74LV373ADGVR	TVSOP	DGV	20	2000	356.0	356.0	35.0
SN74LV373ADWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LV373ANSR	SOP	NS	20	2000	367.0	367.0	45.0
SN74LV373APWR	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74LV373APWR	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74LV373APWRG4	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74LV373ARGYR	VQFN	RGY	20	3000	356.0	356.0	35.0

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

GENERIC PACKAGE VIEW

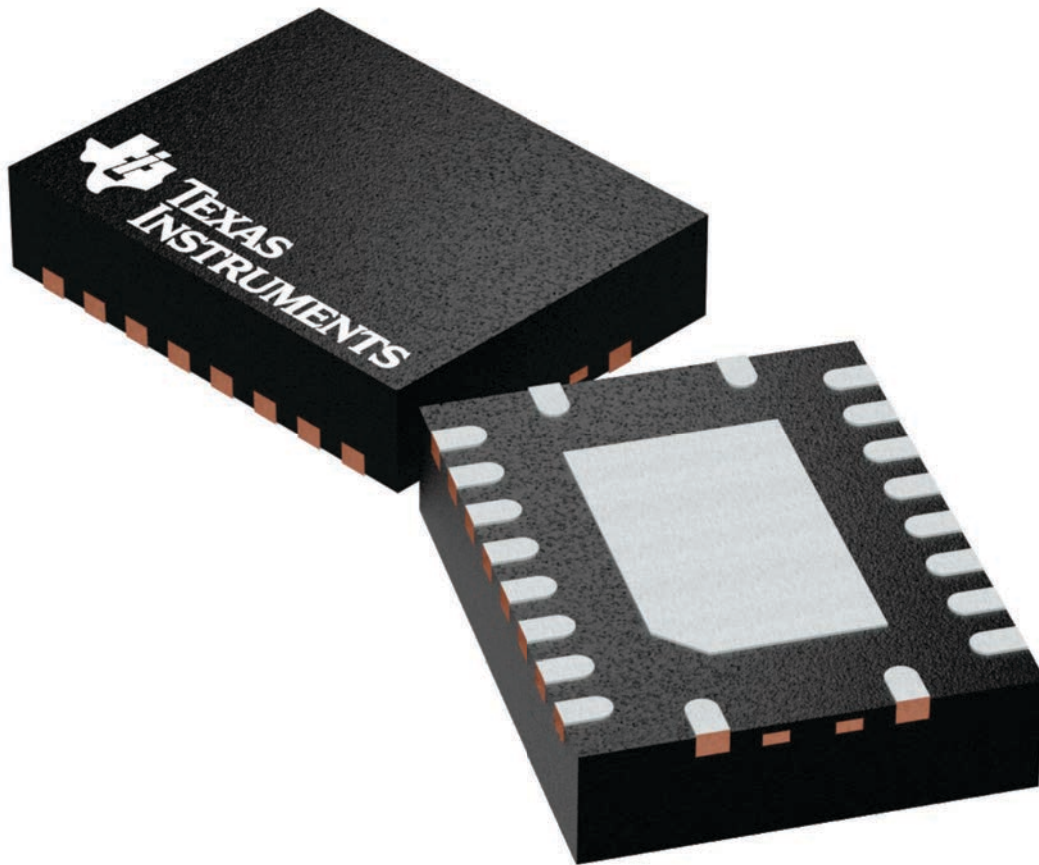
RGY 20

VQFN - 1 mm max height

3.5 x 4.5, 0.5 mm pitch

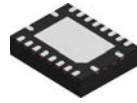
PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225264/A

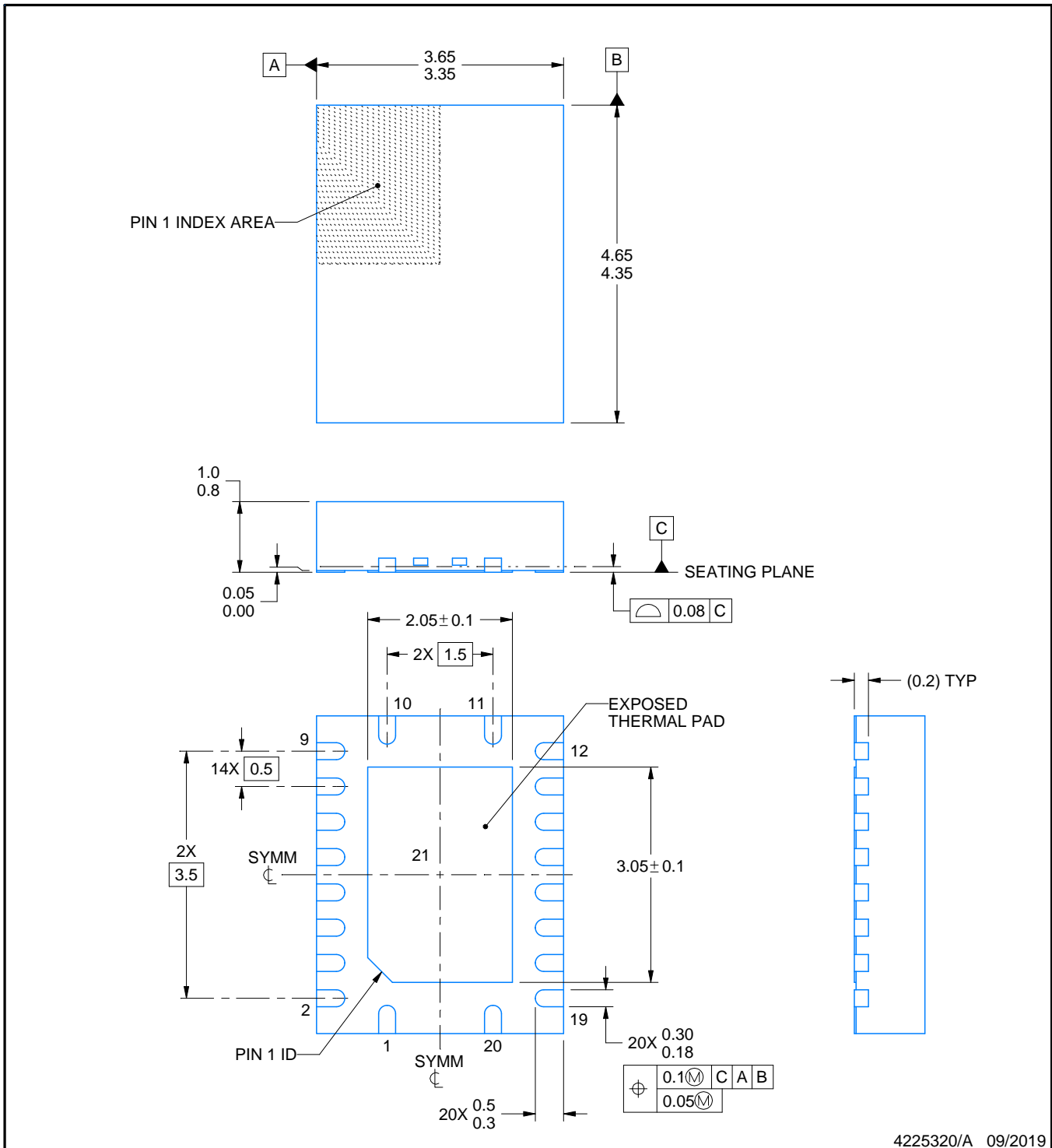
RGY0020A



PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4225320/A 09/2019

NOTES:

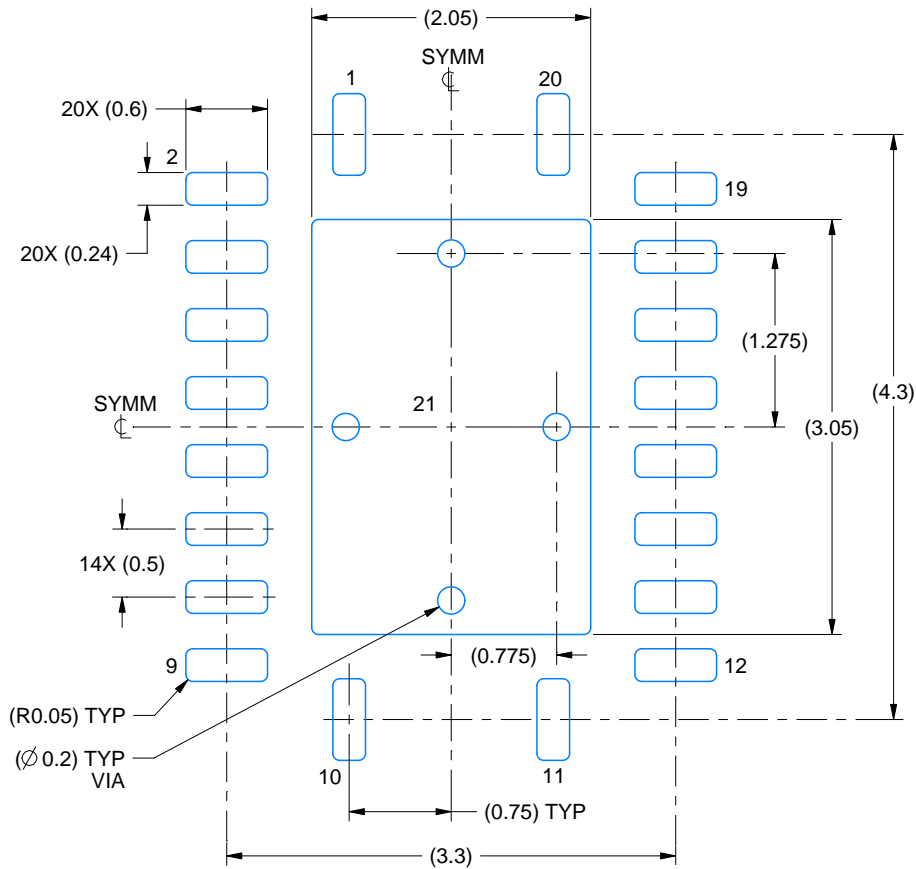
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

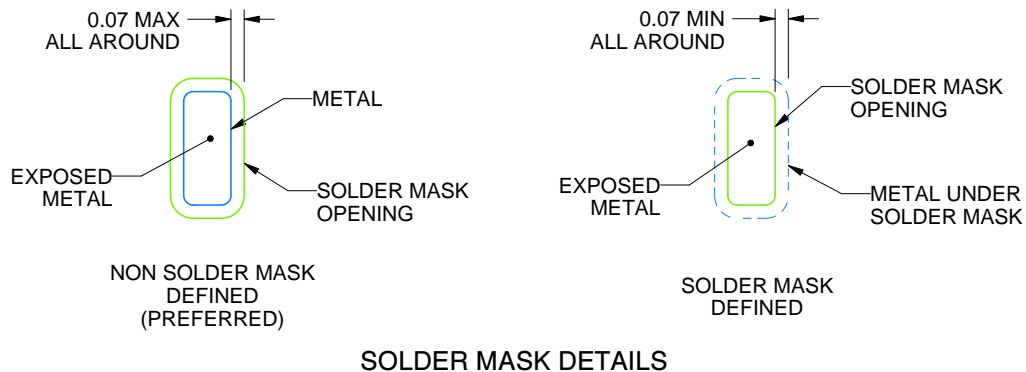
RGY0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4225320/A 09/2019

NOTES: (continued)

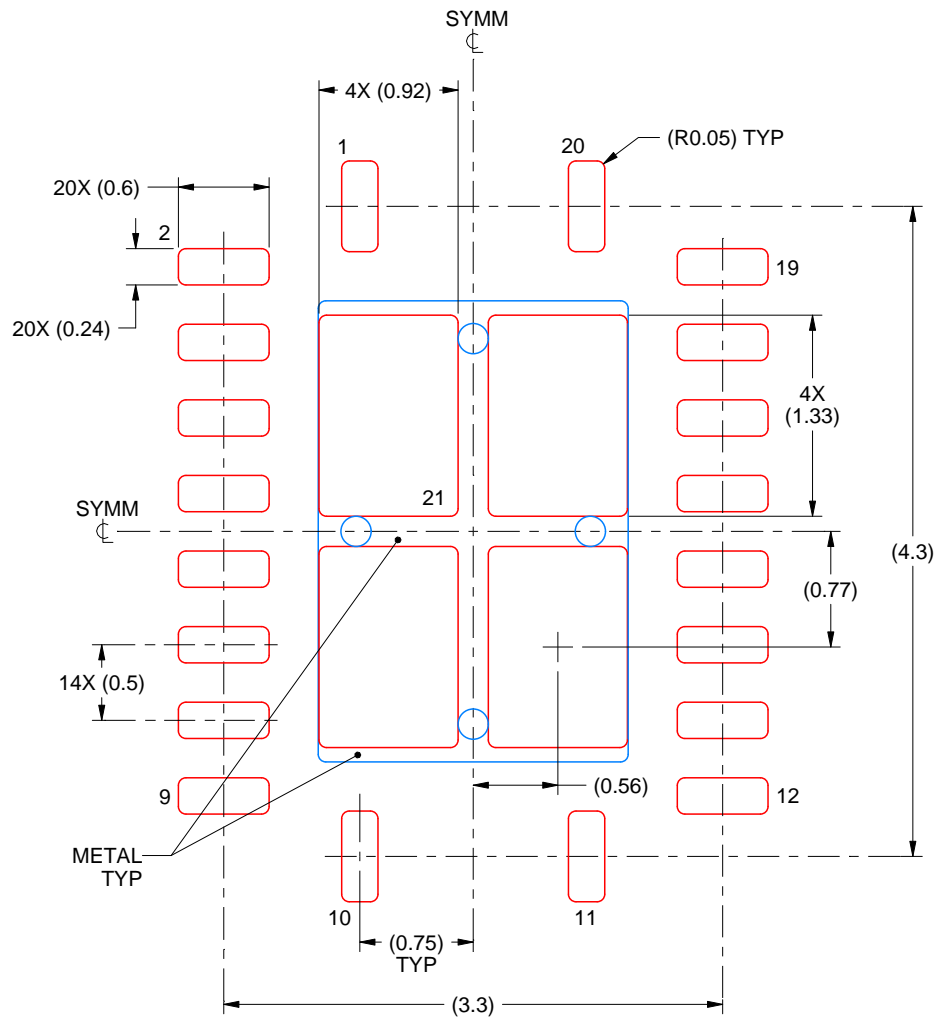
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGY0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 21
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4225320/A 09/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

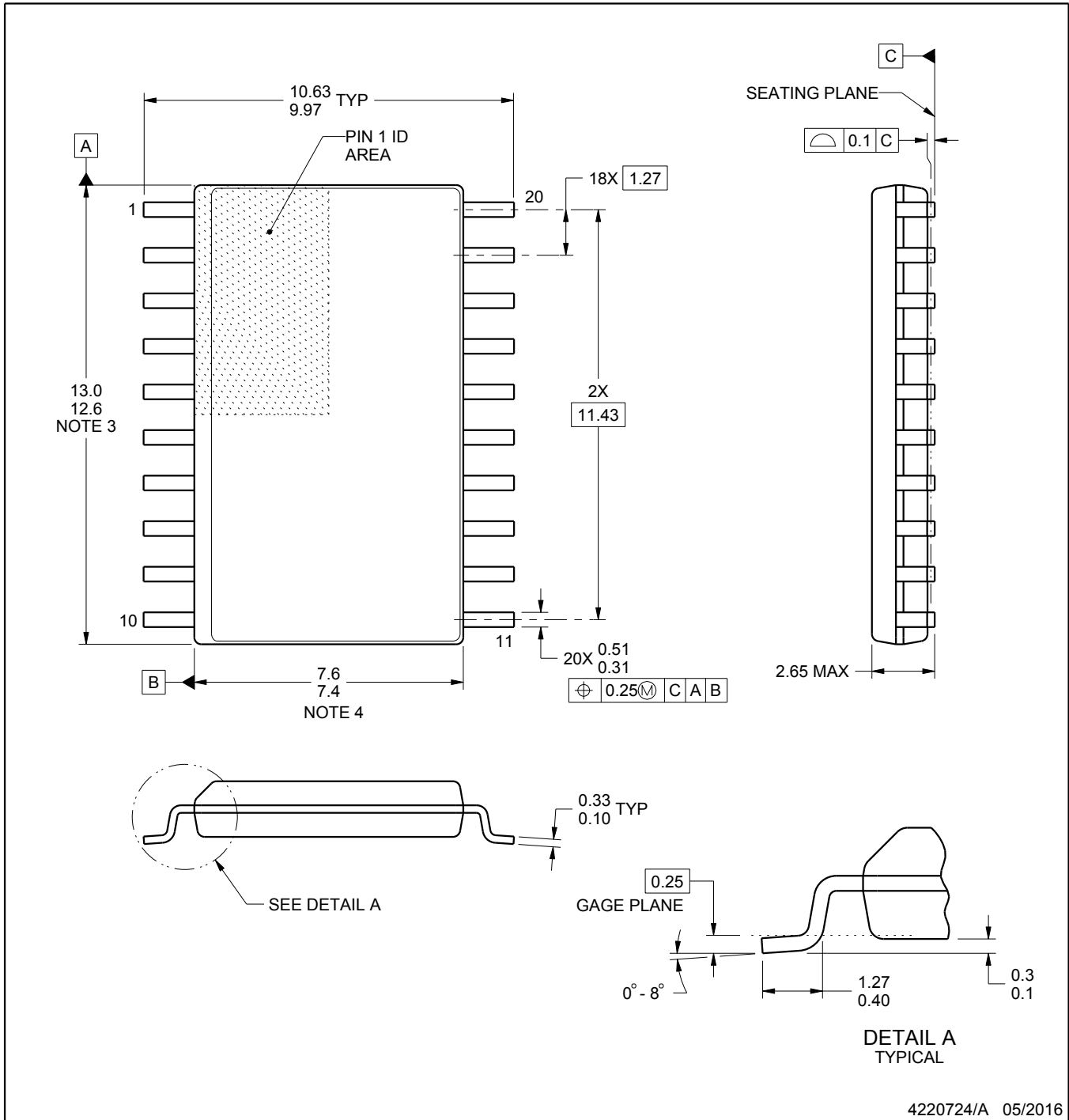
DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC

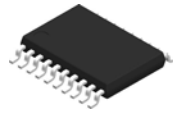


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220206/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

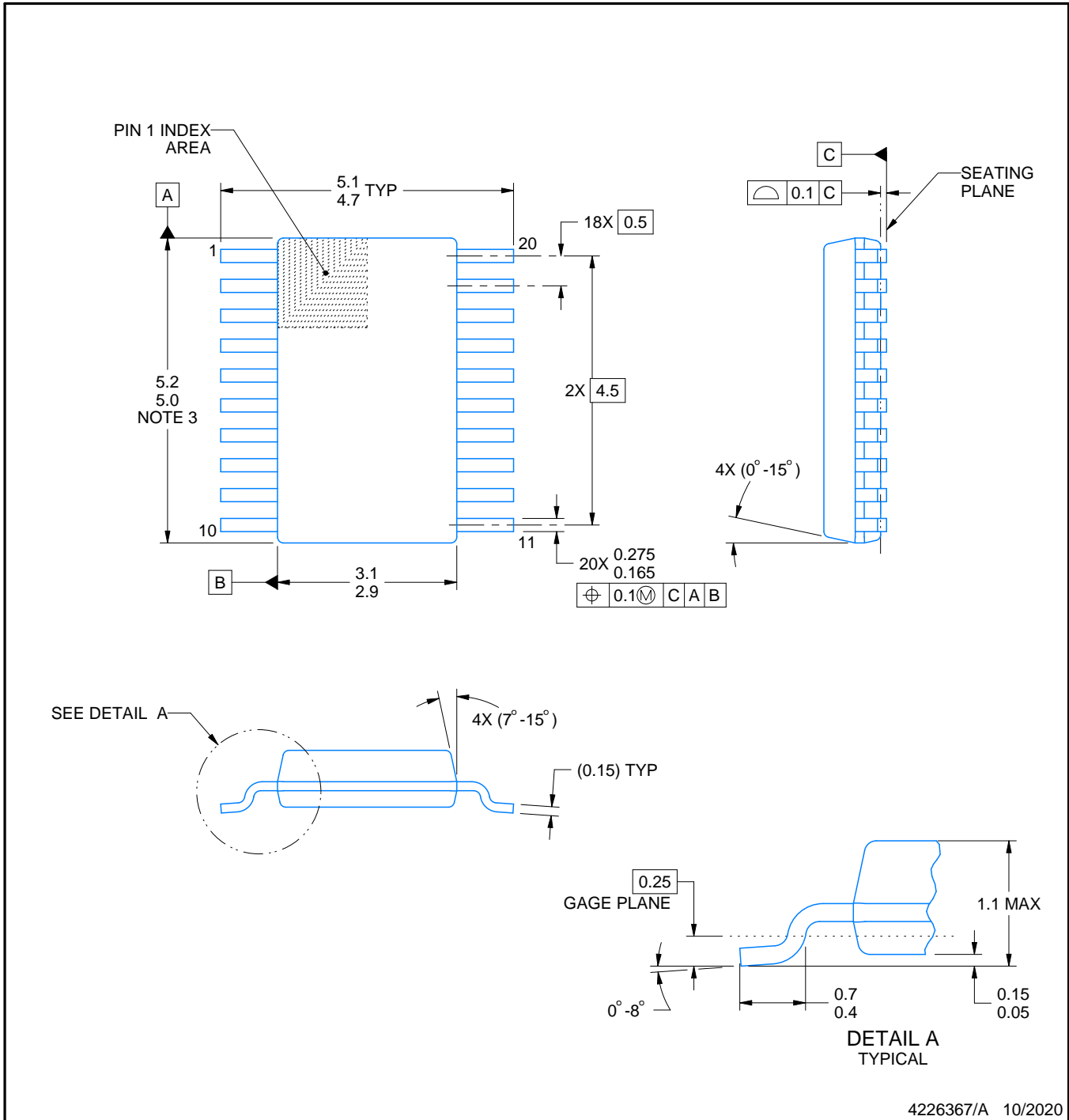
DGS0020A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES:

PowerPAD is a trademark of Texas Instruments.

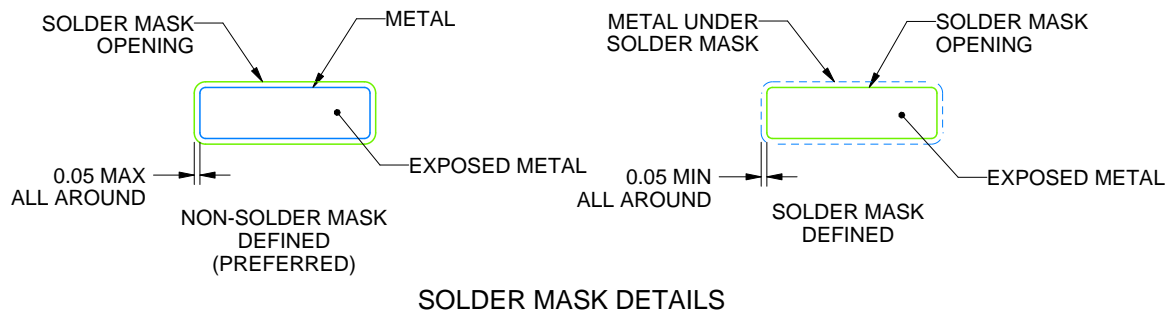
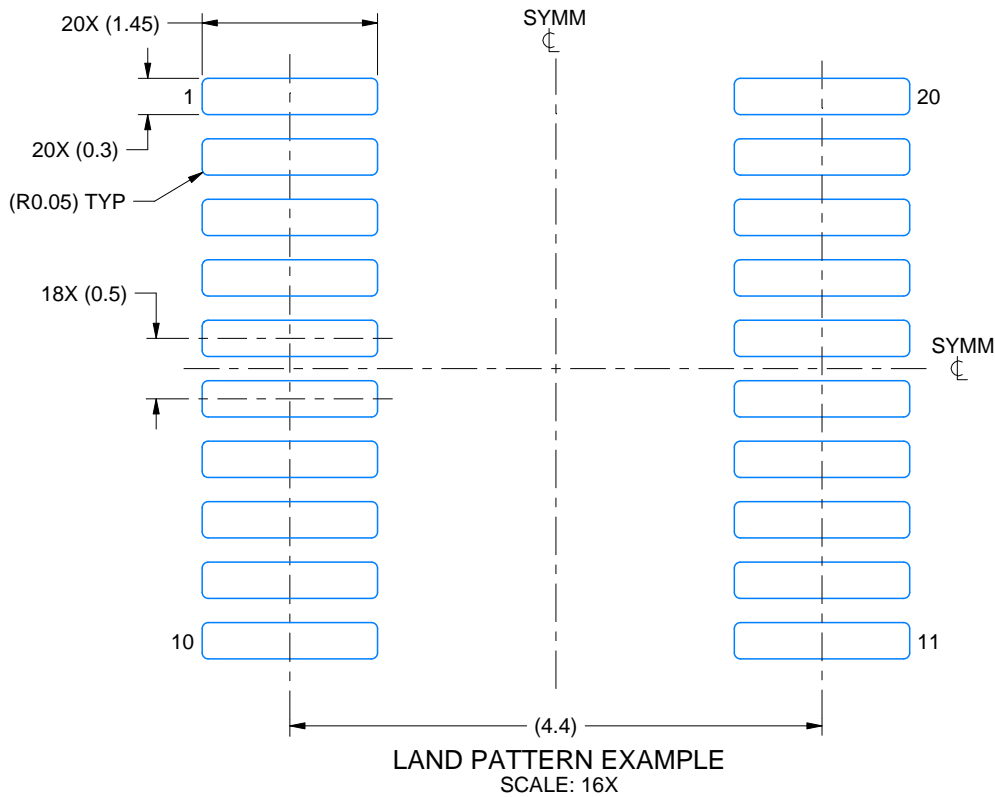
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4226367/A 10/2020

NOTES: (continued)

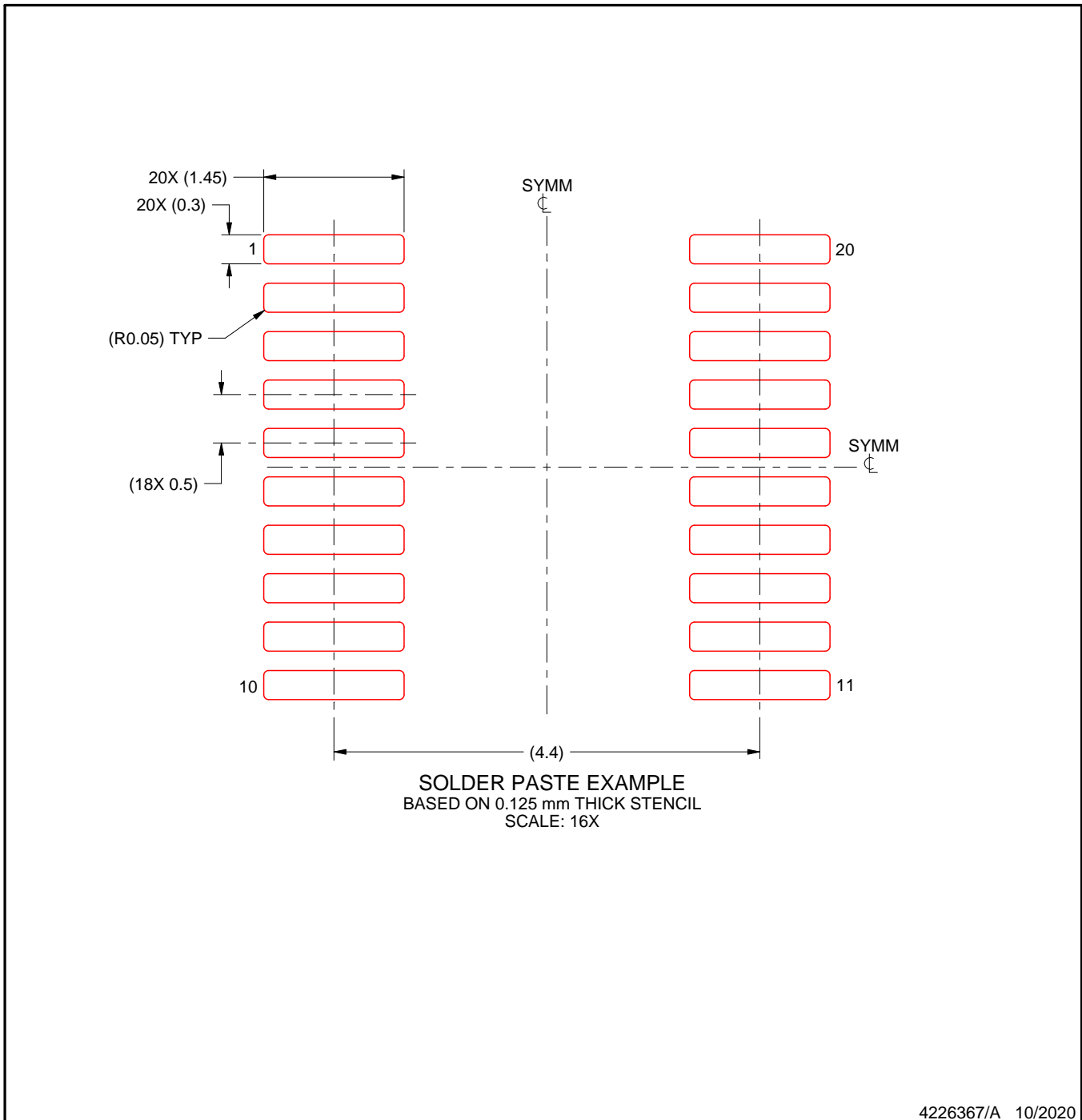
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DGS0020A

VSSOP - 1.1 mm max height

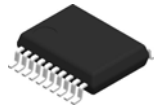
SMALL OUTLINE PACKAGE



NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

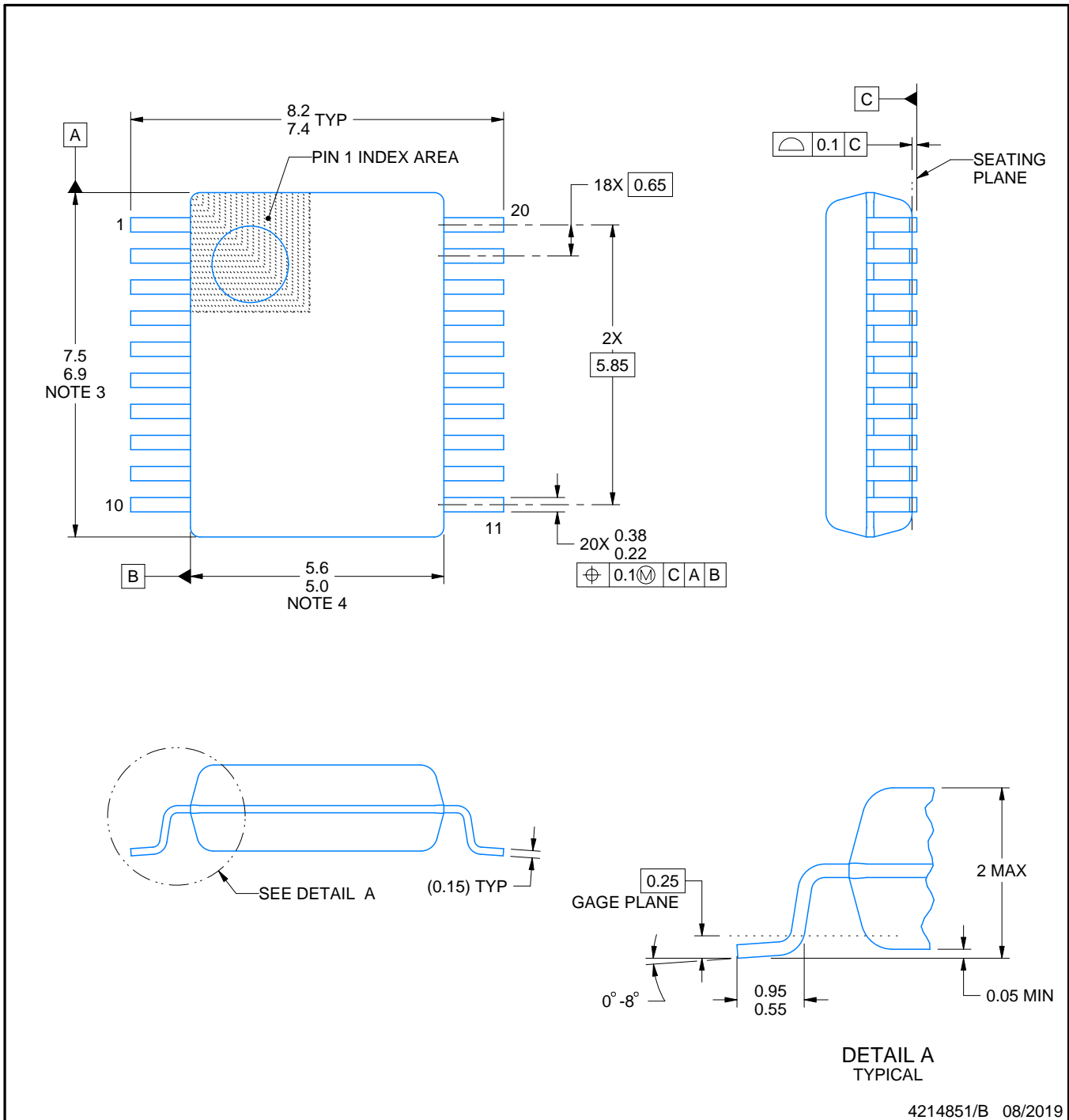
DB0020A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

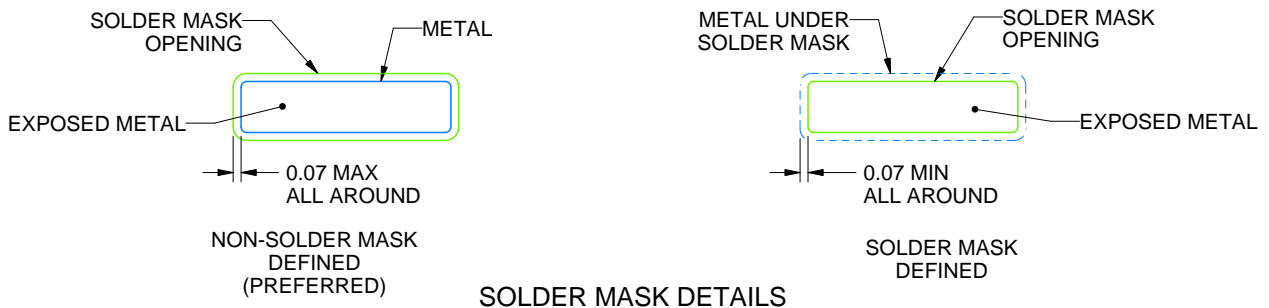
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

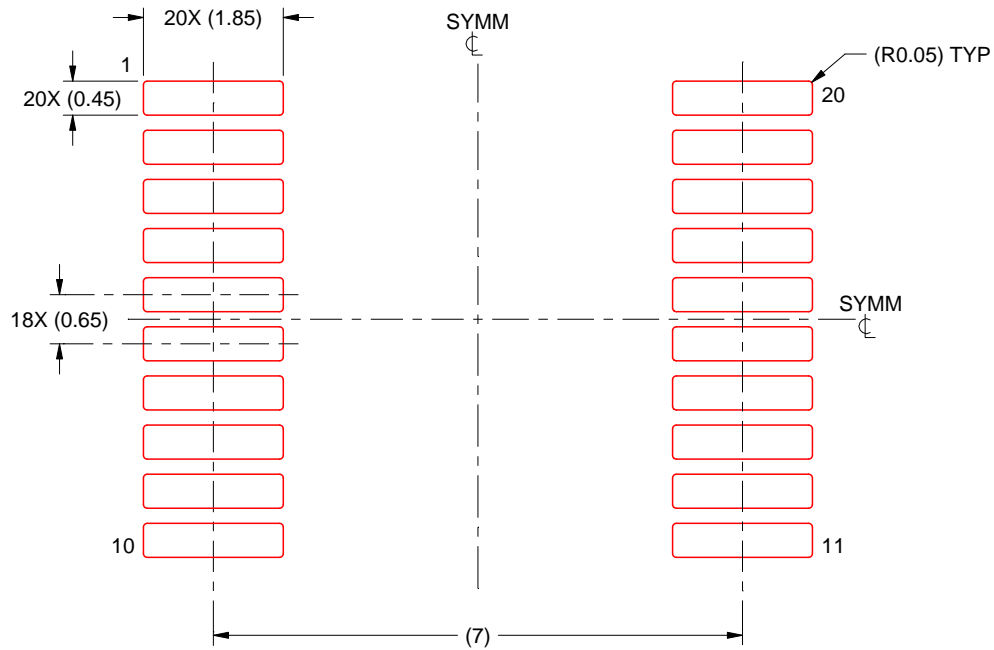
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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