SN74LV4046A High-Speed CMOS Logic Phase-Locked Loop With VCO

1 Features

- ESD Protection Exceeds JESD 22
  - 2000-V Human Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)
- Choice of Three Phase Comparators
  - Exclusive OR
  - Edge-Triggered J-K Flip-Flop
  - Edge-Triggered RS Flip-Flop
- Excellent VCO Frequency Linearity
- VCO-Inhibit Control for ON/OFF Keying and for Low Standby Power Consumption
- Optimized Power-Supply Voltage Range From 3 V to 5.5 V
- Wide Operating Temperature Range From –40°C to +125°C
- Latch-Up Performance Exceeds 250 mA Per JESD 17

2 Applications

- Telecommunications
- Signal Generators
- Digital Phase-Locked Loop

3 Description

The SN74LV4046A is a high-speed silicon-gate CMOS device that is pin compatible with the CD4046B and the CD74HC4046. The device is specified in compliance with JEDEC Std 7.

The SN74LV4046A is a phase-locked loop (PLL) circuit that contains a linear voltage-controlled oscillator (VCO) and three different phase comparators (PC1, PC2, and PC3). A signal input and a comparator input are common to each comparator.

The signal input can be directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. A self-bias input circuit keeps small voltage signals within the linear region of the input amplifiers. With a passive low-pass filter, the SN74LV4046A forms a second-order loop PLL. The excellent VCO linearity is achieved by the use of linear operational amplifier techniques. Various applications include telecommunications, digital phase-locked loop and signal generators.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LV4046ANS	SO (16)	7.70 mm × 10.20 mm
SN74LV4046AD	SOIC (16)	6.00 mm × 9.90 mm
SN74LV4046APW	TSSOP (16)	6.40 mm × 5.00 mm
SN74LV4046ADGVR	TVSOP (16)	3.60 mm × 4.40 mm
SN74LV4046AN	PDIP (16)	19.30 mm × 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

SN74LV4046A Functional Block Diagram

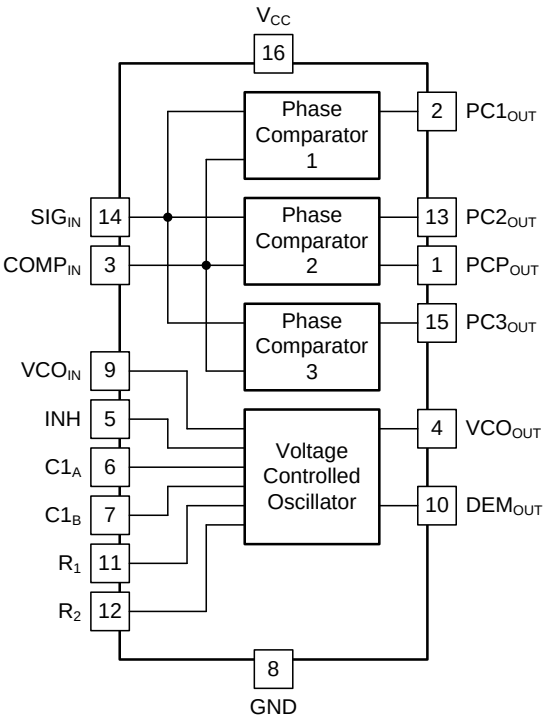


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (September 2015) to Revision E — **Page**

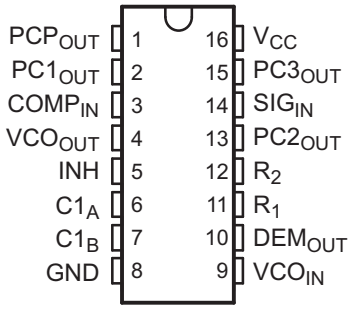
- Deleted 200-V Machine Model (A115-A) from *Features* ... 1
- Added TVSOP and PDIP packages to *Device Information* table ... 1
- Added TVSOP, SO, and PDIP packages to pinout ... 3
- Changed $R_{\theta JA}$ for D package from 73°C/W to 82.8°C/W ... 4
- Changed $R_{\theta JA}$ for DGV package from 120°C/W to 116.8°C/W ... 4
- Changed $R_{\theta JA}$ for NS package from 64°C/W to 83.5°C/W ... 4
- Changed $R_{\theta JA}$ for PW package from 108°C/W to 108.1°C/W ... 4
- Added values in the *Thermal Information* table to align with JEDEC standards ... 4
- Changed x-axis from "–360° 0° 360°" to "0° 90° 180°" ... 9
- Changed "(V_{CC}/4)" to "(V_{CC}/4π)" ... 9
- Added *Receiving Notification of Documentation Updates* section ... 15

Changes from Revision C (April 2007) to Revision D — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

5 Pin Configuration and Functions

D, DGV, NS, N, or PW Package
16-Pin SOIC, TVSOP, SO, PDIP, or TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	PCP_{OUT}	O	Phase comparator pulse output
2	$PC1_{OUT}$	O	Phase comparator 1 output
3	$COMP_{IN}$	I	Comparator input
4	VCO_{OUT}	O	VCO output
5	INH	I	Inhibit input
6	$C1_A$	—	Capacitor C1 connection A
7	$C1_B$	—	Capacitor C1 connection B
8	GND	—	Ground (0 V)
9	VCO_{IN}	I	VCO input
10	DEM_{OUT}	O	Demodulator output
11	R_1	—	Resistor R1 connection
12	R_2	—	Resistor R2 connection
13	$PC2_{OUT}$	O	Phase comparator 2 output
14	SIG_{IN}	I	Signal input
15	$PC3_{OUT}$	O	Phase comparator 3 output
16	V_{CC}	—	Positive supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	DC supply voltage		–0.5	7	V
V_I	Input voltage		–0.5	V_{CC} + 0.5	V
V_O	Output voltage		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		–20	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output curent	V_O = 0 to V_{CC}		±35	mA
I_{CC}	DC V_{CC} or ground current			±70	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
T_A	Operating free-air temperature	–40	125	°C
V_{CC}	Supply voltage	3	5.5	V
V_I, V_O	DC input or output voltage	0	V_{CC}	V

6.4 Thermal Information

THERMAL METRIC(1)		SN74LV4046A					UNIT
		D (SOIC)	DGV (TVSOP)	NS (SO)	PW (TSSOP)	N (PDIP)	
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	82.8	116.8	83.5	108.1	49.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	44.0	43.3	41.7	42.7	36.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.3	48.3	43.8	53.1	29.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.1	3.7	9.3	4.2	21.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	40.0	47.8	43.5	52.5	29.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER				TEST CONDITIONS		V_{CC} (V)	MIN	TYP	MAX	UNIT
				V_I (V)	I_O (mA)					
VCO										
V_{IH}	High-level input voltage	INH				3 to 3.6	V_{CC} × 0.7			V
						4.5 to 5.5	V_{CC} × 0.7			
V_{IL}	Low-level input voltage	INH				3 to 5.5			V_{CC} × 0.3	V
						4.5 to 5.5			V_{CC} × 0.3	
V_{OH}	High-level output voltage	VCO_{OUT}	CMOS	V_{IL} or V_{IH}	–0.05	3 to 3.6	V_{CC} – 0.1			V
						4.5 to 5.5	V_{CC} – 0.1			
			TTL		–12	4.5 to 5.5	3.8			
V_{OL}	Low-level output voltage	VCO_{OUT}	CMOS	V_{IL} or V_{IH}	0.05	3 to 3.6			0.1	V
						4.5 to 5.5			0.1	
			TTL		12	4.5 to 5.5			0.55	
		C1A, C1B (test purposes only)			12	4.5 to 5.5			0.65	
I_I	Input leakage current	INH, VCO_{IN}		V_{CC} or GND		5.5			±1	µA
	R1 range[1]					3 to 5.5	3		50	kΩ
	R2 range[1]					3 to 5.5	3		50	kΩ
	C1 capacitance range					3 to 3.6	40		No Limit	pF
						4.5 to 5.5	40		No Limit	
	Operating voltage range	VCO_{IN}		Over the range specified for R1 for linearity[2]		3 to 3.6	1.1		1.9	V
						4.5 to 5.5	1.1		3.2	
PHASE COMPARATOR										
V_{IH}	DC-coupled high-level input voltage		SIG_{IN}, $COMP_{IN}$			3 to 3.6	V_{CC} × 0.7			
						4.5 to 5.5	V_{CC} × 0.7			
V_{IL}	DC-coupled low-level input voltage		SIG_{IN}, $COMP_{IN}$			3 to 3.6			V_{CC} × 0.3	V
						4.5 to 5.5			V_{CC} × 0.3	
V_{OH}	High-level output voltage	PCP_{OUT}, PCN_{OUT}	CMOS	V_{IL} or V_{IH}	–0.05	3 to 5.5	V_{CC} – 0.1			V
					–6	3 to 3.6	2.48			
			TTL		–12	4.5 to 5.5	3.8			
V_{OL}	Low-level output voltage	PCP_{OUT}, PCN_{OUT}	CMOS	V_{IL} or V_{IH}	0.02	3 to 3.6			0.1	V
						4.5 to 5.5			0.1	
			TTL		4	4.5 to 5.5			0.4	
I_I	Input leakage current		SIG_{IN}, $COMP_{IN}$	V_{CC} or GND		3 to 3.6			±11	µA
						4.5 to 5.5			±29	
I_{OZ}	3-state off-state current		$PC2_{OUT}$	V_{IL} or V_{IH}		3 to 5.5			±5	µA
R_I	Input resistance		SIG_{IN}, $COMP_{IN}$	V_I at self-bias operating point, V_I = 0.5 V		3		800		kΩ
						4.5		250		
DEMODULATOR										
R_S	Resistor range			R_S > 300 kΩ, Leakage current can influence V_{DEMOUT}		3 to 3.6	50		300	kΩ
						4.5 to 5.5	50		300	
V_{OFF}	Offset voltage VCO_{IN} to V_{DEM}			V_I = V_{VCOIN} = $V_{CC/2}$, Values taken over R_S range		3 to 3.6		±30		mV
						4.5 to 5.5		±20		
I_{CC}	Quiescent device current			Pins 3, 5, and 14 at V_{CC}, Pin 9 at GND, I_I at pins 3 and 14 to be excluded		5.5			50	µA

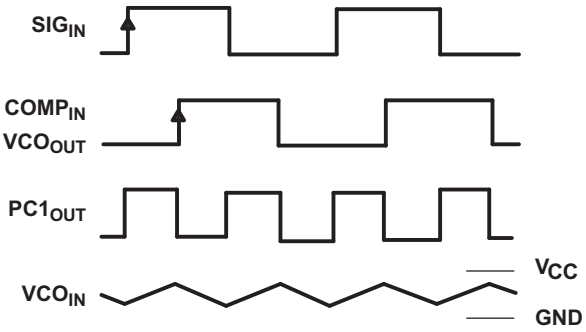
(1) The value for R1 and R2 in parallel should exceed 2.7 kΩ.
(2) The maximum operating voltage can be as high as V_{CC} – 0.9 V; however, this may result in an increased offset voltage.

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted) C_L = 50 pF, Input t_r, t_f = 6 ns

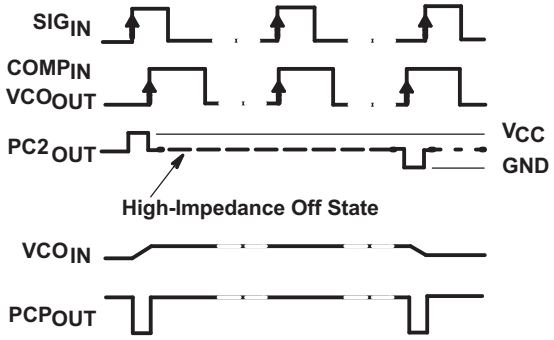
PARAMETER			TEST CONDITIONS	V_{CC} (V)	MIN	TYP	MAX	UNIT
PHASE COMPARATOR								
t_{PLH}, t_{PHL}	Propagation delay	SIG_{IN}, $COMP_{IN}$ to $PC1_{OUT}$		3 to 3.6			135	ns
				4.5 to 5.5			50	
t_{PLH}, t_{PHL}	Propagation delay	SIGIN, $COMP_{IN}$ to PCP_{OUT}		3 to 3.6			300	ns
				4.5 to 5.5			60	
t_{PLH}, t_{PHL}	Propagation delay	SIG_{IN}, $COMP_{IN}$ to $PC3_{OUT}$		3 to 3.6			200	ns
				4.5 to 5.5			50	
t_{THL}, t_{TLH}	Output transition time			3 to 3.6			75	ns
				4.5 to 5.5			15	
t_{PZH}, t_{PZL}	3-state output enable time	SIG_{IN}, $COMP_{IN}$ to $PC2_{OUT}$		3 to 3.6			270	ns
				4.5 to 5.5			54	
t_{PHZ}, t_{PLZ}	3-state output disable time	SIG_{IN}, $COMP_{IN}$ to PC2OUT		3 to 3.6			320	ns
				4.5 to 5.5			65	
	AC-coupled input sensitivity	(P-P) at SIG_{IN} or $COMP_{IN}$	$V_{I(P-P)}$	3 to 3.6		11		mV
				4.5 to 5.5		15		
VCO								
$\Delta f/\Delta T$	Frequency stability with temperature change		V_I = VCO_{IN} = 1/2 V_{CC}, R_1 = 100 kΩ, R_2 = ∞, C_1 = 100 pF	3 to 3.6		0.11		%/°C
				4.5 to 5.5		0.11		
f_{MAX}	Maximum frequency		C_1 = 50 pF, R_1 = 3.5 kΩ, R_2 = ∞	3 to 3.6		24		MHz
				4.5 to 5.5		24		
			C_1 = 0 pF, R_1 = 9.1 kΩ, R2 = ∞	3 to 3.6		38		
				4.5 to 5.5		38		
	Center frequency (duty 50%)		C_1 = 40 pF, R_1 = 3 kΩ, R_2 = ∞, VCO_{IN} = V_{CC}/2	3 to 3.6	7	10		MHz
				4.5 to 5.5	12	17		
				4.5 (1)	15 (1)		17.5 (1)	
ΔfVCO	Frequency linearity		C_1 = 100 pF, R_1 = 100 kΩ, R_2 = ∞	3 to 3.6		0.4%		
				4.5 to 5.5		0.4%		
	Offset frequency		C_1 = 1 nF, R_2 = 220 kΩ	3 to 3.6		400		kHz
				4.5 to 5.5		400		
DEMODULATOR								
V_{OUT} vs f_{IN}			C_1 = 100 pF, C_2 = 100 pF, R_1 = 100 kΩ, R_2 = ∞, R_3 = 100 kΩ	3		8		mV/kHz
				4.5		330		

(1) Data is specified at 25°C



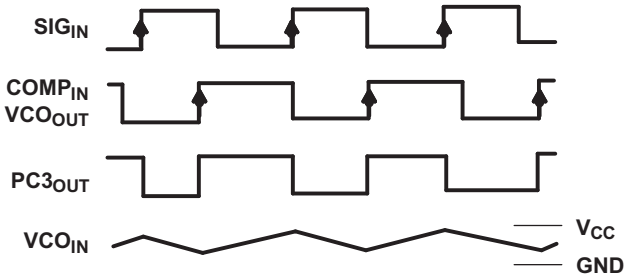
Loop Locked at f_o

Figure 1. Typical Waveforms for PLL Using Phase Comparator 1



Loop Locked at f_o

Figure 2. Typical Waveforms for PLL Using Phase Comparator 2



Loop Locked at f_o

Figure 3. Typical Waveforms for PLL Using Phase Comparator 3

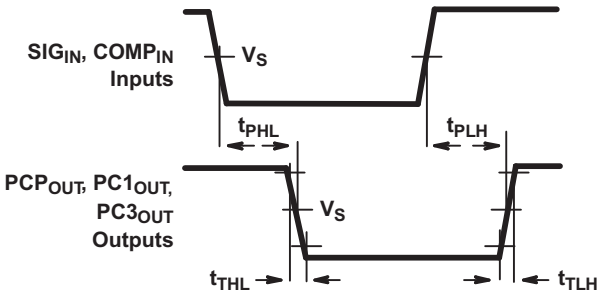


Figure 4. Input-to-Output Propagation Delays and Output Transition Times

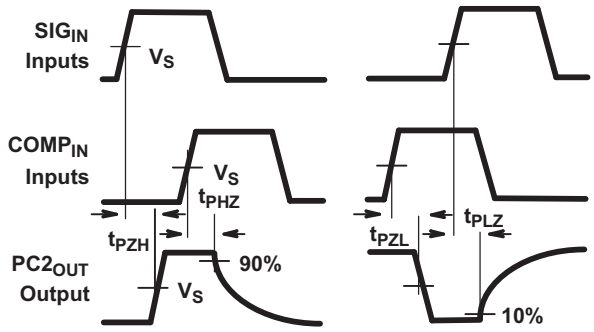
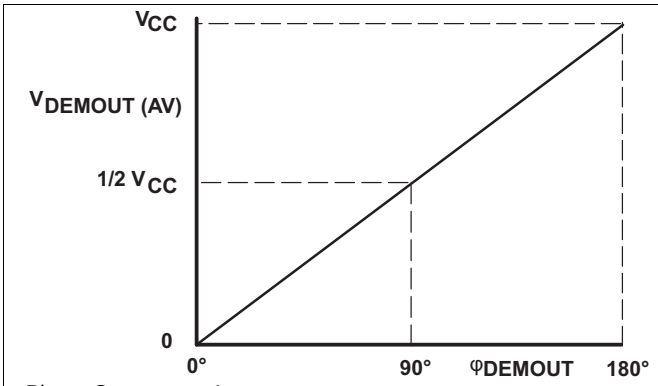


Figure 5. 3-State Enable and Disable Times for $PC2_{OUT}$

6.7 Typical Characteristics

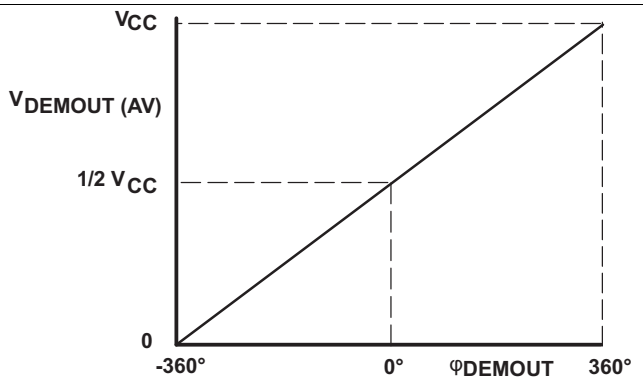


Phase Comparator 1:

$V_{DEMOUT} = V_{PC1OUT} = (V_{CC}/\pi)\ (SIG_{IN} - COMP_{IN})$;

DEMOUT = $(SIG_{IN} - COMP_{IN})$

Figure 6. Average Output Voltage vs Input Phase Difference

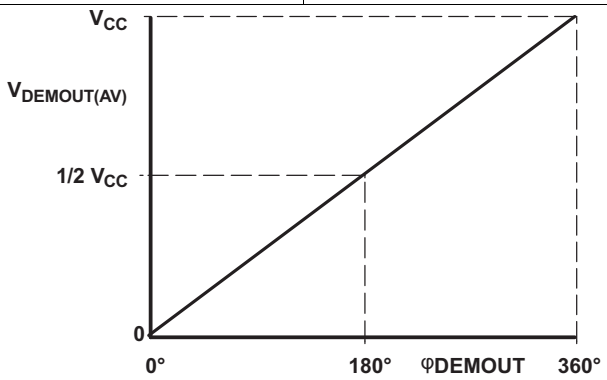


Phase Comparator 2:

$V_{DEMOUT} = V_{PC2OUT} = (V_{CC}/4\pi)\ (SIG_{IN} - COMP_{IN})$;

DEMOUT = $(SIG_{IN} - COMP_{IN})$

Figure 7. Average Output Voltage vs Input Phase Difference



Phase Comparator 3:

$V_{DEMOUT} = V_{PC3OUT} = (V_{CC}/2\pi)\ (SIG_{IN} - COMP_{IN})$;

DEMOUT = $(SIG_{IN} - COMP_{IN})$

Figure 8. Average Output Voltage vs Input Phase Difference

7 Detailed Description

7.1 Overview

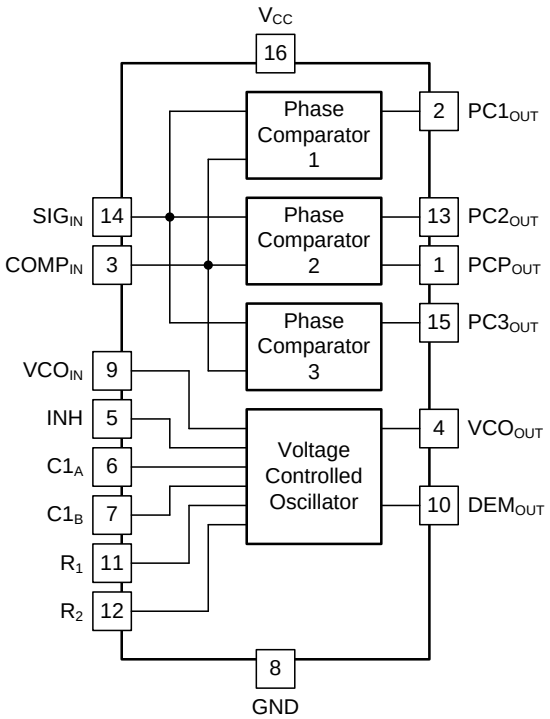
The SN74LV4046A is a high-speed silicon-gate CMOS device that is pin compatible with the CD4046B and the CD74HC4046. The device is specified in compliance with JEDEC Std 7.

The SN74LV4046A is a phase-locked loop (PLL) circuit that contains a linear voltage-controlled oscillator (VCO) and three different phase comparators (PC1, PC2, and PC3) as explained in the *Features* section. A signal input and a comparator input are common to each comparator as shown in the *Functional Block Diagram*.

The signal input can be directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. A self-bias input circuit keeps small voltage signals within the linear region of the input amplifiers. With a passive lowpass filter, the SN74LV4046A forms a second-order loop PLL. The excellent VCO linearity is achieved by the use of linear operational amplifier techniques. Various applications include telecommunications, Digital Phase Locked Loop and Signal generators.

The VCO requires one external capacitor C1 (between C1A and C1B) and one external resistor R1 (between R1 and GND) or two external resistors R1 and R2 (between R1 and GND, and R2 and GND). Resistor R1 and capacitor C1 determine the frequency range of the VCO. Resistor R2 enables the VCO to have a frequency offset if required. The high input impedance of the VCO simplifies the design of lowpass filters by giving the designer a wide choice of resistor or capacitor ranges. In order to not load the lowpass filter, a demodulator output of the VCO input voltage is provided at pin 10 (DEM_{OUT}). In contrast to conventional techniques where the DEM_{OUT} voltage is one threshold voltage lower than the VCO input voltage, here the DEM_{OUT} voltage equals that of the VCO input. If DEM_{OUT} is used, a load resistor (R_S) should be connected from DEM_{OUT} to GND; if unused, DEM_{OUT} should be left open. The VCO output (VCO_{OUT}) can be connected directly to the comparator input ($COMP_{IN}$), or connected through a frequency divider. The VCO output signal has a specified duty factor of 50%. A LOW level at the inhibit input (INH) enables the VCO and demodulator, while a HIGH level turns both off to minimize standby power consumption.

7.2 Functional Block Diagram



7.3 Feature Description

There are three choices for the Phase Comparators in this device which are listed as follows:

- Phase comparator 1 (PC1) is an Exclusive OR network. The average output voltage from PC1, fed to VCO input through the low pass filter and seen at the demodulator output at pin 10 (V_{DEMOUT}), is the resultant of the phase differences of signals (SIG_{IN}) and the compartor input ($COMP_{IN}$) as shown in Figure 7. The average of V_{DEM} is equal to 1/2 VCC when there is no signal or noise at SIG_{IN}, and with this input the VCO oscillates at the center frequency (fo).
- Phase comparator 2 (PC2) is an Edge-Triggered Flip-Flop. This is a positive edge-triggered phase and frequency detector. When the PLL is using this comparator, the loop is controlled by positive signal transitions and the duty factors of SIG_{IN} and $COMP_{IN}$ are not important. PC2 comprises two D-type flip-flops, control-gating and a three-state output stage. The circuit functions as an up-down counter where SIG_{IN} causes an up-count and $COMP_{IN}$ a down-count. The average output voltage from PC2, fed to the VCO through the lowpass filter and seen at the demodulator output at pin 10 (V_{DEMOUT}), is the resultant of the phase differences of SIG_{IN} and $COMP_{IN}$as in Figure 8.
- Phase comparator 3 (PC3) is an positive Edge-Triggered RS Flip-Flop. This is a positive edge-triggered sequential phase detector using an RS-type flip-flop. When the PLL is using this comparator, the loop is controlled by positive signal transitions and the duty factors of SIG_{IN} and $COMP_{IN}$ are not important. The average output from PC3, fed to the VCO through the lowpass filter and seen at the demodulator at pin 10 (V_{DEMOUT}), is the resultant of the phase differences of SIG_{IN} and $COMP_{IN}$ as shown in Figure 9.

The excellent VCO linearity is achieved by the use of linear operational amplifier techniques. It has low standby power consumption using VCO inhibit control. Wide operating temperature range from –40°C to +125°C along with an optimized power supply voltage range from 3 V to 5.5 V.

7.4 Device Functional Modes

The SN74LV4046A device does not feature any special functional modes.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The most common use for the digital phased-locked loop (PLL) device is to match the VCO output to the same phase as the incoming signal and produce an error signal (DEM_{OUT}) that indicates the amount of phase shift required for the match. This can be used as part of many complex systems.

8.2 Typical Application

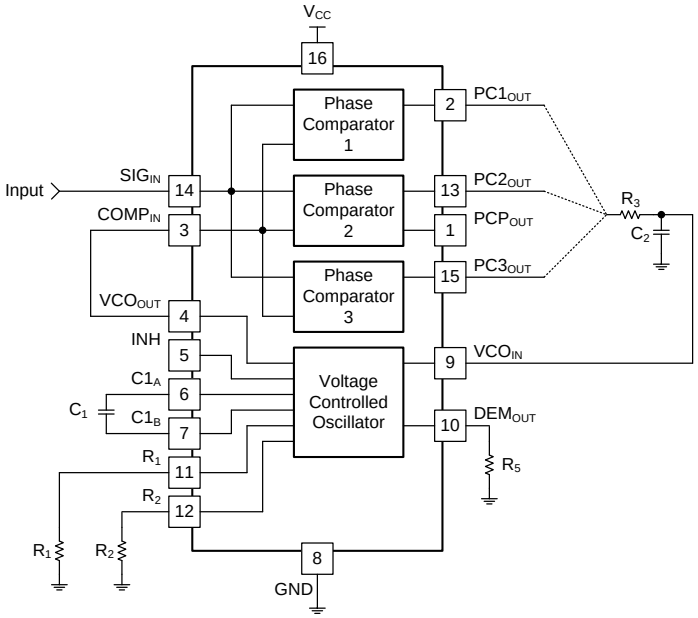


Figure 9. SN74LV4046A Digital Clock Signal Phase Comparison Application

Typical Application (continued)

8.2.1 Design Requirements

Table 1 and Table 2 lists the design requirements of the SN74LV4046A.

Table 1. Component Selection Criteria(1)

COMPONENT	VALUE
R1	3 kΩ to 50 kΩ
R2	3 kΩ to 50 kΩ
R1 || R2	> 2.7 kΩ
C1	> 40 pF
R3	1 kΩ
C2	1 uF
R5	50 kΩ to 300 kΩ

(1) R1 between 3 kΩ and 50 kΩ
R2 between 3 kΩ and 50 kΩ
R1 + R2 parallel value > 2.7 kΩ
C1 > 40 pF

Table 2. C_{PD} (1)

CHIP SECTION	C_{PD}	UNIT
Comparator 1	120	pF
VCO	120	

(1) R1 between 3 kΩ and 50 kΩ
R2 between 3 kΩ and 50 kΩ
R1 + R2 parallel value > 2.7 kΩ
C1 > 40 pF

8.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   – V_{IH} and V_{IL} for each input can be found in *Electrical Characteristics*.
2. Recommended Output Conditions:
   – Valid load resistor values are specified in *Electrical Characteristics*.
3. Frequency Selection Criterion:
   – Frequency data is found in *Electrical Characteristics*.

8.2.3 Application Curves

Table 3 lists the application curves in the *Typical Characteristics* section.

Table 3. Table of Graphs

GRAPH TITLE	FIGURE
Average Output Voltage vs Input Phase Difference	Figure 6
Average Output Voltage vs Input Phase Difference	Figure 7
Average Output Voltage vs Input Phase Difference	Figure 8

9 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage ratings located in the *Recommended Operating Conditions* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply. a 0.1-µF capacitor is recommended and if there are multiple V_{CC} pins then 0.01-µF or 0.022-µF capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

10 Layout

10.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 10 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

10.2 Layout Example

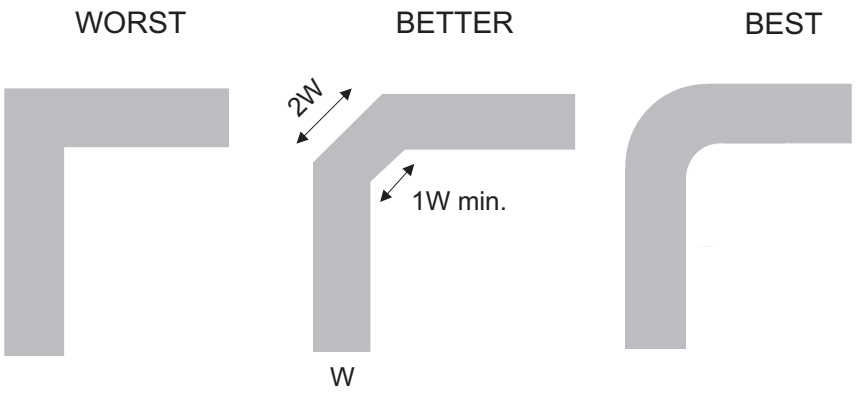


Figure 10. Trace Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

Implications of Slow or Floating CMOS Inputs, SCBA004

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV4046AD	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV4046A	Samples
SN74LV4046ADGVR	ACTIVE	TVSOP	DGV	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW046A	Samples
SN74LV4046ADR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV4046A	Samples
SN74LV4046AN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74LV4046AN	Samples
SN74LV4046ANS	ACTIVE	SO	NS	16	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV4046A	Samples
SN74LV4046ANSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV4046A	Samples
SN74LV4046APW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW046A	Samples
SN74LV4046APWG4	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW046A	Samples
SN74LV4046APWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW046A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

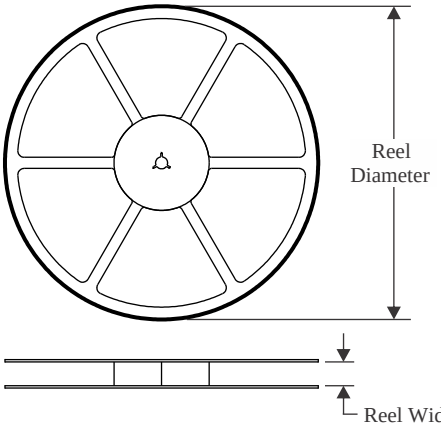
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

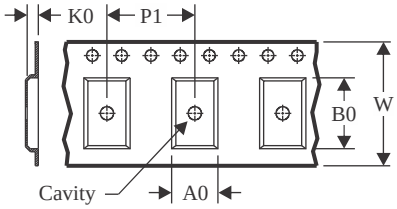
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

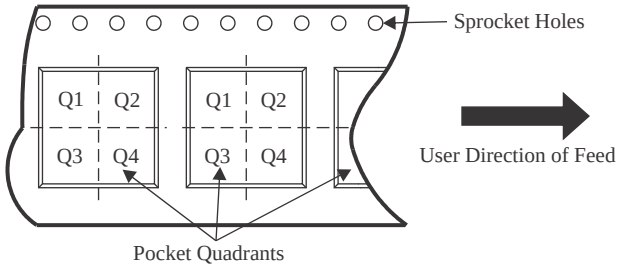


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

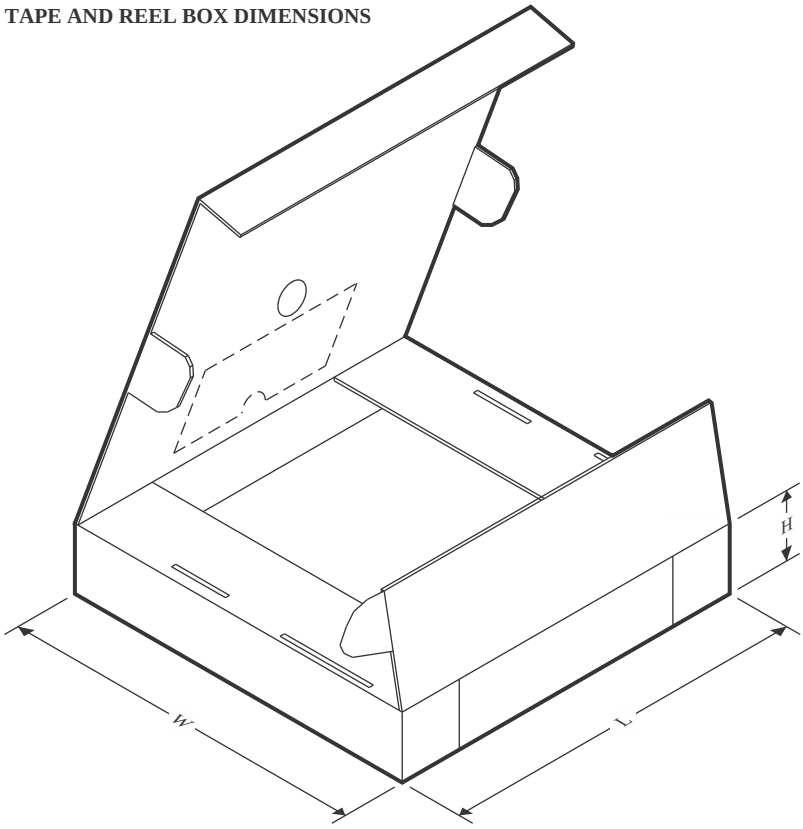
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV4046ADGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV4046ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV4046ANSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LV4046APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

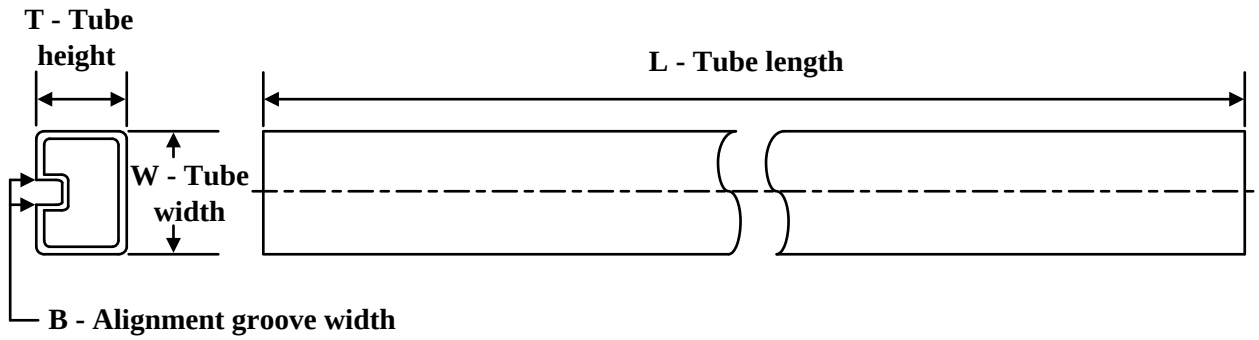
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV4046ADGVR	TVSOP	DGV	16	2000	356.0	356.0	35.0
SN74LV4046ADR	SOIC	D	16	2500	340.5	336.1	32.0
SN74LV4046ANSR	SO	NS	16	2000	356.0	356.0	35.0
SN74LV4046APWR	TSSOP	PW	16	2000	356.0	356.0	35.0

TUBE



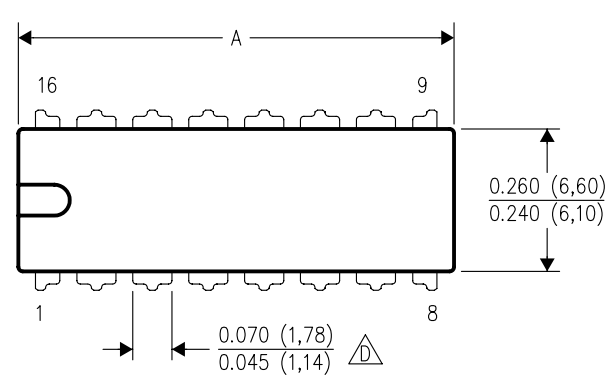
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LV4046AD	D	SOIC	16	40	507	8	3940	4.32
SN74LV4046AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74LV4046AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74LV4046ANS	NS	SOP	16	50	530	10.5	4000	4.1
SN74LV4046APW	PW	TSSOP	16	90	530	10.2	3600	3.5
SN74LV4046APWG4	PW	TSSOP	16	90	530	10.2	3600	3.5

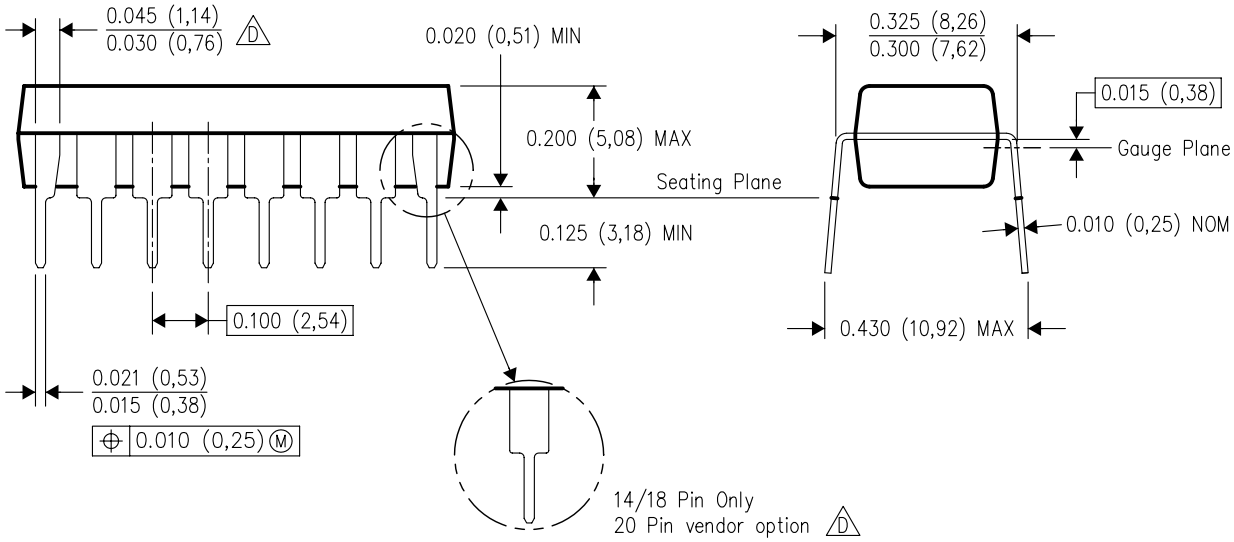
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

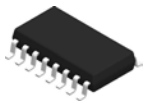


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

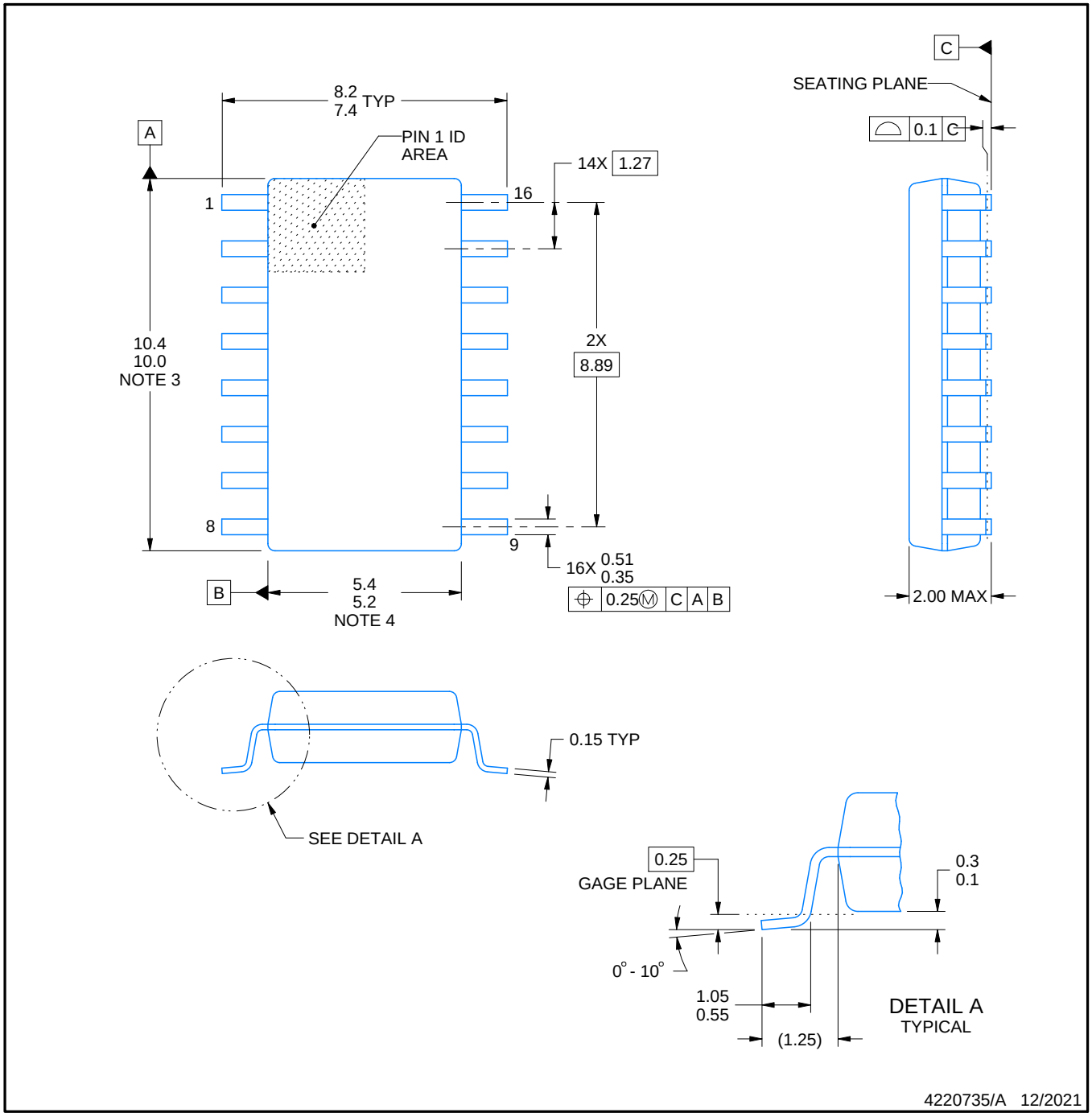


PACKAGE OUTLINE

NS0016A

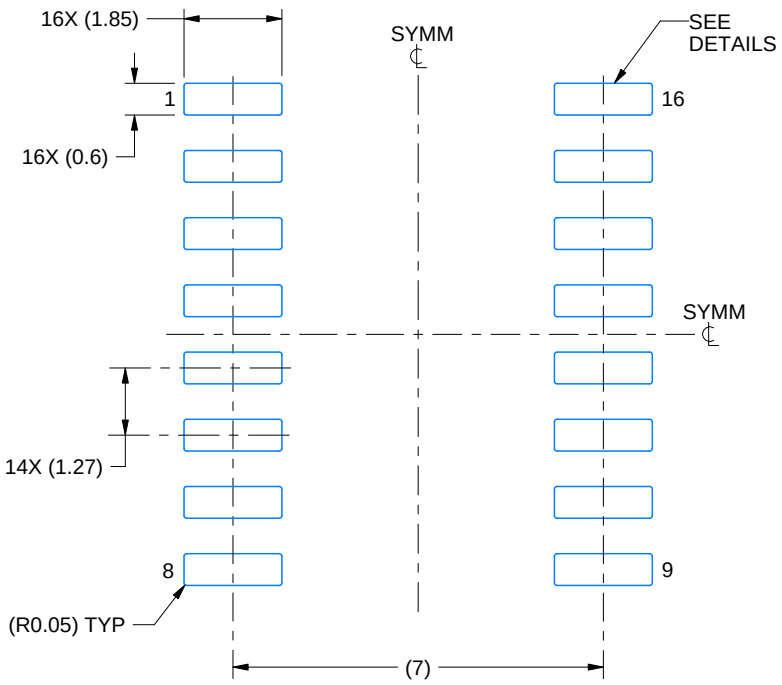
SOP - 2.00 mm max height

SOP

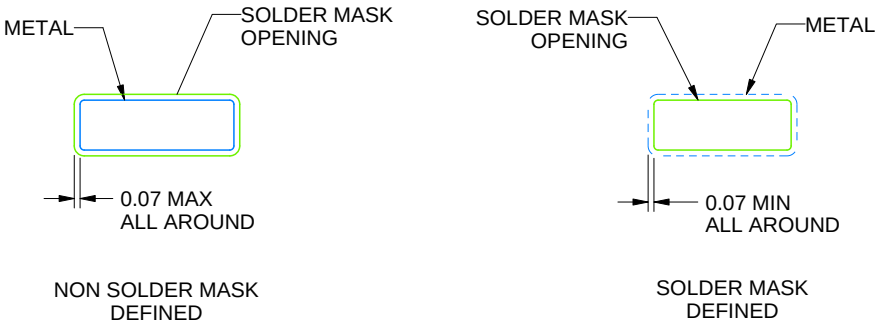


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

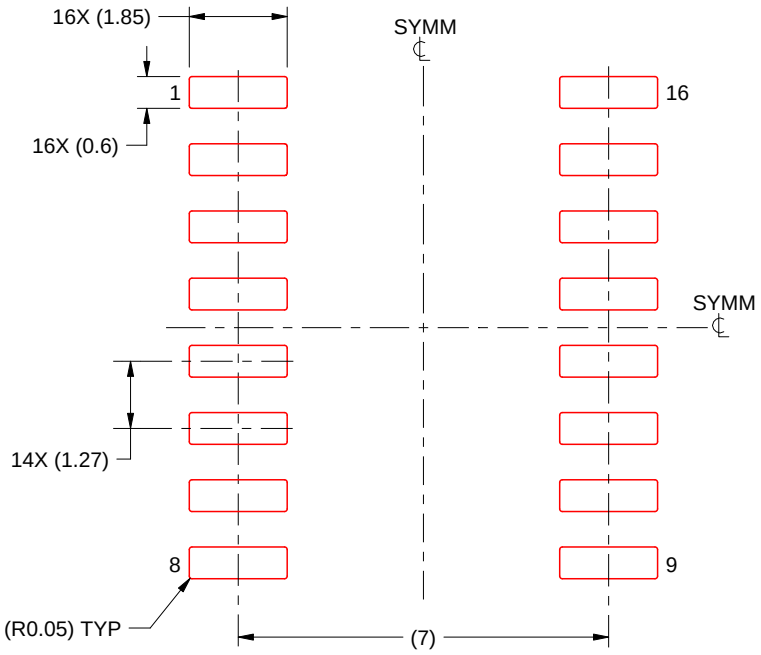
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



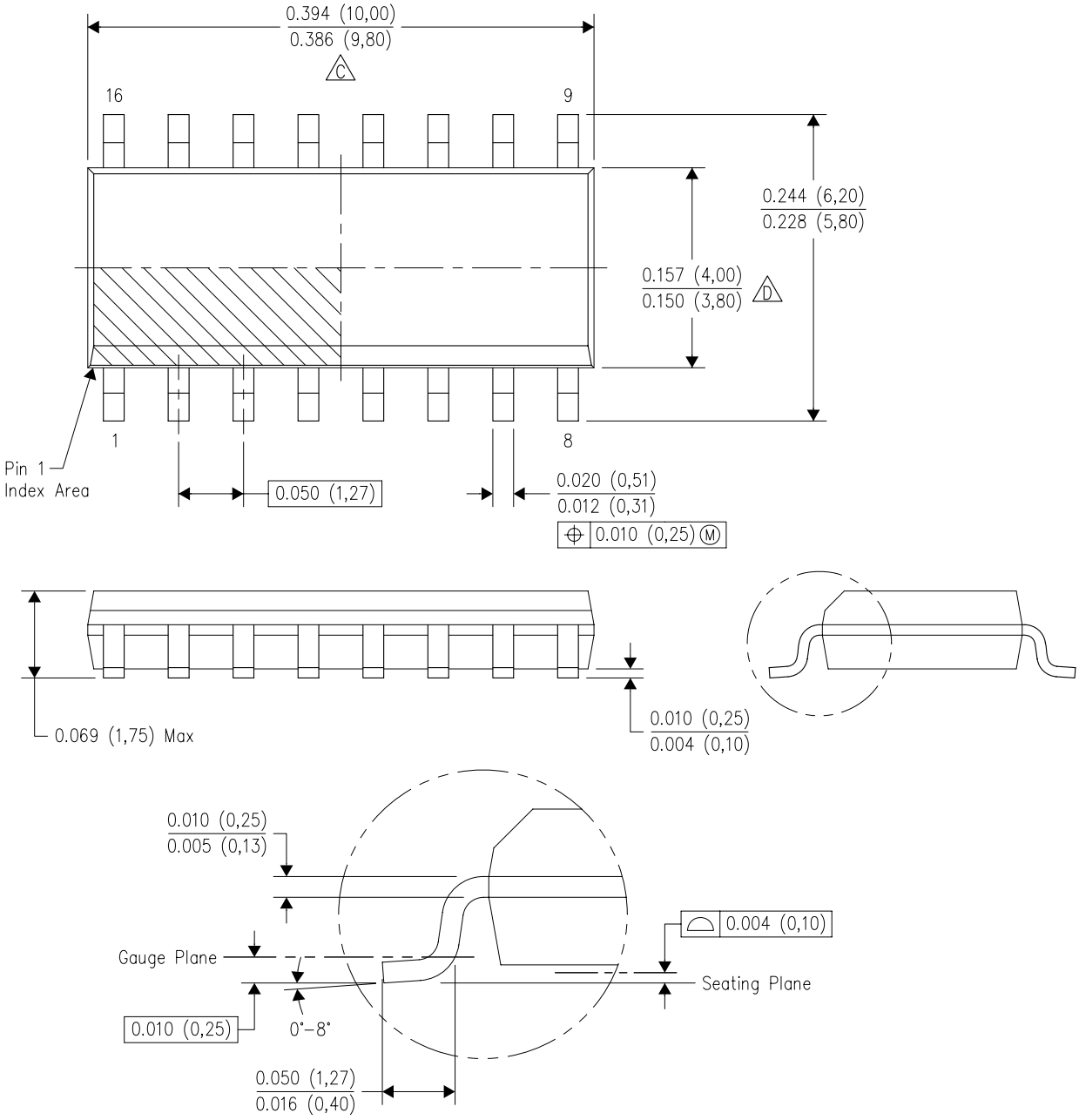
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

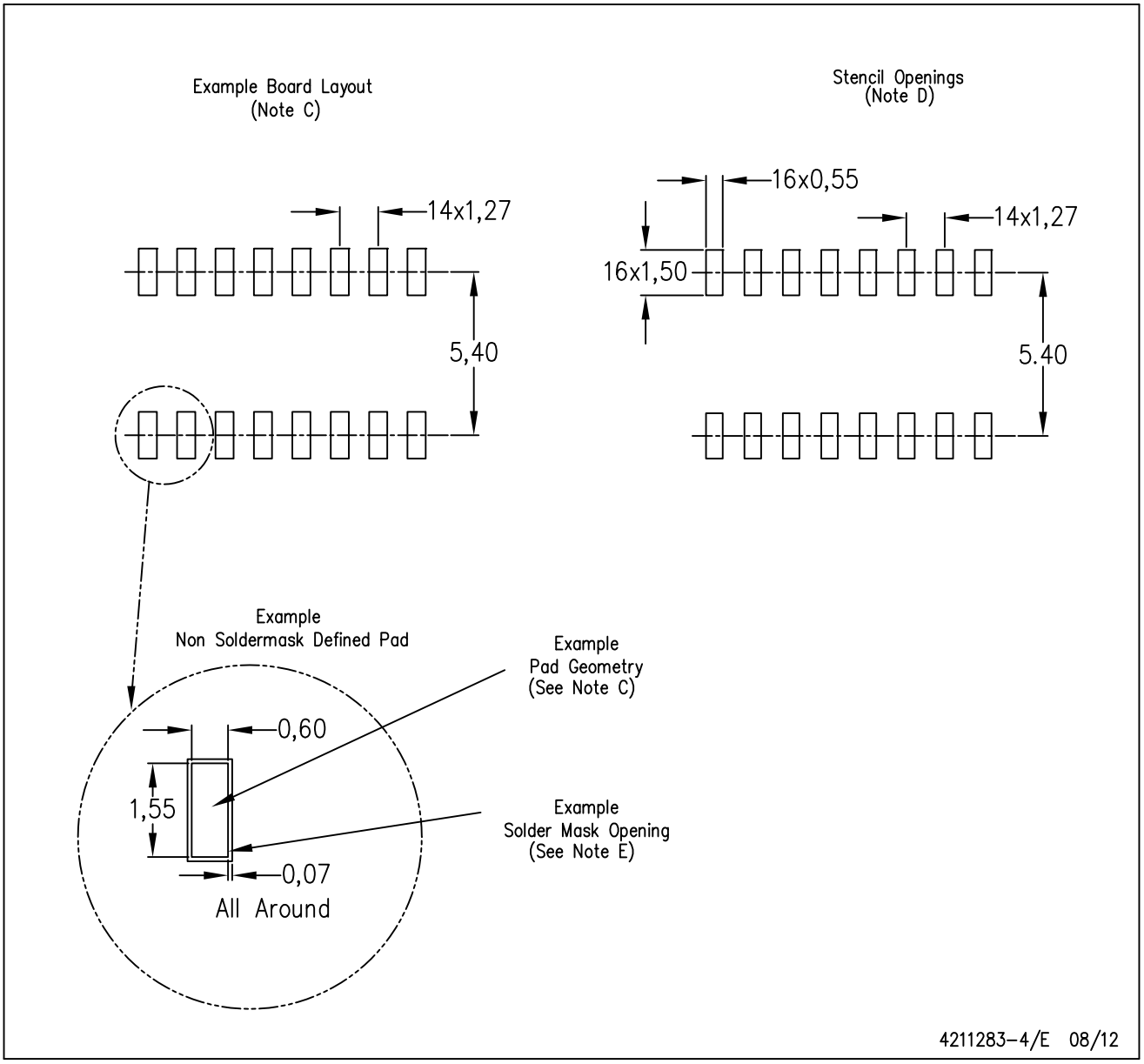
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



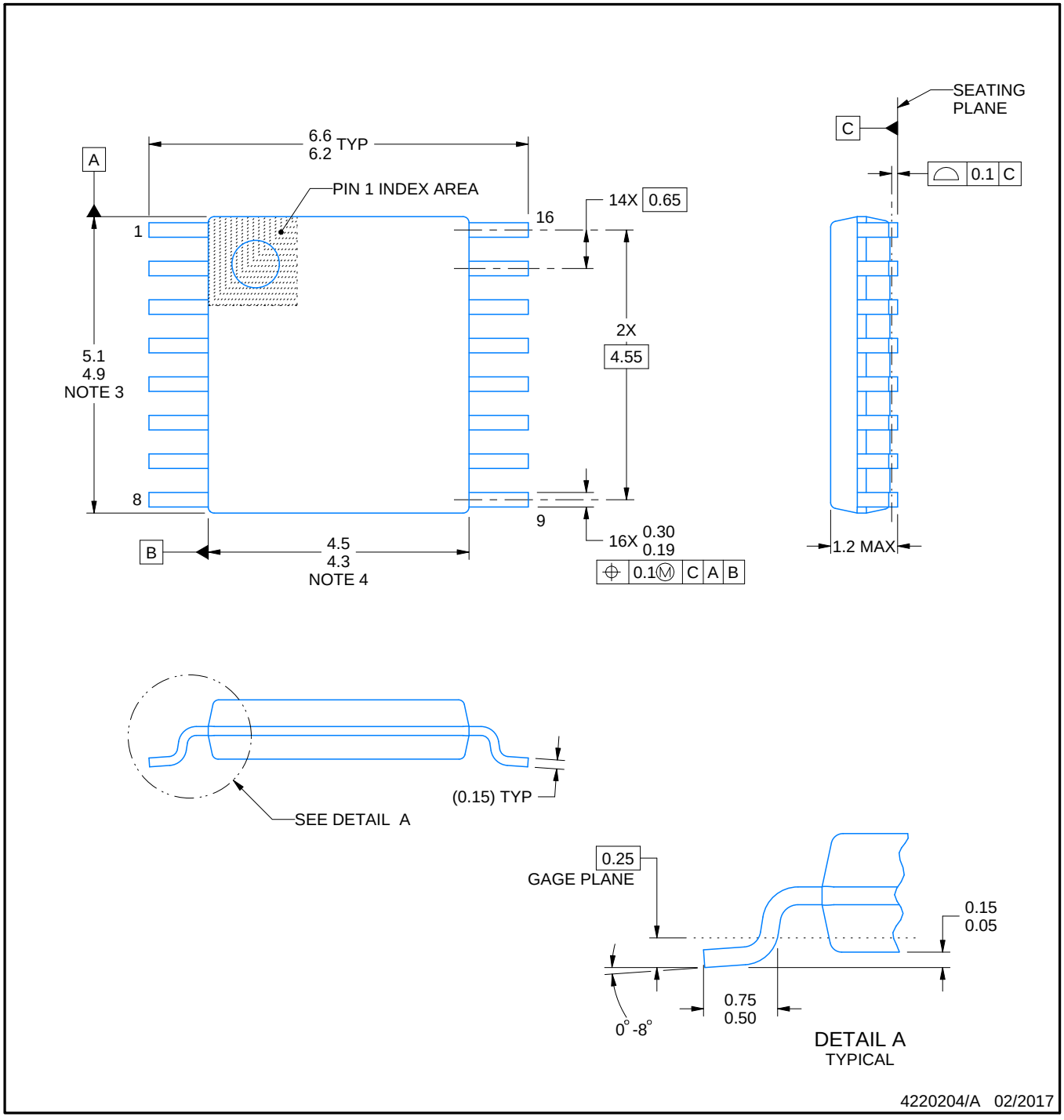
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PW0016A

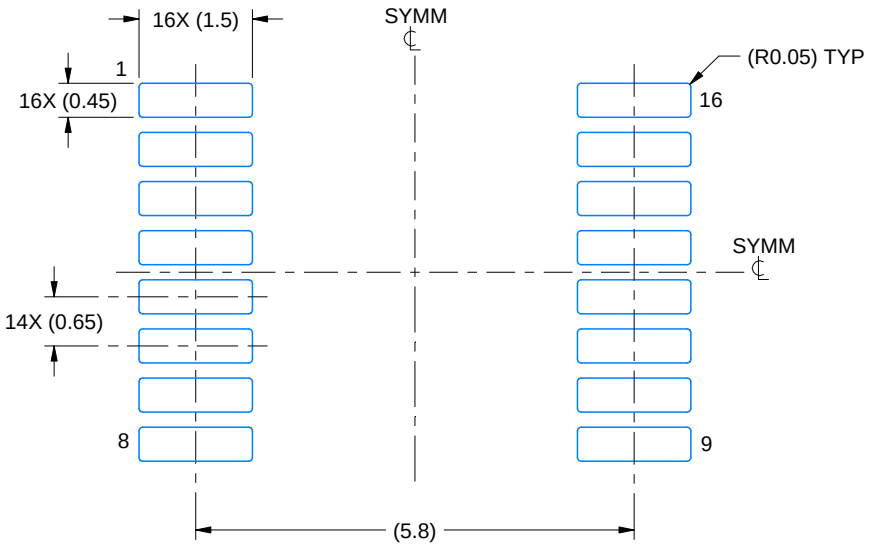
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

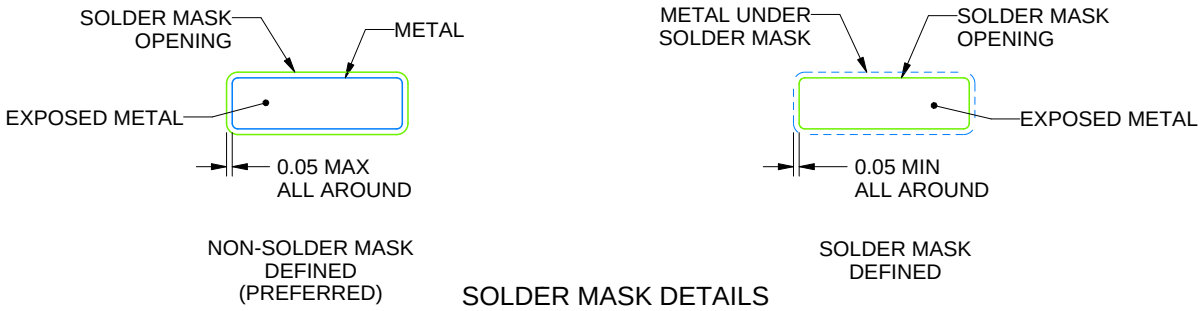


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

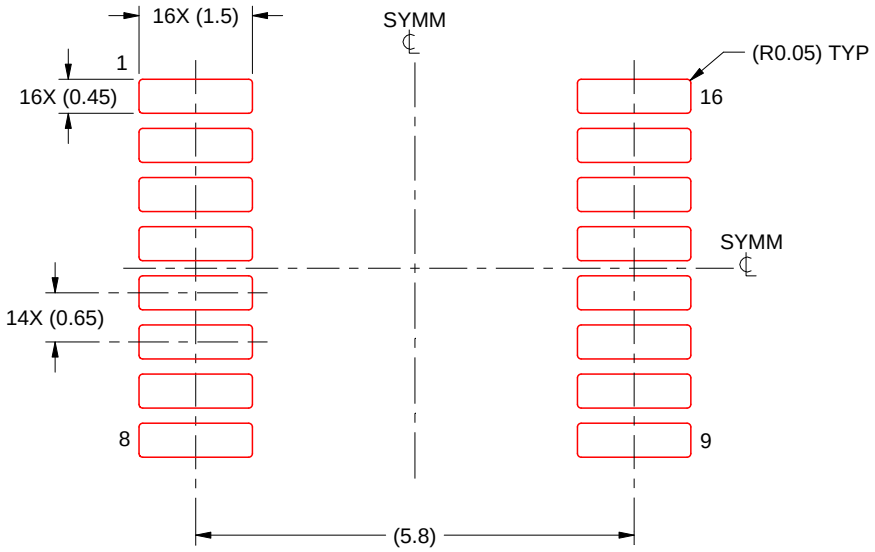


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

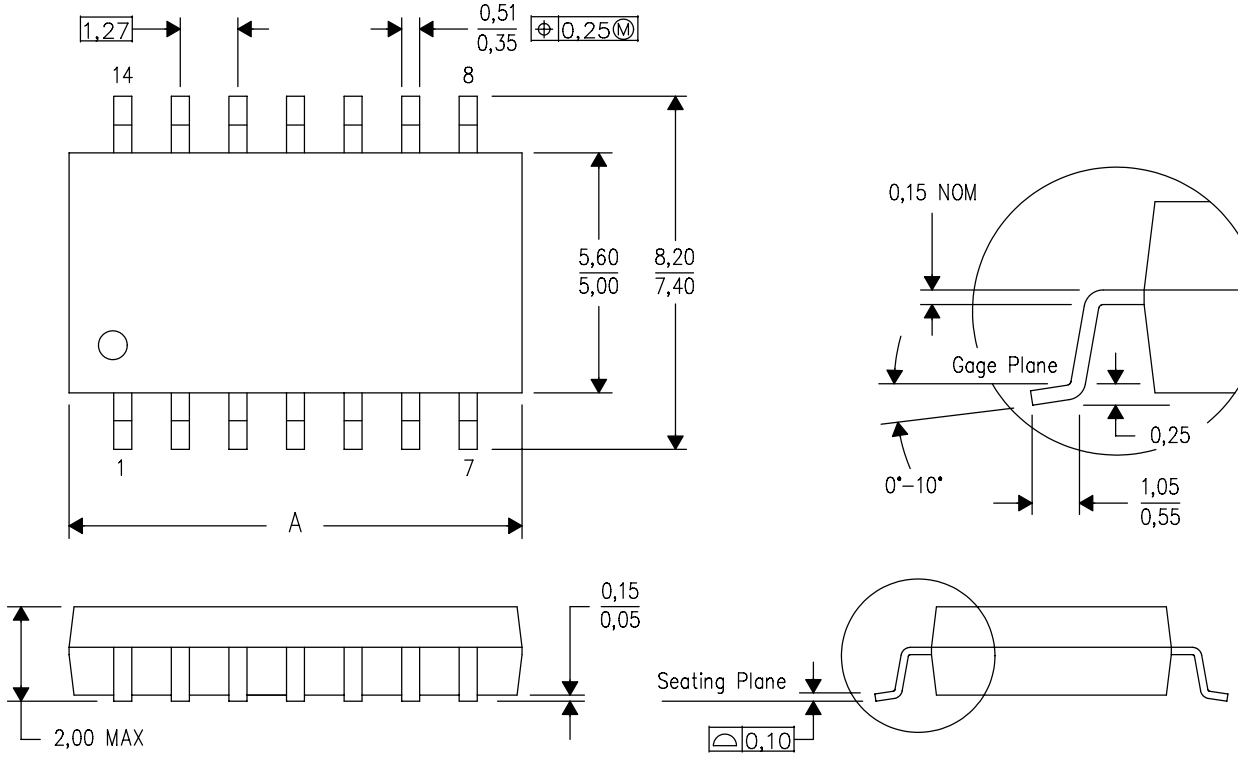
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265