This quadruple silicon-gate CMOS analog switch is designed for 2-V to 5.5-V VCC operation. These switches are designed to handle both analog and digital signals. Each switch permits signals with amplitudes up to 5.5 V (peak) to be transmitted in either direction.

Each switch section has its own enable-input control (C). A high-level voltage applied to C turns on the associated switch section.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

ORDERING INFORMATION

<table>
<thead>
<tr>
<th>TA</th>
<th>PACKAGE†</th>
<th>ORDERABLE PART NUMBER</th>
<th>TOP-SIDE MARKING</th>
</tr>
</thead>
<tbody>
<tr>
<td>-40°C to 85°C</td>
<td>PDIP − N</td>
<td>Tube of 25</td>
<td>SN74LV4066AN</td>
</tr>
<tr>
<td></td>
<td>QFN − RGY</td>
<td>Reel of 1000</td>
<td>SN74LV4066ARGYR</td>
</tr>
<tr>
<td></td>
<td>SOIC − D</td>
<td>Tube of 50</td>
<td>SN74LV4066AD</td>
</tr>
<tr>
<td></td>
<td>Reel of 2500</td>
<td></td>
<td>LV4066A</td>
</tr>
<tr>
<td></td>
<td>SOP − NS</td>
<td>Reel of 2000</td>
<td>SN74LV4066ANSR</td>
</tr>
<tr>
<td></td>
<td>SSOP − DB</td>
<td>Reel of 2000</td>
<td>SN74LV4066ADBR</td>
</tr>
<tr>
<td></td>
<td>TSSOP − PW</td>
<td>Tube of 90</td>
<td>SN74LV4066APW</td>
</tr>
<tr>
<td></td>
<td>Reel of 2000</td>
<td></td>
<td>SN74LV4066APWR</td>
</tr>
<tr>
<td></td>
<td>Reel of 2500</td>
<td></td>
<td>SN74LV4066APWT</td>
</tr>
<tr>
<td></td>
<td>TVSOP − DGV</td>
<td>Reel of 2000</td>
<td>SN74LV4066ADGVR</td>
</tr>
</tbody>
</table>

| -55°C to 125°C | CDIP − J            | Tube of 25            | SNJ54LV4066AJ    |
|                | CFP − W             | Tube of 150           | SNJ54LV4066AW    |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
FUNCTION TABLE
(each switch)

<table>
<thead>
<tr>
<th>INPUT</th>
<th>CONTROL (C)</th>
<th>SWITCH</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>L</td>
<td>OFF</td>
</tr>
<tr>
<td></td>
<td>H</td>
<td>ON</td>
</tr>
</tbody>
</table>

logic diagram (positive logic)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

<table>
<thead>
<tr>
<th>Rating</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage range, $V_{CC}$ (see Note 1)</td>
<td>$-0.5 \text{ V to } 7 \text{ V}$</td>
</tr>
<tr>
<td>Input voltage range, $V_I$ (see Note 1)</td>
<td>$-0.5 \text{ V to } 7 \text{ V}$</td>
</tr>
<tr>
<td>Switch I/O voltage range, $V_{IO}$ (see Notes 1 and 2)</td>
<td>$-0.5 \text{ V to } V_{CC} + 0.5 \text{ V}$</td>
</tr>
<tr>
<td>Control-input clamp current, $I_{IK}$ ($V_I &lt; 0$)</td>
<td>$-20 \text{ mA}$</td>
</tr>
<tr>
<td>I/O diode current, $I_{IOK}$ ($V_{IO} &lt; 0$)</td>
<td>$-50 \text{ mA}$</td>
</tr>
<tr>
<td>On-state switch current, $I_T$ ($V_{IO} = 0$ to $V_{CC}$)</td>
<td>$225 \text{ mA}$</td>
</tr>
<tr>
<td>Continuous current through $V_{CC}$ or GND</td>
<td>$\pm 50 \text{ mA}$</td>
</tr>
<tr>
<td>Package thermal impedance, $\theta_{JA}$ (see Note 3): D package</td>
<td>$86^\circ \text{C/W}$</td>
</tr>
<tr>
<td>(see Note 3): DB package</td>
<td>$96^\circ \text{C/W}$</td>
</tr>
<tr>
<td>(see Note 3): DGV package</td>
<td>$127^\circ \text{C/W}$</td>
</tr>
<tr>
<td>(see Note 3): N package</td>
<td>$80^\circ \text{C/W}$</td>
</tr>
<tr>
<td>(see Note 3): NS package</td>
<td>$76^\circ \text{C/W}$</td>
</tr>
<tr>
<td>(see Note 3): PW package</td>
<td>$113^\circ \text{C/W}$</td>
</tr>
<tr>
<td>(see Note 4): RGY package</td>
<td>$47^\circ \text{C/W}$</td>
</tr>
<tr>
<td>Storage temperature range, $T_{stg}$</td>
<td>$-65^\circ \text{C to } 150^\circ \text{C}$</td>
</tr>
</tbody>
</table>

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.
4. The package thermal impedance is calculated in accordance with JESD 51-5.
<table>
<thead>
<tr>
<th>Parameter</th>
<th>SN54LV4066A</th>
<th>SN74LV4066A</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>VCC</strong> (Supply voltage)</td>
<td>2† max. 5.5</td>
<td>2† max. 5.5</td>
<td>V</td>
</tr>
<tr>
<td><strong>V_{IH}</strong> (High-level input voltage, control inputs)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{CC} = 2$ V</td>
<td>1.5</td>
<td>1.5</td>
<td>V</td>
</tr>
<tr>
<td>$V_{CC} = 2.3$ V to $2.7$ V</td>
<td>$V_{CC} \times 0.7$</td>
<td>$V_{CC} \times 0.7$</td>
<td></td>
</tr>
<tr>
<td>$V_{CC} = 3$ V to $3.6$ V</td>
<td>$V_{CC} \times 0.7$</td>
<td>$V_{CC} \times 0.7$</td>
<td></td>
</tr>
<tr>
<td>$V_{CC} = 4.5$ V to $5.5$ V</td>
<td>$V_{CC} \times 0.7$</td>
<td>$V_{CC} \times 0.7$</td>
<td></td>
</tr>
<tr>
<td><strong>V_{IL}</strong> (Low-level input voltage, control inputs)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{CC} = 2$ V</td>
<td>0</td>
<td>0.5</td>
<td>V</td>
</tr>
<tr>
<td>$V_{CC} = 2.3$ V to $2.7$ V</td>
<td>$V_{CC} \times 0.3$</td>
<td>$V_{CC} \times 0.3$</td>
<td></td>
</tr>
<tr>
<td>$V_{CC} = 3$ V to $3.6$ V</td>
<td>$V_{CC} \times 0.3$</td>
<td>$V_{CC} \times 0.3$</td>
<td></td>
</tr>
<tr>
<td>$V_{CC} = 4.5$ V to $5.5$ V</td>
<td>$V_{CC} \times 0.3$</td>
<td>$V_{CC} \times 0.3$</td>
<td></td>
</tr>
<tr>
<td><strong>V_{I}</strong> (Control input voltage)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{CC} = 2.3$ V to $2.7$ V</td>
<td>0</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>$V_{CC} = 3$ V to $3.6$ V</td>
<td>$V_{CC}$</td>
<td>0</td>
<td>V</td>
</tr>
<tr>
<td>$V_{CC} = 4.5$ V to $5.5$ V</td>
<td>0</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td><strong>V_{IO}</strong> (Input/output voltage)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{CC} = 2.3$ V to $2.7$ V</td>
<td>0</td>
<td>200</td>
<td>ns/V</td>
</tr>
<tr>
<td>$V_{CC} = 3$ V to $3.6$ V</td>
<td>$V_{CC}$</td>
<td>0</td>
<td>V</td>
</tr>
<tr>
<td>$V_{CC} = 4.5$ V to $5.5$ V</td>
<td>0</td>
<td>100</td>
<td>ns/V</td>
</tr>
<tr>
<td><strong>$\Delta t/\Delta v$</strong> (Input transition rise or fall rate)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{CC} = 2.3$ V to $2.7$ V</td>
<td>200</td>
<td></td>
<td>ns/V</td>
</tr>
<tr>
<td>$V_{CC} = 3$ V to $3.6$ V</td>
<td>100</td>
<td></td>
<td>ns/V</td>
</tr>
<tr>
<td>$V_{CC} = 4.5$ V to $5.5$ V</td>
<td>20</td>
<td></td>
<td>ns/V</td>
</tr>
<tr>
<td><strong>T_{A}</strong> (Operating free-air temperature)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{CC} = 2.3$ V to $2.7$ V</td>
<td>-55</td>
<td>125</td>
<td>°C</td>
</tr>
<tr>
<td>$V_{CC} = 3$ V to $3.6$ V</td>
<td>-40</td>
<td>85</td>
<td>°C</td>
</tr>
<tr>
<td>$V_{CC} = 4.5$ V to $5.5$ V</td>
<td>20</td>
<td>20</td>
<td>°C</td>
</tr>
</tbody>
</table>

† With supply voltages at or near 2 V, the analog switch on-state resistance becomes very nonlinear. Only digital signals should be transmitted at these low supply voltages.

**NOTE 5:** All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>$V_{CC}$</th>
<th>$T_A = 25^\circ C$</th>
<th>SN54LV4066A</th>
<th>SN74LV4066A</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>MIN</td>
<td>TYP</td>
<td>MAX</td>
<td>MIN</td>
<td>MAX</td>
</tr>
<tr>
<td>$r_{on}$</td>
<td>On-state switch resistance</td>
<td>$I_T = -1 \ mA,$</td>
<td>2.3 V</td>
<td>38</td>
<td>180</td>
<td>225</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_I = V_{CC}$ or GND, $V_C = V_{IL}$</td>
<td>3 V</td>
<td>29</td>
<td>150</td>
<td>190</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_C = V_{IH}$</td>
<td>4.5 V</td>
<td>21</td>
<td>75</td>
<td>100</td>
</tr>
<tr>
<td>$r_{on(p)}$</td>
<td>Peak on-state resistance</td>
<td>$I_T = -1 \ mA,$</td>
<td>2.3 V</td>
<td>143</td>
<td>500</td>
<td>600</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_I = V_{CC}$ to GND, $V_C = V_{IH}$</td>
<td>3 V</td>
<td>57</td>
<td>180</td>
<td>225</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>4.5 V</td>
<td>31</td>
<td>100</td>
<td>125</td>
</tr>
<tr>
<td>$\Delta r_{on}$</td>
<td>Difference in on-state resistance between switches</td>
<td>$I_T = -1 \ mA,$</td>
<td>2.3 V</td>
<td>6</td>
<td>30</td>
<td>40</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_I = V_{CC}$ to GND, $V_C = V_{IH}$</td>
<td>3 V</td>
<td>3</td>
<td>20</td>
<td>30</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>4.5 V</td>
<td>2</td>
<td>15</td>
<td>20</td>
</tr>
<tr>
<td>$I_I$</td>
<td>Control input current</td>
<td>$V_I = 5.5 \ V$ or GND</td>
<td>0 to 5.5 V</td>
<td>±0.1</td>
<td>±1</td>
<td>±1</td>
</tr>
<tr>
<td>$I_{S(off)}$</td>
<td>Off-state switch leakage current</td>
<td>$V_I = V_{CC}$ and $V_O = GND,$ or $V_I = GND$ and $V_O = V_{CC},$ $V_C = V_{IL}$ (see Figure 2)</td>
<td>5.5 V</td>
<td>±0.1</td>
<td>±1</td>
<td>±1</td>
</tr>
<tr>
<td>$I_{S(on)}$</td>
<td>On-state switch leakage current</td>
<td>$V_I = V_{CC}$ or GND, $V_C = V_{IH}$ (see Figure 3)</td>
<td>5.5 V</td>
<td>±0.1</td>
<td>±1</td>
<td>±1</td>
</tr>
<tr>
<td>$I_{CC}$</td>
<td>Supply current</td>
<td>$V_I = V_{CC}$ or GND</td>
<td>5.5 V</td>
<td>20</td>
<td>20</td>
<td>20</td>
</tr>
<tr>
<td>$C_{IC}$</td>
<td>Control input capacitance</td>
<td></td>
<td></td>
<td></td>
<td>1.5</td>
<td></td>
</tr>
<tr>
<td>$C_{IO}$</td>
<td>Switch input/output capacitance</td>
<td></td>
<td></td>
<td></td>
<td>5.5</td>
<td></td>
</tr>
<tr>
<td>$C_{F}$</td>
<td>Feed-through capacitance</td>
<td></td>
<td></td>
<td></td>
<td>0.5</td>
<td></td>
</tr>
</tbody>
</table>

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.
switching characteristics over recommended operating free-air temperature range, $V_{CC} = 2.5 \, V \pm 0.2 \, V$ (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>TEST CONDITIONS</th>
<th>$T_A = 25^\circ C$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>MIN</td>
<td>TYP</td>
<td>MAX</td>
<td>SN54LV4066A</td>
</tr>
<tr>
<td>$\tau_{PLH}$</td>
<td>$\tau_{PHL}$</td>
<td>Propagation delay time</td>
<td>A or B</td>
<td>B or A</td>
</tr>
<tr>
<td>$\tau_{PZH}$</td>
<td>$\tau_{PZL}$</td>
<td>Switch turn-on time</td>
<td>C</td>
<td>A or B</td>
</tr>
<tr>
<td>$\tau_{PLZ}$</td>
<td>$\tau_{PHZ}$</td>
<td>Switch turn-off time</td>
<td>C</td>
<td>A or B</td>
</tr>
</tbody>
</table>

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 3.3 \, V \pm 0.3 \, V$ (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>TEST CONDITIONS</th>
<th>$T_A = 25^\circ C$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>MIN</td>
<td>TYP</td>
<td>MAX</td>
<td>SN54LV4066A</td>
</tr>
<tr>
<td>$\tau_{PLH}$</td>
<td>$\tau_{PHL}$</td>
<td>Propagation delay time</td>
<td>A or B</td>
<td>B or A</td>
</tr>
<tr>
<td>$\tau_{PZH}$</td>
<td>$\tau_{PZL}$</td>
<td>Switch turn-on time</td>
<td>C</td>
<td>A or B</td>
</tr>
<tr>
<td>$\tau_{PLZ}$</td>
<td>$\tau_{PHZ}$</td>
<td>Switch turn-off time</td>
<td>C</td>
<td>A or B</td>
</tr>
<tr>
<td>$\tau_{PLH}$</td>
<td>$\tau_{PHL}$</td>
<td>Propagation delay time</td>
<td>A or B</td>
<td>B or A</td>
</tr>
<tr>
<td>$\tau_{PZH}$</td>
<td>$\tau_{PZL}$</td>
<td>Switch turn-on time</td>
<td>C</td>
<td>A or B</td>
</tr>
<tr>
<td>$\tau_{PLZ}$</td>
<td>$\tau_{PHZ}$</td>
<td>Switch turn-off time</td>
<td>C</td>
<td>A or B</td>
</tr>
</tbody>
</table>
switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5\, \text{V} \pm 0.5\, \text{V}$ (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>TEST CONDITIONS</th>
<th>$T_A = 25^\circ\text{C}$</th>
<th>SN54LV4066A</th>
<th>SN74LV4066A</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{PLH}$</td>
<td>A or B</td>
<td>B or A</td>
<td>$C_L = 15, \text{pF}$ (see Figure 4)</td>
<td>0.3</td>
<td>4</td>
<td>7</td>
<td>7</td>
</tr>
<tr>
<td>$t_{PHL}$</td>
<td>C</td>
<td>A or B</td>
<td>$C_L = 15, \text{pF}$, $R_L = 1, \text{k}\Omega$ (see Figure 5)</td>
<td>1.6</td>
<td>7</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>$t_{PLZ}$</td>
<td>C</td>
<td>A or B</td>
<td>$C_L = 15, \text{pF}$, $R_L = 1, \text{k}\Omega$ (see Figure 5)</td>
<td>3.2</td>
<td>7</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>$t_{PHZ}$</td>
<td>A or B</td>
<td>B or A</td>
<td>$C_L = 50, \text{pF}$ (see Figure 4)</td>
<td>0.6</td>
<td>6</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>$t_{PZH}$</td>
<td>C</td>
<td>A or B</td>
<td>$C_L = 50, \text{pF}$, $R_L = 1, \text{k}\Omega$ (see Figure 5)</td>
<td>2.1</td>
<td>12</td>
<td>16</td>
<td>16</td>
</tr>
<tr>
<td>$t_{PLZ}$</td>
<td>C</td>
<td>A or B</td>
<td>$C_L = 50, \text{pF}$, $R_L = 1, \text{k}\Omega$ (see Figure 5)</td>
<td>5.1</td>
<td>12</td>
<td>16</td>
<td>16</td>
</tr>
</tbody>
</table>

analog switch characteristics over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>TEST CONDITIONS</th>
<th>$V_{CC}$</th>
<th>$T_A = 25^\circ\text{C}$</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency response</td>
<td>A or B</td>
<td>B or A</td>
<td>$C_L = 50, \text{pF}$, $R_L = 600, \Omega$, $f_{in} = 1, \text{MHz}$ (sine wave) $20\log_{10}(V_O/V_I) = -3, \text{dB}$ (see Figure 6)</td>
<td>2.3 V</td>
<td>30</td>
<td>MHz</td>
</tr>
<tr>
<td>Crosstalk between any switches</td>
<td>A or B</td>
<td>B or A</td>
<td>$C_L = 50, \text{pF}$, $R_L = 600, \Omega$, $f_{in} = 1, \text{MHz}$ (sine wave) (see Figure 7)</td>
<td>2.3 V</td>
<td>-45</td>
<td>dB</td>
</tr>
<tr>
<td>Crosstalk control input to signal output</td>
<td>C</td>
<td>A or B</td>
<td>$C_L = 50, \text{pF}$, $R_L = 600, \Omega$, $f_{in} = 1, \text{MHz}$ (square wave) (see Figure 8)</td>
<td>2.3 V</td>
<td>15</td>
<td>mV</td>
</tr>
<tr>
<td>Feed-through attenuation (switch off)</td>
<td>A or B</td>
<td>B or A</td>
<td>$C_L = 50, \text{pF}$, $R_L = 600, \Omega$, $f_{in} = 1, \text{MHz}$ (see Figure 9)</td>
<td>2.3 V</td>
<td>-40</td>
<td>dB</td>
</tr>
<tr>
<td>Sine-wave distortion</td>
<td>A or B</td>
<td>B or A</td>
<td>$C_L = 50, \text{pF}$, $R_L = 10, \text{k}\Omega$, $f_{in} = 1, \text{kHz}$ (sine wave) (see Figure 10) $V_I = 2, V_{pp}$</td>
<td>2.3 V</td>
<td>0.1</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$V_I = 2.5, V_{pp}$</td>
<td>3 V</td>
<td>0.1</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$V_I = 4, V_{pp}$</td>
<td>4.5 V</td>
<td>0.1</td>
<td></td>
</tr>
</tbody>
</table>

operating characteristics, $T_A = 25^\circ\text{C}$

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>TYP</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{pd}$</td>
<td>$C_L = 50, \text{pF}$, $f = 10, \text{MHz}$</td>
<td>4.5</td>
<td>pF</td>
</tr>
</tbody>
</table>
PARAMETER MEASUREMENT INFORMATION

\[ r_{on} = \frac{V_I - V_O}{10^{-3}} \Omega \]

Figure 1. On-State Resistance Test Circuit

Condition 1: \( V_I = 0, V_O = V_{CC} \)
Condition 2: \( V_I = V_{CC}, V_O = 0 \)

Figure 2. Off-State Switch Leakage-Current Test Circuit

Figure 3. On-State Leakage-Current Test Circuit
PARAMETER MEASUREMENT INFORMATION

VCC

$V_C = V_{IH}$

$V_I$

50 Ω

50% 50%

$V_{OL}$

$V_O$

GND

TEST CIRCUIT

$V_{OH}$

$V_{CC}$

10%

90%

0 V

50%

90%

10%

10%

$t_{PLH}$

$t_{PHL}$

$V_I$

A or B

$V_O$

B or A

$V_{PLH}$

$V_{OH}$

$V_{OL}$

$V_{CC}$

$t_{PHL}$

$V_{CC}$

0 V

50% 50%

$V_{OL}$

$V_O$

B or A

$V_{OH}$

$V_{OL}$

$V_{CC}$

$t_{PHL}$

$V_{CC}$

0 V

$V_{OL}$

$V_O$

B or A

$V_{OH}$

$V_{OL}$

$V_{CC}$

50% 50%

$V_{OL}$

$V_O$

B or A

$V_{OH}$

$V_{OL}$

$V_{CC}$

50% 50%

$V_{OL}$

$V_O$

B or A

$V_{OH}$

$V_{OL}$

$V_{CC}$

50% 50%

$V_{OL}$

$V_O$

B or A

$V_{OH}$

$V_{OL}$

$V_{CC}$

50% 50%

$V_{OL}$

$V_O$

B or A

$V_{OH}$

$V_{OL}$

$V_{CC}$

50% 50%

$V_{OL}$

$V_O$

B or A

$V_{OH}$

$V_{OL}$

$V_{CC}$

50% 50%

$V_{OL}$

$V_O$

B or A

$V_{OH}$

$V_{OL}$

$V_{CC}$

50% 50%

$V_{OL}$

$V_O$

B or A

$V_{OH}$

$V_{OL}$

$V_{CC}$

50% 50%

$V_{OL}$

$V_O$

B or A

$V_{OH}$

$V_{OL}$

$V_{CC}$

50% 50%

$V_{OL}$

$V_O$

B or A

$V_{OH}$

$V_{OL}$

$V_{CC}$

50% 50%

$V_{OL}$

$V_O$

B or A

$V_{OH}$

$V_{OL}$

$V_{CC}$

50% 50%

$V_{OL}$

$V_O$

B or A

$V_{OH}$

$V_{OL}$

$V_{CC}$

50% 50%

$V_{OL}$

$V_O$

B or A

$V_{OH}$

$V_{OL}$

$V_{CC}$

50% 50%

$V_{OL}$

$V_O$

B or A

$V_{OH}$

$V_{OL}$

$V_{CC}$

50% 50%

$V_{OL}$

$V_O$

B or A

$V_{OH}$

$V_{OL}$

$V_{CC}$

50% 50%

$V_{OL}$

$V_O$

B or A

$V_{OH}$

$V_{OL}$

$V_{CC}$

50% 50%

$V_{OL}$

$V_O$

B or A

$V_{OH}$

$V_{OL}$

$V_{CC}$

50% 50%

$V_{OL}$

$V_O$

B or A

$V_{OH}$

$V_{OL}$

$V_{CC}$

50% 50%

$V_{OL}$

$V_O$

B or A

$V_{OH}$

$V_{OL}$

$V_{CC}$

50% 50%

$V_{OL}$

$V_O$

B or A

$V_{OH}$

$V_{OL}$

$V_{CC}$

50% 50%

$V_{OL}$

$V_O$

B or A

$V_{OH}$

$V_{OL}$

$V_{CC}$

50% 50%

$V_{OL}$

$V_O$

B or A

$V_{OH}$

$V_{OL}$

$V_{CC}$

50% 50%

$V_{OL}$

$V_O$

B or A

$V_{OH}$

$V_{OL}$

$V_{CC}$

50% 50%

$V_{OL}$

$V_O$

B or A

$V_{OH}$

$V_{OL}$

$V_{CC}$

50% 50%

$V_{OL}$

$V_O$

B or A

$V_{OH}$

$V_{OL}$

$V_{CC}$

50% 50%

$V_{OL}$

$V_O$

B or A

$V_{OH}$

$V_{OL}$

$V_{CC}$

50% 50%

$V_{OL}$

$V_O$

B or A

$V_{OH}$

$V_{OL}$

$V_{CC}$

50% 50%

$V_{OL}$

$V_O$

B or A

$V_{OH}$

$V_{OL}$

$V_{CC}$

50% 50%

$V_{OL}$

$V_O$

B or A

$V_{OH}$

$V_{OL}$

$V_{CC}$

50% 50%

$V_{OL}$

$V_O$

B or A

$V_{OH}$

$V_{OL}$

$V_{CC}$

50% 50%

$V_{OL}$

$V_O$

B or A

$V_{OH}$

$V_{OL}$

$V_{CC}$

50% 50%

$V_{OL}$

$V_O$

B or A

$V_{OH}$

$V_{OL}$

$V_{CC}$

50% 50%

$V_{OL}$

$V_O$

B or A

$V_{OH}$

$V_{OL}$

$V_{CC}$

50% 50%

$V_{OL}$

$V_O$

B or A

$V_{OH}$

$V_{OL}$

$V_{CC}$

50% 50%

$V_{OL}$

$V_O$

B or A

$V_{OH}$

$V_{OL}$

$V_{CC}$

50% 50%

$V_{OL}$

$V_O$

B or A

$V_{OH}$

$V_{OL}$

$V_{CC}$

50% 50%

$V_{OL}$

$V_O$

B or A

$V_{OH}$

$V_{OL}$

$V_{CC}$

50% 50%

$V_{OL}$

$V_O$

B or A

$V_{OH}$

$V_{OL}$

$V_{CC}$

50% 50%

$V_{OL}$

$V_O$ Figure 4. Propagation Delay Time, Signal Input to Signal Output
PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT

<table>
<thead>
<tr>
<th>TEST</th>
<th>S1</th>
<th>S2</th>
</tr>
</thead>
<tbody>
<tr>
<td>tPZL</td>
<td>GND</td>
<td>VCC</td>
</tr>
<tr>
<td>tPZH</td>
<td>VCC</td>
<td>GND</td>
</tr>
<tr>
<td>tPLZ</td>
<td>GND</td>
<td>VCC</td>
</tr>
<tr>
<td>tPHZ</td>
<td>VCC</td>
<td>GND</td>
</tr>
</tbody>
</table>

VOLTAGE WAVEFORMS

Figure 5. Switching Time (tPZL, tPLZ, tPZH, tPHZ), Control to Signal Output
PARAMETER MEASUREMENT INFORMATION

Figure 6. Frequency Response (Switch On)

Figure 7. Crosstalk Between Any Two Switches

Figure 8. Crosstalk (Control Input – Switch Output)
PARAMETER MEASUREMENT INFORMATION

Figure 9. Feed-Through Attenuation (Switch Off)

Figure 10. Sine-Wave Distortion
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead finish/ Ball material</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN74LV4066AD</td>
<td>LIFEBUY</td>
<td>SOIC</td>
<td>D</td>
<td>14</td>
<td>50</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>LV4066A</td>
<td></td>
</tr>
<tr>
<td>SN74LV4066ADBR</td>
<td>LIFEBUY</td>
<td>SSOP</td>
<td>DB</td>
<td>14</td>
<td>2000</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>LW066A</td>
<td></td>
</tr>
<tr>
<td>SN74LV4066ADGVR</td>
<td>LIFEBUY</td>
<td>TVSOP</td>
<td>DGV</td>
<td>14</td>
<td>2000</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>LW066A</td>
<td></td>
</tr>
<tr>
<td>SN74LV4066ADR</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>14</td>
<td>2500</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>LV4066A</td>
<td></td>
</tr>
<tr>
<td>SN74LV4066AN</td>
<td>LIFEBUY</td>
<td>PDIP</td>
<td>N</td>
<td>14</td>
<td>25</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>N / A for Pkg Type</td>
<td>-40 to 85</td>
<td>SN74LV4066AN</td>
<td></td>
</tr>
<tr>
<td>SN74LV4066ANSR</td>
<td>LIFEBUY</td>
<td>SO</td>
<td>NS</td>
<td>14</td>
<td>2000</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>74LV4066A</td>
<td></td>
</tr>
<tr>
<td>SN74LV4066APW</td>
<td>LIFEBUY</td>
<td>TSSOP</td>
<td>PW</td>
<td>14</td>
<td>90</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>LW066A</td>
<td></td>
</tr>
<tr>
<td>SN74LV4066APWR</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>PW</td>
<td>14</td>
<td>2000</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>LW066A</td>
<td></td>
</tr>
<tr>
<td>SN74LV4066APWT</td>
<td>LIFEBUY</td>
<td>TSSOP</td>
<td>PW</td>
<td>14</td>
<td>2500</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>LW066A</td>
<td></td>
</tr>
<tr>
<td>SN74LV4066ARGYR</td>
<td>ACTIVE</td>
<td>VQFN</td>
<td>RGY</td>
<td>14</td>
<td>3000</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>LW066A</td>
<td></td>
</tr>
<tr>
<td>SN74LV4066ARGYRG4</td>
<td>ACTIVE</td>
<td>VQFN</td>
<td>RGY</td>
<td>14</td>
<td>3000</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>LW066A</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:  
ACTIVE: Product device recommended for new designs.  
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.  
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.  
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.  
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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# TAPE AND REEL INFORMATION

## REEL DIMENSIONS
![Reel Dimensions Diagram]

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

## TAPE DIMENSIONS
![Tape Dimensions Diagram]

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

- **Sprocket Holes**
- **Pocket Quadrants**
- **User Direction of Feed**

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN74LV4066ADB</td>
<td>SSOP</td>
<td>DB</td>
<td>14</td>
<td>2000</td>
<td>330.0</td>
<td>16.4</td>
<td>8.35</td>
<td>6.6</td>
<td>2.4</td>
<td>12.0</td>
<td>16.0</td>
<td>Q1</td>
</tr>
<tr>
<td>SN74LV4066ADG</td>
<td>TVSOP</td>
<td>DGV</td>
<td>14</td>
<td>2000</td>
<td>330.0</td>
<td>12.4</td>
<td>6.8</td>
<td>4.0</td>
<td>1.6</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
<tr>
<td>SN74LV4066ADR</td>
<td>SOIC</td>
<td>D</td>
<td>14</td>
<td>2500</td>
<td>330.0</td>
<td>16.4</td>
<td>6.5</td>
<td>9.0</td>
<td>2.1</td>
<td>8.0</td>
<td>16.0</td>
<td>Q1</td>
</tr>
<tr>
<td>SN74LV4066ANSR</td>
<td>SO</td>
<td>NS</td>
<td>14</td>
<td>2000</td>
<td>330.0</td>
<td>16.4</td>
<td>8.2</td>
<td>10.5</td>
<td>2.5</td>
<td>12.0</td>
<td>16.0</td>
<td>Q1</td>
</tr>
<tr>
<td>SN74LV4066APWR</td>
<td>TSSOP</td>
<td>PW</td>
<td>14</td>
<td>2000</td>
<td>330.0</td>
<td>12.4</td>
<td>6.9</td>
<td>5.6</td>
<td>1.6</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
<tr>
<td>SN74LV4066APWT</td>
<td>TSSOP</td>
<td>PW</td>
<td>14</td>
<td>250</td>
<td>330.0</td>
<td>12.4</td>
<td>6.9</td>
<td>5.6</td>
<td>1.6</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
<tr>
<td>SN74LV4066ARGYR</td>
<td>VQFN</td>
<td>RGY</td>
<td>14</td>
<td>3000</td>
<td>330.0</td>
<td>12.4</td>
<td>3.75</td>
<td>3.75</td>
<td>1.15</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>
## TAPE AND REEL BOX DIMENSIONS

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN74LV4066ADBR</td>
<td>SSOP</td>
<td>DB</td>
<td>14</td>
<td>2000</td>
<td>356.0</td>
<td>356.0</td>
<td>35.0</td>
</tr>
<tr>
<td>SN74LV4066ADGVR</td>
<td>TVSOP</td>
<td>DGV</td>
<td>14</td>
<td>2000</td>
<td>356.0</td>
<td>356.0</td>
<td>35.0</td>
</tr>
<tr>
<td>SN74LV4066ADR</td>
<td>SOIC</td>
<td>D</td>
<td>14</td>
<td>2500</td>
<td>356.0</td>
<td>356.0</td>
<td>35.0</td>
</tr>
<tr>
<td>SN74LV4066NSR</td>
<td>SO</td>
<td>NS</td>
<td>14</td>
<td>2000</td>
<td>356.0</td>
<td>356.0</td>
<td>35.0</td>
</tr>
<tr>
<td>SN74LV4066APWR</td>
<td>TSSOP</td>
<td>PW</td>
<td>14</td>
<td>2000</td>
<td>356.0</td>
<td>356.0</td>
<td>35.0</td>
</tr>
<tr>
<td>SN74LV4066APWT</td>
<td>TSSOP</td>
<td>PW</td>
<td>14</td>
<td>250</td>
<td>356.0</td>
<td>356.0</td>
<td>35.0</td>
</tr>
<tr>
<td>SN74LV4066ARGYR</td>
<td>VQFN</td>
<td>RGY</td>
<td>14</td>
<td>3000</td>
<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
TUBE

L - Tube length

T - Tube height

W - Tube width

B - Alignment groove width

*All dimensions are nominal

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Name</th>
<th>Package Type</th>
<th>Pins</th>
<th>SPQ</th>
<th>L (mm)</th>
<th>W (mm)</th>
<th>T (µm)</th>
<th>B (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN74LV4066AD</td>
<td>D</td>
<td>SOIC</td>
<td>14</td>
<td>50</td>
<td>506.6</td>
<td>8</td>
<td>3940</td>
<td>4.32</td>
</tr>
<tr>
<td>SN74LV4066AN</td>
<td>N</td>
<td>PDIP</td>
<td>14</td>
<td>25</td>
<td>506</td>
<td>13.97</td>
<td>11230</td>
<td>4.32</td>
</tr>
<tr>
<td>SN74LV4066AN</td>
<td>N</td>
<td>PDIP</td>
<td>14</td>
<td>25</td>
<td>506</td>
<td>13.97</td>
<td>11230</td>
<td>4.32</td>
</tr>
<tr>
<td>SN74LV4066APW</td>
<td>PW</td>
<td>TSSOP</td>
<td>14</td>
<td>90</td>
<td>530</td>
<td>10.2</td>
<td>3600</td>
<td>3.5</td>
</tr>
</tbody>
</table>
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No-Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

⚠ Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated.

The Pin 1 identifiers are either a molded, marked, or metal feature.

G. Package complies to JEDEC MO-241 variation BA.
THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal was, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

![Exposed Thermal Pad Dimensions](image)

NOTE: All linear dimensions are in millimeters
NOTES:  
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SQFN PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.15.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
   14/16/20/56 Pins – MO-194
MECHANICAL DATA

D (R-PDSO-G14) PLASTIC SMALL OUTLINE

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
   △ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.
   △ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.
E. Reference JEDEC MS-012 variation AB.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
⚠️ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 each side.
⚠️ Body width does not include interlead flash. Interlead flash shall not exceed 0.25 each side.
E. Falls within JEDEC MO-153
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
N (R-PDIP-T**)  
PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

<table>
<thead>
<tr>
<th></th>
<th>14</th>
<th>16</th>
<th>18</th>
<th>20</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dim</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A MAX</td>
<td>0.775 (19.69)</td>
<td>0.775 (19.69)</td>
<td>0.920 (23.37)</td>
<td>1.060 (26.92)</td>
</tr>
<tr>
<td>A MIN</td>
<td>0.745 (18.92)</td>
<td>0.745 (18.92)</td>
<td>0.850 (21.59)</td>
<td>0.940 (23.88)</td>
</tr>
<tr>
<td>MS-001 Variation</td>
<td>AA</td>
<td>BB</td>
<td>AC</td>
<td>AD</td>
</tr>
</tbody>
</table>

**NOTES:**
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.
MECHANICAL DATA

DB (R-PDSO-G**)  PLASTIC SMALL-OUTLINE

28 PINS SHOWN

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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