

SN74LVC1G132 Single 2-Input NAND Gate With Schmitt-Trigger Inputs

1 Features

- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- Available in Texas Instruments NanoStar™ and NanoFree™ Packages
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 5.3 ns at 3.3 V
- Low Power Consumption, 10- μ A Maximum I_{CC}
- ± 24 -mA Output Drive at 3.3 V
- I_{off} Supports Partial-Power-Down Mode Operation

2 Applications

- AV Receiver
- Audio Dock: Portable
- Blu-Ray Player and Home Theater
- Embedded PC
- MP3 Player/Recorder (Portable Audio)
- Personal Digital Assistant (PDA)
- Power: Telecom/Server AC/DC Supply: Single Controller: Analog and Digital
- Solid State Drive (SSD): Client and Enterprise
- TV: LCD/Digital and High-Definition (HDTV)
- Tablet: Enterprise
- Video Analytics: Server
- Wireless Headset, Keyboard, and Mouse

3 Description

The SN74LVC1G132 device contains one 2-input NAND gate with Schmitt-trigger inputs designed for 1.65-V to 5.5-V V_{CC} operation and performs the Boolean function $Y = A \times B$ or $Y = \overline{A + B}$ in positive logic.

Because of Schmitt action, this device has different input threshold levels for positive-going (V_{T+}) and negative-going (V_{T-}) signals.

This device can be triggered from the slowest of input ramps and still give clean jitter-free output signals.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

Device Information(1)

| ORDER NUMBER | PACKAGE | BODY SIZE |
|-----------------|------------|-------------------|
| SN74LVC1G132DBV | SOT-23 (5) | 2.90 mm x 1.60 mm |
| SN74LVC1G132DCK | SC70 (5) | 2.00 mm x 1.25 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)

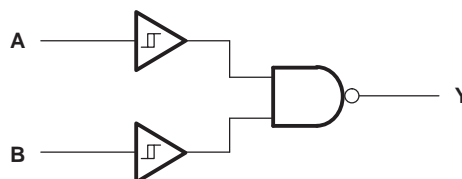


Table of Contents

| | | | |
|--|----------|--|-----------|
| 1 Features | 1 | 6.9 Operating Characteristics..... | 6 |
| 2 Applications | 1 | 7 Parameter Measurement Information | 7 |
| 3 Description | 1 | 8 Detailed Description | 9 |
| 4 Revision History | 2 | 8.1 Functional Block Diagram | 9 |
| 5 Pin Configuration and Functions | 3 | 8.2 Device Functional Modes..... | 9 |
| 6 Specifications | 3 | 9 Device and Documentation Support | 10 |
| 6.1 Absolute Maximum Ratings | 3 | 9.1 Documentation Support | 10 |
| 6.2 ESD Ratings..... | 4 | 9.2 Receiving Notification of Documentation Updates.. | 10 |
| 6.3 Recommended Operating Conditions..... | 4 | 9.3 Community Resources..... | 10 |
| 6.4 Thermal Information | 4 | 9.4 Trademarks | 10 |
| 6.5 Electrical Characteristics..... | 5 | 9.5 Electrostatic Discharge Caution..... | 10 |
| 6.6 Switching Characteristics: –40°C to +85°C, C _L = 15 pF..... | 5 | 9.6 Glossary | 10 |
| 6.7 Switching Characteristics: –40°C to +85°C..... | 6 | 10 Mechanical, Packaging, and Orderable Information | 11 |
| 6.8 Switching Characteristics: –40°C to +125°C..... | 6 | | |

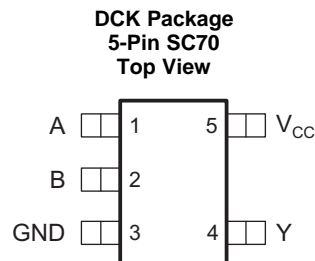
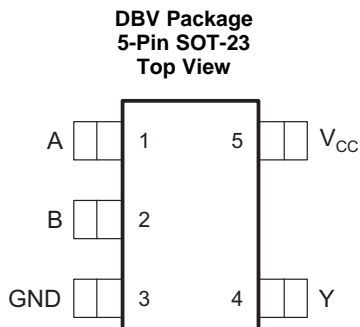
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision C (December 2013) to Revision D | Page |
|---|-------------|
| • Added <i>Applications</i> , <i>Device Information</i> table, <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section..... | 1 |
| • Deleted YEP, YZP packages throughout data sheet | 1 |

| Changes from Revision B (September 2006) to Revision C | Page |
|---|-------------|
| • Updated document to new TI data sheet format | 1 |
| • Removed <i>Ordering Information</i> table | 1 |
| • Updated operating temperature range. | 4 |
| • Added ESD warning. | 10 |

5 Pin Configuration and Functions



See mechanical drawings for dimensions.

Pin Functions

| PIN | | I/O | DESCRIPTION |
|-----------------|----------|-----|---------------------|
| NAME | DBV, DCK | | |
| A | 1 | I | A logic input |
| B | 2 | I | B logic input |
| GND | 3 | — | Ground |
| V _{CC} | 5 | — | Positive supply |
| Y | 4 | O | Y NAND logic output |

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT | |
|------------------|---|--------------------|-----------------------|------|----|
| V _{CC} | Supply voltage | -0.5 | 6.5 | V | |
| V _I | Input voltage ⁽²⁾ | -0.5 | 6.5 | V | |
| V _O | Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾ | -0.5 | 6.5 | V | |
| V _O | Voltage range applied to any output in the high or low state ⁽²⁾⁽³⁾ | -0.5 | V _{CC} + 0.5 | V | |
| I _{IK} | Input clamp current | V _I < 0 | | -50 | mA |
| I _{OK} | Output clamp current | V _O < 0 | | -50 | mA |
| I _O | Continuous output current | | | ±50 | mA |
| | Continuous current through V _{CC} or GND | | | ±100 | mA |
| T _{stg} | Storage temperature | -65 | 150 | °C | |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

6.2 ESD Ratings

| | | VALUE | UNIT |
|-------------|-------------------------|--|------|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | 2000 |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | 1000 |
| | | Machine Model (A115-A) | 200 |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

| | | MIN | MAX | UNIT | |
|----------|--------------------------------|--------------------------|----------|------|----|
| V_{CC} | Supply voltage | Operating | 1.65 | 5.5 | V |
| | | Data retention only | 1.5 | | |
| V_I | Input voltage | 0 | 5.5 | V | |
| V_O | Output voltage | 0 | V_{CC} | V | |
| I_{OH} | High-level output current | $V_{CC} = 1.65\text{ V}$ | | –4 | mA |
| | | $V_{CC} = 2.3\text{ V}$ | | –8 | |
| | | $V_{CC} = 3\text{ V}$ | | –16 | |
| | | | | –24 | |
| | | $V_{CC} = 4.5\text{ V}$ | | –32 | |
| I_{OL} | Low-level output current | $V_{CC} = 1.65\text{ V}$ | | 4 | mA |
| | | $V_{CC} = 2.3\text{ V}$ | | 8 | |
| | | $V_{CC} = 3\text{ V}$ | | 16 | |
| | | | | 24 | |
| | | $V_{CC} = 4.5\text{ V}$ | | 32 | |
| T_A | Operating free-air temperature | –40 | 125 | °C | |

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See [Implications of Slow or Floating CMOS Inputs](#), SCBA004.

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | SN74LVC1G132 | | UNIT | |
|-------------------------------|--|------------|------|------|
| | DBV (SOT-23) | DCK (SC70) | | |
| | 5 PINS | 5 PINS | | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 206 | 252 | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | –40°C to +85°C | | | –40°C to +125°C | | | UNIT |
|---|---------------------------|---|-----------------------|--------------------|-----------------------|-----------------|--------------------|------|------|
| | | | MIN | TYP ⁽¹⁾ | MAX | MIN | TYP ⁽¹⁾ | MAX | |
| V _{T+} Positive-going input threshold voltage | | 1.65 V | 0.79 | | 1.16 | 0.79 | | 1.16 | V |
| | | 2.3 V | 1.11 | | 1.56 | 1.11 | | 1.56 | |
| | | 3 V | 1.5 | | 1.87 | 1.5 | | 1.87 | |
| | | 4.5 V | 2.16 | | 2.74 | 2.16 | | 2.74 | |
| | | 5.5 V | 2.61 | | 3.33 | 2.61 | | 3.33 | |
| V _{T–} Negative-going input threshold voltage | | 1.65 V | 0.39 | | 0.62 | 0.39 | | 0.62 | V |
| | | 2.3 V | 0.58 | | 0.87 | 0.58 | | 0.87 | |
| | | 3 V | 0.84 | | 1.14 | 0.84 | | 1.16 | |
| | | 4.5 V | 1.41 | | 1.79 | 1.41 | | 1.84 | |
| | | 5.5 V | 1.87 | | 2.29 | 1.87 | | 2.33 | |
| ΔV _T Hysteresis (V _{T+} – V _{T–}) | | 1.65 V | 0.37 | | 0.62 | 0.37 | | 0.62 | V |
| | | 2.3 V | 0.48 | | 0.77 | 0.48 | | 0.77 | |
| | | 3 V | 0.56 | | 0.87 | 0.54 | | 0.87 | |
| | | 4.5 V | 0.71 | | 1.04 | 0.66 | | 1.04 | |
| | | 5.5 V | 0.71 | | 1.11 | 0.67 | | 1.11 | |
| V _{OH} | I _{OH} = –100 μA | 1.65 V to 5.5 V | V _{CC} – 0.1 | | V _{CC} – 0.1 | | | | V |
| | I _{OH} = –4 mA | 1.65 V | 1.2 | | 1.2 | | | | |
| | I _{OH} = –8 mA | 2.3 V | 1.9 | | 1.9 | | | | |
| | I _{OH} = –16 mA | 3 V | 2.4 | | 2.4 | | | | |
| | I _{OH} = –24 mA | | 2.3 | | 2.3 | | | | |
| | I _{OH} = –32 mA | 4.5 V | 3.8 | | 3.8 | | | | |
| V _{OL} | I _{OL} = 100 μA | 1.65 V to 5.5 V | | | 0.1 | | 0.1 | | V |
| | I _{OL} = 4 mA | 1.65 V | | | 0.45 | | 0.45 | | |
| | I _{OL} = 8 mA | 2.3 V | | | 0.3 | | 0.3 | | |
| | I _{OL} = 16 mA | 3 V | | | 0.4 | | 0.4 | | |
| | I _{OL} = 24 mA | | | | 0.55 | | 0.55 | | |
| | I _{OL} = 32 mA | 4.5 V | | | 0.55 | | 0.55 | | |
| I _i | A or B inputs | V _I = 5.5 V or GND | 1.65 V to 5.5 V | | ±1 | | ±1 | | μA |
| I _{off} | | V _I or V _O = 5.5 V | 0 | | ±10 | | ±10 | | μA |
| I _{CC} | | V _I = V _{CC} or GND, I _O = 0 | 1.65 V to 5.5 V | | 10 | | 10 | | μA |
| ΔI _{CC} | | One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND | 3 V to 5.5 V | | 500 | | 500 | | μA |
| C _i | | V _I = V _{CC} or GND | 3.3 V | | 3.5 | | | | pF |

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

6.6 Switching Characteristics: –40°C to +85°C, C_L = 15 pF

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | –40°C to +85°C | | | | | | | | UNIT |
|-----------------|-----------------|----------------|------------------------------------|-----|-----------------------------------|-----|-----------------------------------|-----|---------------------------------|-----|------|
| | | | V _{CC} = 1.8 V ±0.15 V | | V _{CC} = 2.5 V ±0.2 V | | V _{CC} = 3.3 V ±0.3 V | | V _{CC} = 5 V ±0.5 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _{pd} | A or B | Y | 4 | 16 | 2.5 | 7 | 2 | 5.3 | 1.5 | 4.4 | ns |

6.7 Switching Characteristics: –40°C to +85°C

 over recommended operating free-air temperature range, $C_L = 30$ pF or 50 pF (unless otherwise noted) (see [Figure 2](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | –40°C to +85°C | | | | | | | | UNIT |
|-----------|-----------------|----------------|--|-----|---|-----|---|-----|---|-----|------|
| | | | $V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$ | | $V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$ | | $V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$ | | $V_{CC} = 5\text{ V}$ $\pm 0.5\text{ V}$ | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_{pd} | A or B | Y | 4 | 16 | 3 | 7.5 | 2 | 6 | 2 | 5 | ns |

6.8 Switching Characteristics: –40°C to +125°C

 over recommended operating free-air temperature range, $C_L = 30$ pF or 50 pF (unless otherwise noted) (see [Figure 2](#))

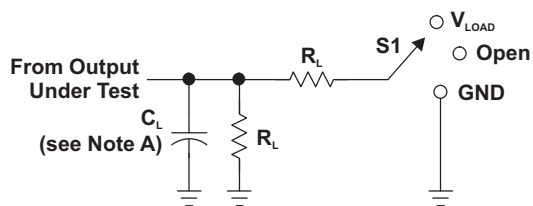
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | –40°C to +125°C | | | | | | | | UNIT |
|-----------|-----------------|----------------|--|------|---|-----|---|-----|---|-----|------|
| | | | $V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$ | | $V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$ | | $V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$ | | $V_{CC} = 5\text{ V}$ $\pm 0.5\text{ V}$ | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_{pd} | A or B | Y | 4 | 16.5 | 3 | 8 | 2 | 6.5 | 2 | 5.5 | ns |

6.9 Operating Characteristics

 $T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | $V_{CC} = 1.8\text{ V}$ | $V_{CC} = 2.5\text{ V}$ | $V_{CC} = 3.3\text{ V}$ | $V_{CC} = 5\text{ V}$ | UNIT |
|--|---------------------|-------------------------|-------------------------|-------------------------|-----------------------|------|
| | | TYP | TYP | TYP | TYP | |
| C_{pd} Power dissipation capacitance | $f = 10\text{ MHz}$ | 17 | 18 | 18 | 20 | pF |

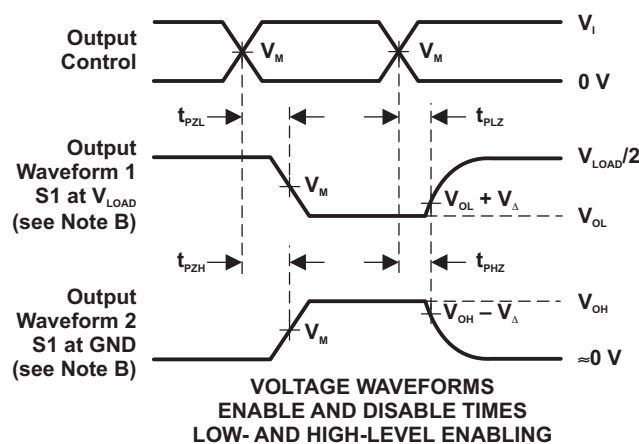
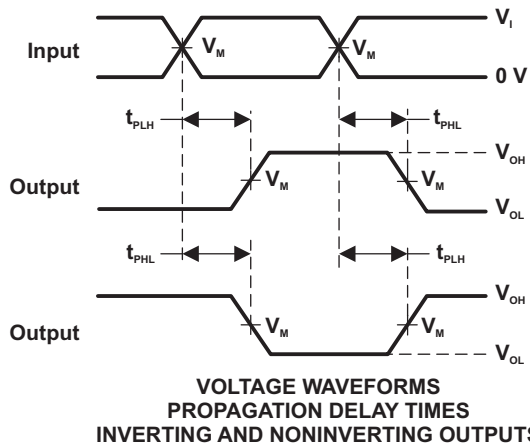
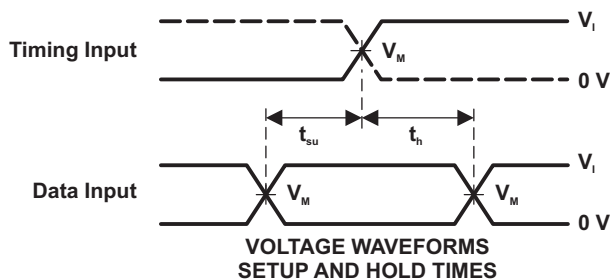
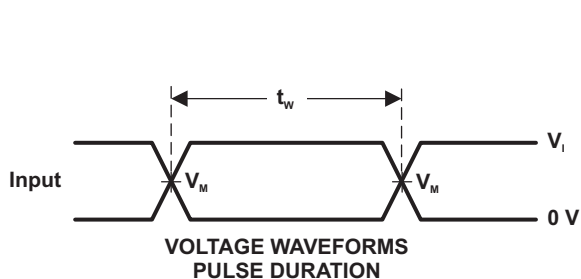
7 Parameter Measurement Information



LOAD CIRCUIT

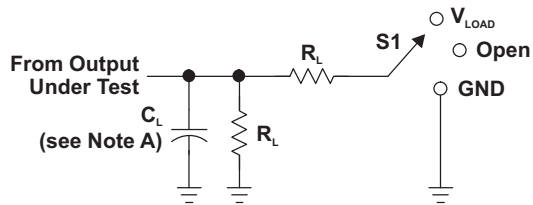
| TEST | S1 |
|-------------------|------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | V_{LOAD} |
| t_{PHZ}/t_{PZH} | GND |

| V_{CC} | INPUTS | | V_M | V_{LOAD} | C_L | R_L | V_{Δ} |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
| | V_i | t_i/t_r | | | | | |
| $1.8\text{ V} \pm 0.15\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 1 M Ω | 0.15 V |
| $2.5\text{ V} \pm 0.2\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 1 M Ω | 0.15 V |
| $3.3\text{ V} \pm 0.3\text{ V}$ | 3 V | $\leq 2.5\text{ ns}$ | 1.5 V | 6 V | 15 pF | 1 M Ω | 0.3 V |
| $5\text{ V} \pm 0.5\text{ V}$ | V_{CC} | $\leq 2.5\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 1 M Ω | 0.3 V |



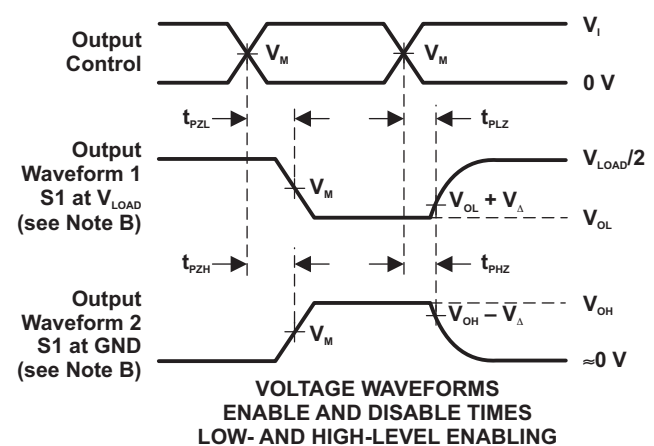
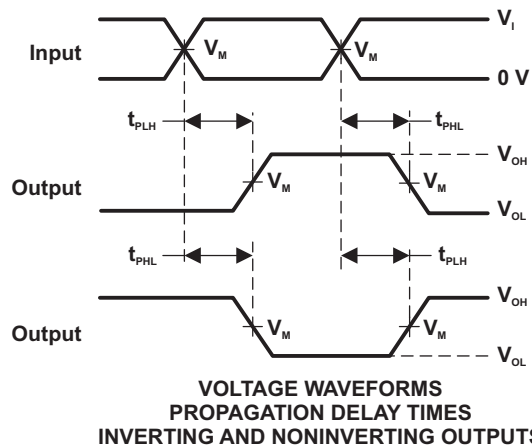
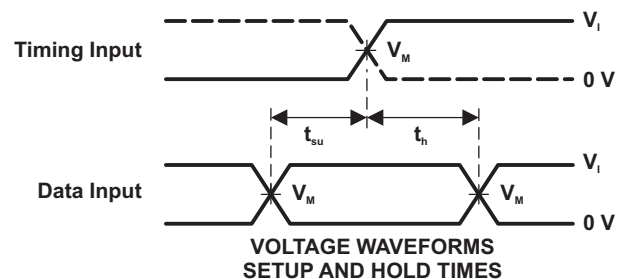
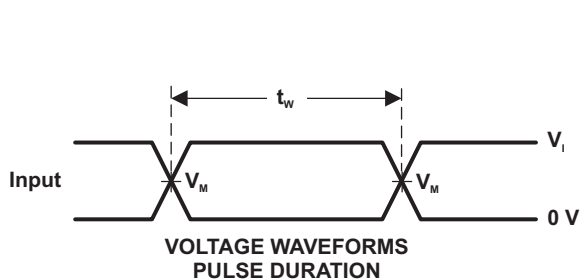
- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_o = 50\ \Omega$.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

Parameter Measurement Information (continued)

LOAD CIRCUIT

| TEST | S1 |
|-------------------|------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | V_{LOAD} |
| t_{PHZ}/t_{PZH} | GND |

| V_{CC} | INPUTS | | V_M | V_{LOAD} | C_L | R_L | V_{Δ} |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
| | V_I | t_r/t_f | | | | | |
| $1.8\text{ V} \pm 0.15\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k Ω | 0.15 V |
| $2.5\text{ V} \pm 0.2\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| $3.3\text{ V} \pm 0.3\text{ V}$ | 3 V | $\leq 2.5\text{ ns}$ | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| $5\text{ V} \pm 0.5\text{ V}$ | V_{CC} | $\leq 2.5\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 50 pF | 500 Ω | 0.3 V |



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_o = 50\ \Omega$.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{on} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Functional Block Diagram

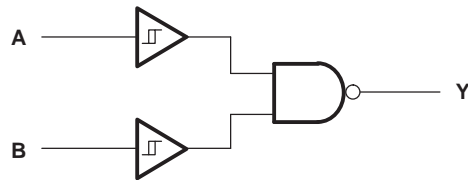


Figure 3. Logic Diagram (Positive Logic)

8.2 Device Functional Modes

Table 1 lists the functional modes of the SN74LVC1G132.

Table 1. Function Table

| INPUTS | | OUTPUT Y |
|--------|---|-------------|
| A | B | |
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

[Implications of Slow or Floating CMOS Inputs](#), SCBA004

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

9.4 Trademarks

NanoStar, NanoFree, E2E are trademarks of Texas Instruments. All other trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

9.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|----------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| 74LVC1G132DBVRG4.Z | Active | Production | SOT-23 (DBV) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C3BR |
| 74LVC1G132DCKRG4 | Active | Production | SC70 (DCK) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | D5R |
| 74LVC1G132DCKRG4.Z | Active | Production | SC70 (DCK) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | D5R |
| 74LVC1G132DCKTG4 | Active | Production | SC70 (DCK) 5 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | D5R |
| 74LVC1G132DCKTG4.Z | Active | Production | SC70 (DCK) 5 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | D5R |
| SN74LVC1G132DBVR | Active | Production | SOT-23 (DBV) 5 | 3000 LARGE T&R | Yes | NIPDAU SN NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (C3BJ, C3BR) |
| SN74LVC1G132DBVR.Z | Active | Production | SOT-23 (DBV) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (C3BJ, C3BR) |
| SN74LVC1G132DBVT | Active | Production | SOT-23 (DBV) 5 | 250 SMALL T&R | Yes | NIPDAU SN NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (C3BJ, C3BR) |
| SN74LVC1G132DBVT.Z | Active | Production | SOT-23 (DBV) 5 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (C3BJ, C3BR) |
| SN74LVC1G132DBVTG4.Z | Active | Production | SOT-23 (DBV) 5 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C3BR |
| SN74LVC1G132DCKR | Active | Production | SC70 (DCK) 5 | 3000 LARGE T&R | Yes | NIPDAU SN NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (D55, D5J, D5R) |
| SN74LVC1G132DCKR.Z | Active | Production | SC70 (DCK) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (D55, D5J, D5R) |
| SN74LVC1G132DCKRG4.Z | Active | Production | SC70 (DCK) 5 | 3000 LARGE T&R | - | Call TI | Call TI | -40 to 125 | |
| SN74LVC1G132DCKT | Active | Production | SC70 (DCK) 5 | 250 SMALL T&R | Yes | NIPDAU SN | Level-1-260C-UNLIM | -40 to 125 | (D55, D5J, D5R) |
| SN74LVC1G132DCKT.Z | Active | Production | SC70 (DCK) 5 | 250 SMALL T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | (D55, D5J, D5R) |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| 74LVC1G132DCKRG4 | SC70 | DCK | 5 | 3000 | 180.0 | 8.4 | 2.47 | 2.3 | 1.25 | 4.0 | 8.0 | Q3 |
| 74LVC1G132DCKTG4 | SC70 | DCK | 5 | 250 | 180.0 | 8.4 | 2.47 | 2.3 | 1.25 | 4.0 | 8.0 | Q3 |
| SN74LVC1G132DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| SN74LVC1G132DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| SN74LVC1G132DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| SN74LVC1G132DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| SN74LVC1G132DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74LVC1G132DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 8.4 | 2.47 | 2.3 | 1.25 | 4.0 | 8.0 | Q3 |
| SN74LVC1G132DCKT | SC70 | DCK | 5 | 250 | 180.0 | 8.4 | 2.47 | 2.3 | 1.25 | 4.0 | 8.0 | Q3 |
| SN74LVC1G132DCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| 74LVC1G132DCKRG4 | SC70 | DCK | 5 | 3000 | 183.0 | 183.0 | 20.0 |
| 74LVC1G132DCKTG4 | SC70 | DCK | 5 | 250 | 183.0 | 183.0 | 20.0 |
| SN74LVC1G132DBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| SN74LVC1G132DBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| SN74LVC1G132DBVT | SOT-23 | DBV | 5 | 250 | 210.0 | 185.0 | 35.0 |
| SN74LVC1G132DBVT | SOT-23 | DBV | 5 | 250 | 210.0 | 185.0 | 35.0 |
| SN74LVC1G132DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G132DCKR | SC70 | DCK | 5 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74LVC1G132DCKT | SC70 | DCK | 5 | 250 | 202.0 | 201.0 | 28.0 |
| SN74LVC1G132DCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |

EXAMPLE BOARD LAYOUT

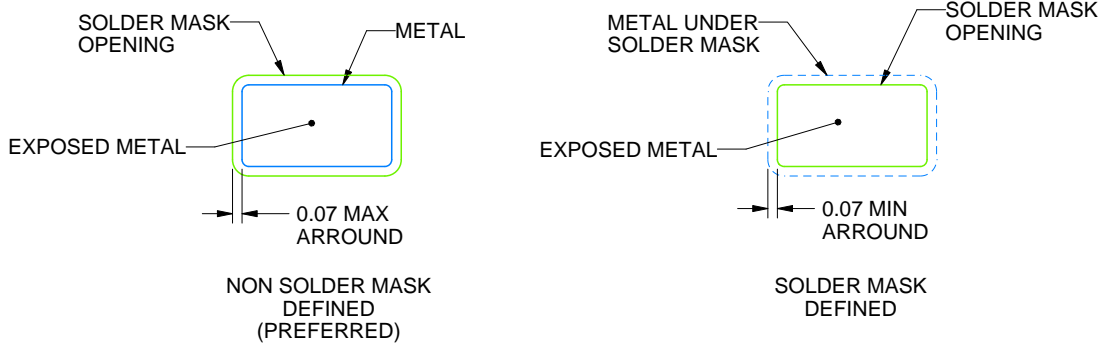
DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

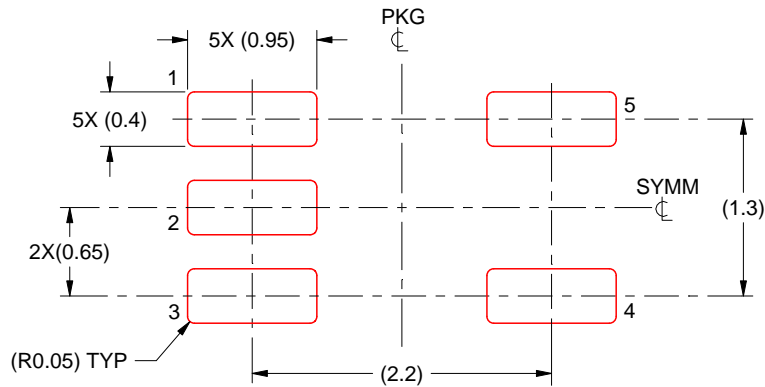
- 7. Publication IPC-7351 may have alternate designs.
- 8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2025, Texas Instruments Incorporated