SN74LVC1G14 Single Schmitt-Trigger Inverter

1 Features

• Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
• ESD Protection Exceeds JESD 22
  – 2000-V Human-Body Model (A114-A)
  – 200-V Machine Model (A115-A)
  – 1000-V Charged-Device Model (C101)
• Available in the Texas Instruments NanoFree™ Package
• Supports 5-V V<sub>CC</sub> Operation
• Inputs Accept Voltages to 5.5 V
• Max t<sub>pd</sub> of 4.6 ns at 3.3 V
• Low Power Consumption, 10-µA Max I<sub>CC</sub>
• ±24-mA Output Drive at 3.3 V
• I<sub>off</sub> Supports Partial-Power-Down Mode Operation

2 Applications

• AV Receiver
• Audio Dock: Portable
• Blu-ray Player and Home Theater
• Embedded PC
• MP3 Player/Recorder (Portable Audio)
• Personal Digital Assistant (PDA)
• Power: Telecom/Server AC/DC Supply: Single Controller: Analog and Digital
• Solid State Drive (SSD): Client and Enterprise
• TV: LCD/Digital and High-Definition (HDTV)
• Tablet: Enterprise
• Video Analytics: Server
• Wireless Headset, Keyboard, and Mouse

3 Description

This single Schmitt-trigger inverter is designed for 1.65-V to 5.5-V V<sub>CC</sub> operation.

The SN74LVC1G14 device contains one inverter and performs the Boolean function Y = \bar{A}. The device functions as an independent inverter with Schmitt-trigger inputs, so the device has different input threshold levels for positive-going (V<sub>T+</sub>) and negative-going (V<sub>T–</sub>) signals to provide hysteresis (ΔV<sub>T</sub>) which makes the device tolerant to slow or noisy input signals.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs when the device is powered down. This inhibits current backflow into the device which prevents damage to the device.

<table>
<thead>
<tr>
<th>ORDER NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN74LVC1G14DBV</td>
<td>SOT-23 (5)</td>
<td>2.90 mm x 1.60 mm</td>
</tr>
<tr>
<td>SN74LVC1G14DCK</td>
<td>SC70 (5)</td>
<td>2.00 mm x 1.25 mm</td>
</tr>
<tr>
<td>SN74LVC1G14DRL</td>
<td>SOT-5X3 (5)</td>
<td>1.60 mm x 1.20 mm</td>
</tr>
<tr>
<td>SN74LVC1G14DRY</td>
<td>SON (6)</td>
<td>1.45 mm x 1.00 mm</td>
</tr>
<tr>
<td>SN74LVC1G14DSF</td>
<td>SON (6)</td>
<td>1.00 mm x 1.00 mm</td>
</tr>
<tr>
<td>SN74LVC1G14YZP</td>
<td>DSBGA (5)</td>
<td>1.39 mm x 0.89 mm</td>
</tr>
<tr>
<td>SN74LVC1G14YZV</td>
<td>DSBGA (4)</td>
<td>0.89 mm x 0.89 mm</td>
</tr>
<tr>
<td>SN74LVC1G14DPW</td>
<td>X2SON (5)</td>
<td>0.80 mm x 0.80 mm</td>
</tr>
</tbody>
</table>

Logic Diagram (Positive Logic)

(DBV, DCK, DRL, DRY, DPW, and YZP Package)

Logic Diagram (Positive Logic)

(YZV Package)
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   9.1 Application Information ...................................... 11
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision X (August 2017) to Revision Y Page

- Changed New package pinout added to Pin Functions table. Multiple Pin Functions tables condensed to one. ................. 4
- Changed Tj and Tsstg lines switched for consistency with other devices. ................................................................. 4
- Added differentiated ROC temperatures for DPW, YZP and YZV packages .......................................................... 5
- Changed format of Switching Characteristics tables to include columns for different Cl conditions .......................... 7
- Added temperature range to Conditions statement for Switching Characteristics tables ................................. 7
- Replaced PMI section with updated load circuit and relevant waveform figures. Collapsed parameter measurement values into one table. ......................................................... 8

Changes from Revision W (March 2014) to Revision X Page

- Added Thermal Information table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, and Layout section .......................................................... 1
- Added DSF, YZP, YZV, and DPW packages to Device Information table ................................................................. 1
- Changed Terminal Configuration and Functions to Pin Configuration and Functions ............................................. 3
- Moved Storage temperature, Tsstg to Absolute Maximum Ratings table ................................................................. 4
- Changed Handling Ratings table to ESD Ratings ................................. 4
- Changed values in the Thermal Information table to align with JEDEC standards ................................................. 5
- Added typical application .................................................. 11
- Added Documentation Support, Receiving Notification of Documentation Updates, and Community Resources .... 14

Changes from Revision V (Novmber 2012) to Revision W Page

- Added DPW Package .................................................. 1
- Added Applications ................................................... 1
- Moved Tsstg to Handling Ratings table ................................. 4
5 Pin Configuration and Functions

See mechanical drawings for dimensions.

N.C. – No internal connection

DNU – Do not use
### Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>2</td>
<td>Signal Input</td>
</tr>
<tr>
<td>GND</td>
<td>3</td>
<td>Ground</td>
</tr>
<tr>
<td>N.C.</td>
<td>1, 5</td>
<td>No internal connection (1)</td>
</tr>
<tr>
<td>DNU</td>
<td>—</td>
<td>Do not use (2)</td>
</tr>
<tr>
<td>VCC</td>
<td>5</td>
<td>Positive Supply</td>
</tr>
<tr>
<td>Y</td>
<td>4</td>
<td>Signal Output</td>
</tr>
</tbody>
</table>

(1) Pins labeled N.C. can be connected to any signal or voltage source, including ground. They should always be soldered to the board.

(2) Pins labeled DNU should not be connected to any signal or voltage source, including ground. They should always be soldered to the board.

### 6 Specifications

#### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td>–0.5</td>
<td>6.5</td>
<td>V</td>
</tr>
<tr>
<td>$V_I$</td>
<td>–0.5</td>
<td>6.5</td>
<td>V</td>
</tr>
<tr>
<td>$V_O$</td>
<td>–0.5</td>
<td>$V_{CC} + 0.5$</td>
<td>V</td>
</tr>
<tr>
<td>$I_{IK}$</td>
<td>–50</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$I_{OK}$</td>
<td>–50</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$I_O$</td>
<td>±50</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$T_J$</td>
<td>–65</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>$T_{STG}$</td>
<td>150</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The value of $V_{CC}$ is provided in the recommended operating conditions table.

#### 6.2 ESD Ratings

<table>
<thead>
<tr>
<th>ESD Type</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{ESD}$</td>
<td>Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)</td>
<td>2000</td>
</tr>
<tr>
<td></td>
<td>Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)</td>
<td>1000</td>
</tr>
<tr>
<td></td>
<td>Machine Model (A115-A)</td>
<td>200</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Unit</th>
<th>MIN</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>(V_{CC})</td>
<td>V</td>
<td>1.65</td>
<td>5.5</td>
</tr>
<tr>
<td>Operating</td>
<td>Data retention only</td>
<td></td>
<td></td>
<td>1.5</td>
</tr>
<tr>
<td>Input voltage</td>
<td>(V_I)</td>
<td>V</td>
<td>0</td>
<td>5.5</td>
</tr>
<tr>
<td>Output voltage</td>
<td>(V_O)</td>
<td>V</td>
<td>0</td>
<td>(V_{CC})</td>
</tr>
</tbody>
</table>

\(I_{OH}\) High-level output current

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Unit</th>
<th>(V_{CC})</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>(I_{OH})</td>
<td>High-level output current</td>
<td>mA</td>
<td>1.65 V</td>
<td>–4</td>
</tr>
<tr>
<td>(I_{OH})</td>
<td></td>
<td></td>
<td>2.3 V</td>
<td>–8</td>
</tr>
<tr>
<td>(I_{OH})</td>
<td></td>
<td></td>
<td>3 V</td>
<td>–16</td>
</tr>
<tr>
<td>(I_{OH})</td>
<td></td>
<td></td>
<td>3.3 V</td>
<td>–24</td>
</tr>
<tr>
<td>(I_{OH})</td>
<td></td>
<td></td>
<td>4.5 V</td>
<td>–32</td>
</tr>
</tbody>
</table>

\(I_{OL}\) Low-level output current

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Unit</th>
<th>(V_{CC})</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>(I_{OL})</td>
<td>Low-level output current</td>
<td>mA</td>
<td>1.65 V</td>
<td>4</td>
</tr>
<tr>
<td>(I_{OL})</td>
<td></td>
<td></td>
<td>2.3 V</td>
<td>8</td>
</tr>
<tr>
<td>(I_{OL})</td>
<td></td>
<td></td>
<td>3 V</td>
<td>16</td>
</tr>
<tr>
<td>(I_{OL})</td>
<td></td>
<td></td>
<td>3.3 V</td>
<td>24</td>
</tr>
<tr>
<td>(I_{OL})</td>
<td></td>
<td></td>
<td>4.5 V</td>
<td>32</td>
</tr>
</tbody>
</table>

\(T_A\) Operating free-air temperature

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Unit</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>(T_A)</td>
<td>Operating free-air temperature</td>
<td>°C</td>
<td>–40</td>
</tr>
<tr>
<td>YZP, YZV, and DPW packages</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>All other packages</td>
<td></td>
<td></td>
<td>–40</td>
</tr>
</tbody>
</table>

(1) All unused inputs of the device must be held at \(V_{CC}\) or GND to assure proper device operation. See Implications of Slow or Floating CMOS Inputs.

6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1)})</th>
<th>Unit</th>
<th>DBV (SOT-23)</th>
<th>DCK (SC70)</th>
<th>DRL (SOT-5X3)</th>
<th>DRY (SON)</th>
<th>DPW (X2SON)</th>
<th>YZV (DSBGA)</th>
<th>YZP (DSBGA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(R_{JUA}) Junction-to-ambient thermal resistance</td>
<td>°C/W</td>
<td>247.2</td>
<td>276.1</td>
<td>296.2</td>
<td>369.6</td>
<td>522.9</td>
<td>168.2</td>
<td>146.2</td>
</tr>
<tr>
<td>(R_{JUC(top)}) Junction-to-case (top) thermal resistance</td>
<td>°C/W</td>
<td>154.5</td>
<td>178.9</td>
<td>137.3</td>
<td>257.6</td>
<td>250.5</td>
<td>2.1</td>
<td>1.4</td>
</tr>
<tr>
<td>(R_{JUB}) Junction-to-board thermal resistance</td>
<td>°C/W</td>
<td>86.8</td>
<td>70.9</td>
<td>145.3</td>
<td>230.8</td>
<td>384.0</td>
<td>55.9</td>
<td>39.8</td>
</tr>
<tr>
<td>(\psi_{JT}) Junction-to-top characterization parameter</td>
<td>°C/W</td>
<td>58.0</td>
<td>47.0</td>
<td>14.7</td>
<td>77.2</td>
<td>46.5</td>
<td>1.1</td>
<td>0.7</td>
</tr>
<tr>
<td>(\psi_{JB}) Junction-to-board characterization parameter</td>
<td>°C/W</td>
<td>86.4</td>
<td>69.3</td>
<td>145.9</td>
<td>231.0</td>
<td>382.8</td>
<td>56.3</td>
<td>39.3</td>
</tr>
<tr>
<td>(R_{JUC(bot)}) Junction-to-case (bottom) thermal resistance</td>
<td>°C/W</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>174.1</td>
<td>N/A</td>
<td>N/A</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>( V_{CC} )</th>
<th>(-40^\circ C ) to ( 85^\circ C )</th>
<th>(-40^\circ C ) to ( 125^\circ C )</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{T+} )</td>
<td>Positive-going input threshold voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>DBV, DCK, DRL, DRY, DSF, YZV and YZP packages</td>
<td>1.65 V</td>
<td>0.79</td>
<td>1.16</td>
<td>.79</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.3 V</td>
<td>1.11</td>
<td>1.56</td>
<td>1.11</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3 V</td>
<td>1.5</td>
<td>1.87</td>
<td>1.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4.5 V</td>
<td>2.16</td>
<td>2.74</td>
<td>2.16</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5.5 V</td>
<td>2.61</td>
<td>3.33</td>
<td>2.61</td>
</tr>
<tr>
<td>( V_{T-} )</td>
<td>Negative-going input threshold voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>DPW package</td>
<td>1.65 V</td>
<td>0.39</td>
<td>0.62</td>
<td>.39</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.3 V</td>
<td>0.58</td>
<td>0.87</td>
<td>.58</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3 V</td>
<td>0.84</td>
<td>1.14</td>
<td>.84</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4.5 V</td>
<td>1.41</td>
<td>1.79</td>
<td>1.41</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5.5 V</td>
<td>1.87</td>
<td>2.29</td>
<td>1.87</td>
</tr>
<tr>
<td>( \Delta V_T )</td>
<td>Hysteresis ( (V_{T+} - V_{T-}) )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.65 V</td>
<td>0.37</td>
<td>0.62</td>
<td>0.37</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.3 V</td>
<td>0.48</td>
<td>0.77</td>
<td>0.48</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3 V</td>
<td>0.56</td>
<td>0.87</td>
<td>0.56</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4.5 V</td>
<td>0.71</td>
<td>1.04</td>
<td>0.71</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5.5 V</td>
<td>0.71</td>
<td>1.11</td>
<td>0.71</td>
</tr>
<tr>
<td>( V_{OH} )</td>
<td>( I_{OL} = -100 \mu A )</td>
<td>( V_{CC} - 0.1 )</td>
<td>1.65 V to 4.5 V</td>
<td>1.2</td>
<td>1.2</td>
</tr>
<tr>
<td></td>
<td>( I_{OL} = -4 \mu A )</td>
<td></td>
<td>1.65 V</td>
<td>1.2</td>
<td>1.2</td>
</tr>
<tr>
<td></td>
<td>( I_{OL} = -8 \mu A )</td>
<td></td>
<td>2.3 V</td>
<td>1.9</td>
<td>1.9</td>
</tr>
<tr>
<td></td>
<td>( I_{OL} = -16 \mu A )</td>
<td></td>
<td>3 V</td>
<td>2.4</td>
<td>2.4</td>
</tr>
<tr>
<td></td>
<td>( I_{OL} = -24 \mu A )</td>
<td></td>
<td>4.5 V</td>
<td>2.3</td>
<td>2.3</td>
</tr>
<tr>
<td></td>
<td>( I_{OL} = -32 \mu A )</td>
<td></td>
<td>4.5 V</td>
<td>3.8</td>
<td>3.8</td>
</tr>
<tr>
<td>( V_{OL} )</td>
<td>( I_{OL} = 100 \mu A )</td>
<td>( V_{CC} - 0.1 )</td>
<td>1.65 V to 4.5 V</td>
<td>0.1</td>
<td>0.1</td>
</tr>
<tr>
<td></td>
<td>( I_{OL} = 4 \mu A )</td>
<td></td>
<td>1.65 V</td>
<td>0.45</td>
<td>0.45</td>
</tr>
<tr>
<td></td>
<td>( I_{OL} = 8 \mu A )</td>
<td></td>
<td>2.3 V</td>
<td>0.3</td>
<td>0.3</td>
</tr>
<tr>
<td></td>
<td>( I_{OL} = 16 \mu A )</td>
<td></td>
<td>3 V</td>
<td>0.4</td>
<td>0.4</td>
</tr>
<tr>
<td></td>
<td>( I_{OL} = 24 \mu A )</td>
<td></td>
<td>4.5 V</td>
<td>0.55</td>
<td>0.55</td>
</tr>
<tr>
<td></td>
<td>( I_{OL} = 32 \mu A )</td>
<td></td>
<td>4.5 V</td>
<td>0.55</td>
<td>0.55</td>
</tr>
<tr>
<td>( I_i )</td>
<td>( I_{i} ) = input ( V_I = 5.5 ) V or GND</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( V_I = 5.5 ) V or GND</td>
<td></td>
<td>0 to 5.5 V</td>
<td>±5</td>
<td>±5</td>
</tr>
<tr>
<td>( I_{off} )</td>
<td>( V_I ) or ( V_O = 5.5 ) V</td>
<td></td>
<td>0</td>
<td>±10</td>
<td>±10</td>
</tr>
<tr>
<td>( I_{CC} )</td>
<td>( V_I = 5.5 ) V or GND, ( I_O = 0 )</td>
<td>( V_{CC} - 0.6 ) V, or GND</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( V_{CC} = 5.5 ) V</td>
<td></td>
<td>1.65 V to 5.5 V</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>( \Delta I_{CC} )</td>
<td>One input at ( V_{CC} = 0.6 ) V, or GND</td>
<td></td>
<td>3 V to 5.5 V</td>
<td>500</td>
<td>500</td>
</tr>
<tr>
<td>( C_i )</td>
<td>( V_I = V_{CC} ) or GND</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( V_I = V_{CC} ) or GND</td>
<td></td>
<td>3.3 V</td>
<td>4.5</td>
<td>4.5</td>
</tr>
</tbody>
</table>

(1) These specifications do not apply to DPW, YZV and YZP packages. DPW, YZV and YZP have a recommended operating free-air temperature range of \(-40^\circ C \) to \( 85^\circ C \).

(2) All typical values are at \( V_{CC} = 3.3 \) V, \( T_A = 25^\circ C \).
6.6 Switching Characteristics: –40°C to 85°C
over recommended operating free-air temperature range, (–40°C to 85°C unless otherwise noted) (see )

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>$V_{CC}$</th>
<th>$C_L = 15$ pF</th>
<th>$C_L = 30$ pF or 50 pF</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{pd}$</td>
<td>A</td>
<td>Y</td>
<td>$1.8 \text{ V} \pm 0.15 \text{ V}$</td>
<td>2.8</td>
<td>3.8</td>
<td>11</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$2.5 \text{ V} \pm 0.2 \text{ V}$</td>
<td>1.6</td>
<td>2</td>
<td>6.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$3.3 \text{ V} \pm 0.3 \text{ V}$</td>
<td>1.5</td>
<td>1.8</td>
<td>5.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$5 \text{ V} \pm 0.5 \text{ V}$</td>
<td>0.9</td>
<td>1.2</td>
<td>5</td>
</tr>
</tbody>
</table>

6.7 Switching Characteristics: –40°C to 125°C
over operating free-air temperature range, (–40°C to 125°C unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>$V_{CC}$</th>
<th>$C_L = 30$ pF or 50 pF</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{pd}$</td>
<td>A</td>
<td>Y</td>
<td>$1.8 \text{ V} \pm 0.15 \text{ V}$</td>
<td>3.8</td>
<td>13</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$2.5 \text{ V} \pm 0.2 \text{ V}$</td>
<td>2</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$3.3 \text{ V} \pm 0.3 \text{ V}$</td>
<td>1.8</td>
<td>6.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$5 \text{ V} \pm 0.5 \text{ V}$</td>
<td>1.2</td>
<td>6</td>
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</table>

6.8 Operating Characteristics
$T_A = 25°C$

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>$V_{CC}$</th>
<th>TYP</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{pd}$</td>
<td>$f = 10 \text{ MHz}$</td>
<td>$1.8 \text{ V}$</td>
<td>20</td>
<td>pF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$2.5 \text{ V}$</td>
<td>21</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$3.3 \text{ V}$</td>
<td>22</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$5 \text{ V}$</td>
<td>25</td>
<td></td>
</tr>
</tbody>
</table>

6.9 Typical Characteristics
$T_A = 25°C$

Figure 1. Typical $V_{OH}$ vs $I_{OH}$ - 25°C

Figure 2. Typical $V_{OL}$ vs $I_{OL}$ - 25°C
7 Parameter Measurement Information

- Input pulse is supplied by generator having the following characteristics: PRR ≤ 10MHz, Z₀ = 50Ω.
- The outputs are measured one at a time, with one transition per measurement.

![Load Circuit](image)

(1) $C_L$ includes probe and jig capacitance.

**Table 1. Parameter Measurement Conditions**

<table>
<thead>
<tr>
<th>$V_{cc}$</th>
<th>INPUTS</th>
<th>$V_M$</th>
<th>$V_{LOAD}$</th>
<th>$C_L$</th>
<th>$R_L$</th>
<th>$V_D$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$1.8 , V \pm 0.15 , V$</td>
<td>$V_{cc}$</td>
<td>$\leq 2$ ns</td>
<td>$V_{cc}/2$</td>
<td>$2 \times V_{cc}$</td>
<td>15 pF</td>
<td>1 MΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>30 pF</td>
<td>1 kΩ</td>
</tr>
<tr>
<td>$2.5 , V \pm 0.2 , V$</td>
<td>$V_{cc}$</td>
<td>$\leq 2$ ns</td>
<td>$V_{cc}/2$</td>
<td>$2 \times V_{cc}$</td>
<td>15 pF</td>
<td>1 MΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>30 pF</td>
<td>500 Ω</td>
</tr>
<tr>
<td>$3.3 , V \pm 0.3 , V$</td>
<td>$3 , V$</td>
<td>$\leq 2.5$ ns</td>
<td>1.5 V</td>
<td>6 V</td>
<td>15 pF</td>
<td>1 MΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>50 pF</td>
<td>500 Ω</td>
</tr>
<tr>
<td>$5 , V \pm 0.5 , V$</td>
<td>$V_{cc}$</td>
<td>$\leq 2.5$ ns</td>
<td>$V_{cc}/2$</td>
<td>$2 \times V_{cc}$</td>
<td>15 pF</td>
<td>1 MΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>50 pF</td>
<td>500 Ω</td>
</tr>
</tbody>
</table>

![Voltage Waveforms](image)

(1) The maximum value of $t_{pd}$ is the worst case of $t_{PLH}$ or $t_{PHL}$.

**Figure 4. Voltage Waveforms, Propagation Delay Times, Inverting and Non-Inverting Outputs**
8 Detailed Description

8.1 Overview
The SN74LVC1G14 single Schmitt-trigger inverter is designed for 1.65 V to 5.5 V operation and performs the Boolean function \( Y = \overline{A} \). This device is fully specified for partial-power-down applications using \( I_{\text{off}} \). The \( I_{\text{off}} \) circuitry disables the outputs when the device is powered down. This inhibits current backflow into the device which prevents damage to the device.

8.2 Functional Block Diagrams

![Logic Diagram (Positive Logic)](image)

Figure 5. Logic Diagram (Positive Logic)
(DBV, DCK, DRL, DRY, DPW, and YZP Package)

![Logic Diagram (Positive Logic)](image)

Figure 6. Logic Diagram (Positive Logic)
(YZV Package)

8.3 Feature Description

8.3.1 Balanced High-Drive CMOS Push-Pull Outputs
A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the power output of the device to be limited to avoid thermal runaway and damage due to over-current. The electrical and thermal limits defined the in the Absolute Maximum Ratings must be followed at all times.

8.3.2 CMOS Schmitt-Trigger Inputs
Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the Electrical Characteristics. The worst case resistance is calculated with the maximum input voltage, given in the Absolute Maximum Ratings, and the maximum input leakage current, given in the Electrical Characteristics, using ohm’s law \( R = V \div I \).

The Schmitt-trigger input architecture provides hysteresis as define in the Electrical Characteristics, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs slowly will also increase dynamic current consumption of the device.
Feature Description (continued)

8.3.3 Clamp Diodes

The inputs and outputs to this device have negative clamping diodes.

<table>
<thead>
<tr>
<th>CAUTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltages beyond the values specified in the <strong>Absolute Maximum Ratings</strong> table can cause damage to the device. The input negative-voltage and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.</td>
</tr>
</tbody>
</table>

![Figure 7. Electrical Placement of Clamping Diodes for Each Input and Output](image)

8.3.4 Partial Power Down (\(I_{\text{off}}\))

The inputs and outputs for this device enter a high impedance state when the supply voltage is 0 V. The maximum leakage into or out of any input or output pin on the device is specified by \(I_{\text{off}}\) in the **Electrical Characteristics**.

8.3.5 Over-Voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the **Absolute Maximum Ratings**.

8.4 Device Functional Modes

Table 2 lists the functional modes of the SN74LVC1G14 device.

<table>
<thead>
<tr>
<th>Table 2. Function Table</th>
</tr>
</thead>
<tbody>
<tr>
<td>INPUT A</td>
</tr>
<tr>
<td>H</td>
</tr>
<tr>
<td>L</td>
</tr>
</tbody>
</table>
9 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information
Mechanical input elements, such as push buttons or rotary knobs, offer simple ways to interact with electronic systems. Typically, these elements have recoil or bouncing, where the mechanical element makes and breaks contact multiple times during human interaction. This bouncing can cause one or more repeated signals to be passed, triggering multiple actions when only a single input was intended. One potential solution to mitigating these multiple inputs is by utilizing a Schmitt-trigger to create a debounce circuit. Figure 8 shows an example of this solution.

9.2 Typical Application
The input due to the push button switches multiple times, causing the output of a non Schmitt-trigger device to trigger multiple times, while the Schmitt-trigger input device with RC delay limits the output pulse to a single pulse desired by the user. The separated positive and negative input voltage threshold values, see Figure 9, prevent multiple triggers from occurring.

9.2.1 Design Requirements
This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive also creates fast edges into light loads so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure
1. Recommended Input Conditions:
   - For specified high and low levels, see (\(V_{T+}\) and \(V_{T-}\)) in the Recommended Operating Conditions table.
   - Inputs are overvoltage tolerant allowing them to go as high as (\(V_i\) max) in the Recommended Operating Conditions table at any valid \(V_{CC}\).
2. Recommended Output Conditions:
   - Load currents should not exceed (\(I_O\ max\)) per output and should not exceed (Continuous current through \(V_{CC}\) or GND) total current for the part. These limits are located in the Absolute Maximum Ratings table.

Figure 8. Push Button Debounce Circuit Schematic
Typical Application (continued)

9.2.3 Application Curve

Figure 9 is created from the values given in the Electrical Characteristics. Linear interpolation shows the values between each given point.

![Interpolated Threshold Voltages vs. VCC](image)

**Figure 9. Interpolated Threshold Voltages vs. VCC**

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the Recommended Operating Conditions table.

The $V_{CC}$ pin must have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended, and it is ok to parallel multiple bypass caps to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

Even low data rate digital signals can contain high-frequency signal components due to fast edge rates. When a printed-circuit board (PCB) trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

An example layout is given in Figure 10 for the DPW (X2SON-5) package. This example layout includes a 0402 (metric) capacitor and uses the measurements found in the example board layout appended to this end of this datasheet. A via of diameter 0.1 mm (3.973 mil) is placed directly in the center of the device. This via can be used to trace out the center pin connection through another board layer, or it can be left out of the layout.
11.2 Layout Example

![Diagram of Example Layout With DPW (X2SON-5) Package]

Figure 10. Example Layout With DPW (X2SON-5) Package
12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation
For related documentation see the following:

*Implications of Slow or Floating CMOS Inputs*

12.2 Receiving Notification of Documentation Updates
To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources
The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks
NanoFree, E2E are trademarks of Texas Instruments. All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

**SLYZ022 — TI Glossary.**

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead finish/ Ball material</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN74LVC1G14DBVR</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>3000</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>(C145, C14F, C14J, C14K, C14R) (C14H, C14S)</td>
</tr>
<tr>
<td>SN74LVC1G14DBRE4</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>3000</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td></td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>C14F</td>
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<td>3000</td>
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<td>NIPDAU</td>
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<td>SN74LVC1G14DBVT</td>
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<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>250</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>SN</td>
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<td>-40 to 125</td>
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<td>DBV</td>
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<td>250</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
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<tr>
<td>SN74LVC1G14DCKR</td>
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<td>SC70</td>
<td>DCK</td>
<td>5</td>
<td>3000</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>(CF5, CFF, CFJ, CFK, CFR, CFT) (CFH, CFS)</td>
</tr>
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<td>NIPDAU</td>
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<td>-40 to 125</td>
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<td>NIPDAU</td>
<td>SN</td>
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<td>NIPDAU</td>
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<td>CF5</td>
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<td>SC70</td>
<td>DCK</td>
<td>5</td>
<td>250</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
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<td>-40 to 125</td>
<td>CF5</td>
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<td>SN74LVC1G14DPWR</td>
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<td>X2SON</td>
<td>DPW</td>
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<td>3000</td>
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<td></td>
<td>Level-1-260C-UNLIM</td>
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<td>9H</td>
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<td>DRL</td>
<td>5</td>
<td>4000</td>
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<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>(CF7, CFR)</td>
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<tr>
<td>SN74LVC1G14DRLRG4</td>
<td>ACTIVE</td>
<td>SOT-5X3</td>
<td>DRL</td>
<td>5</td>
<td>4000</td>
<td>RoHS &amp; Green</td>
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<td>(CF7, CFR)</td>
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<td>-40 to 125</td>
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<td>Package Type</td>
<td>Package Drawing</td>
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<td>Package Qty</td>
<td>Package Qty</td>
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<td>MSL Peak Temp (3)</td>
<td>Op Temp (°C)</td>
<td>Device Marking (4/5)</td>
<td>Samples</td>
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<td>DSBGA</td>
<td>YZP</td>
<td>5</td>
<td>3000</td>
<td>RoHS &amp; Green</td>
<td>SNAGCU Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>CF7, CFN</td>
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<td>-40 to 85</td>
<td>CF</td>
<td>(7, N)</td>
<td>Samples</td>
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</table>

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC1G14:
• Automotive: SN74LVC1G14-Q1

• Enhanced Product: SN74LVC1G14-EP

NOTE: Qualified Version Definitions:

• Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

• Enhanced Product - Supports Defense, Aerospace and Medical Applications
### TAPE AND REEL INFORMATION

#### REEL DIMENSIONS

- **Reel Diameter**
- **Reel Width (W1)**

#### TAPE DIMENSIONS

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

#### TAPE AND REEL INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
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*All dimensions are nominal*
### TAPE AND REEL BOX DIMENSIONS

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<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
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*All dimensions are nominal*
Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).
NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
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2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.
NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.
4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.
D: Max = 0.918 mm, Min = 0.858 mm
E: Max = 0.918 mm, Min = 0.858 mm

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

2. This drawing is subject to change without notice.

3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

4. Reference JEDEC registration MO-293 Variation UAAD-1.
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.
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