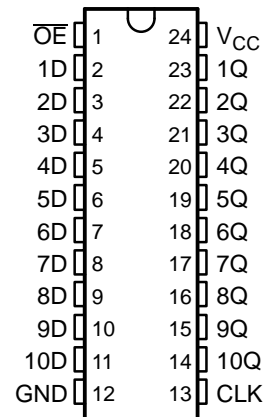


FEATURES

- Operates From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 7.3 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22 – 2000-V Human-Body Model (A114-A)

DB, DGV, DW, NS, OR PW PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

This 10-bit bus-interface flip-flop is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC821A features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. This device is particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The ten flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs.

A buffered output-enable (\overline{OE}) input can be used to place the ten outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

\overline{OE} does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

ORDERING INFORMATION

| T_A | PACKAGE ⁽¹⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|------------------------|-----------------|-----------------------|------------------|
| –40°C to 85°C | SOIC – DW | Tube of 25 | SN74LVC821ADW | LVC821A |
| | | Reel of 2000 | SN74LVC821ADWR | |
| | SOP – NS | Reel of 2000 | SN74LVC821ANSR | LVC821A |
| | SSOP – DB | Reel of 2000 | SN74LVC821ADBR | LC821A |
| | TSSOP – PW | Tube of 60 | SN74LVC821APW | LC821A |
| | | Reel of 2000 | SN74LVC821APWR | |
| | | Reel of 250 | SN74LVC821APWT | |
| TVSOP – DGV | Reel of 2000 | SN74LVC821ADGVR | LC821A | |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SN74LVC821A
10-BIT BUS-INTERFACE FLIP-FLOP
WITH 3-STATE OUTPUTS

SCAS304J—MARCH 1993—REVISED FEBRUARY 2005

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

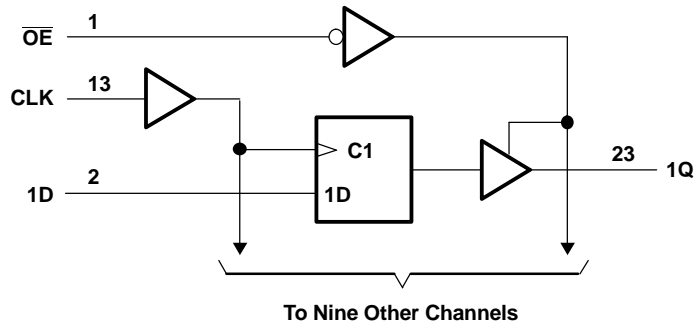
This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE
(EACH FLIP-FLOP)

| INPUTS | | | OUTPUT |
|-----------------|--------|---|--------|
| \overline{OE} | CLK | D | Q |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | H or L | X | Q_0 |
| H | X | X | Z |

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|------------------|---|--------------------|-----------------------|------|
| V _{CC} | Supply voltage range | −0.5 | 6.5 | V |
| V _I | Input voltage range ⁽²⁾ | −0.5 | 6.5 | V |
| V _O | Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾ | −0.5 | 6.5 | V |
| V _O | Voltage range applied to any output in the high or low state ⁽²⁾⁽³⁾ | −0.5 | V _{CC} + 0.5 | V |
| I _{IK} | Input clamp current | V _I < 0 | −50 | mA |
| I _{OK} | Output clamp current | V _O < 0 | −50 | mA |
| I _O | Continuous output current | | ±50 | mA |
| | Continuous current through V _{CC} or GND | | ±100 | mA |
| θ _{JA} | Package thermal impedance ⁽⁴⁾ | DB package | 63 | °C/W |
| | | DGV package | 86 | |
| | | DW package | 46 | |
| | | NS package | 65 | |
| | | PW package | 88 | |
| T _{stg} | Storage temperature range | −65 | 150 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

| | | MIN | MAX | UNIT | |
|-----------------|------------------------------------|------------------------------------|------------------------|------------------------|----|
| V _{CC} | Supply voltage | Operating | 1.65 | 3.6 | V |
| | | Data retention only | 1.5 | | |
| V _{IH} | High-level input voltage | V _{CC} = 1.65 V to 1.95 V | 0.65 × V _{CC} | | V |
| | | V _{CC} = 2.3 V to 2.7 V | 1.7 | | |
| | | V _{CC} = 2.7 V to 3.6 V | 2 | | |
| V _{IL} | Low-level input voltage | V _{CC} = 1.65 V to 1.95 V | | 0.35 × V _{CC} | V |
| | | V _{CC} = 2.3 V to 2.7 V | | 0.7 | |
| | | V _{CC} = 2.7 V to 3.6 V | | 0.8 | |
| V _I | Input voltage | 0 | 5.5 | V | |
| V _O | Output voltage | High or low state | 0 | V _{CC} | V |
| | | 3-state | 0 | 5.5 | |
| I _{OH} | High-level output current | V _{CC} = 1.65 V | | −4 | mA |
| | | V _{CC} = 2.3 V | | −8 | |
| | | V _{CC} = 2.7 V | | −12 | |
| | | V _{CC} = 3 V | | −24 | |
| I _{OL} | Low-level output current | V _{CC} = 1.65 V | | 4 | mA |
| | | V _{CC} = 2.3 V | | 8 | |
| | | V _{CC} = 2.7 V | | 12 | |
| | | V _{CC} = 3 V | | 24 | |
| Δt/Δv | Input transition rise or fall rate | | 10 | ns/V | |
| T _A | Operating free-air temperature | −40 | 85 | °C | |

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74LVC821A

10-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS

SCAS304J–MARCH 1993–REVISED FEBRUARY 2005

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|------------------|--------------------------|--|-----------------|-----------------------|--------------------|------|------|
| V _{OH} | | I _{OH} = -100 μA | 1.65 V to 3.6 V | V _{CC} - 0.2 | | | V |
| | | I _{OH} = -4 mA | 1.65 V | 1.2 | | | |
| | | I _{OH} = -8 mA | 2.3 V | 1.7 | | | |
| | | I _{OH} = -12 mA | 2.7 V | 2.2 | | | |
| | | | 3 V | 2.4 | | | |
| | I _{OH} = -24 mA | 3 V | 2.2 | | | | |
| V _{OL} | | I _{OL} = 100 μA | 1.65 V to 3.6 V | | | 0.2 | V |
| | | I _{OL} = 4 mA | 1.65 V | | | 0.45 | |
| | | I _{OL} = 8 mA | 2.3 V | | | 0.7 | |
| | | I _{OL} = 12 mA | 2.7 V | | | 0.4 | |
| | | I _{OL} = 24 mA | 3 V | | | 0.55 | |
| I _I | | V _I = 0 to 5.5 V | 3.6 V | | | ±5 | μA |
| I _{off} | | V _I or V _O = 5.5 V | 0 | | | ±10 | μA |
| I _{OZ} | | V _O = 0 to 5.5 V | 3.6 V | | | ±10 | μA |
| I _{CC} | | V _I = V _{CC} or GND | 3.6 V | I _O = 0 | | 10 | μA |
| | | 3.6 V ≤ V _I ≤ 5.5 V ⁽²⁾ | | | | 10 | |
| ΔI _{CC} | | One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND | 2.7 V to 3.6 V | | | 500 | μA |
| C _i | Control inputs | V _I = V _{CC} or GND | 3.3 V | | | 5 | pF |
| | Data inputs | | | | | 4 | |
| C _o | | V _O = V _{CC} or GND | 3.3 V | | | 7 | pF |

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

(2) This applies in the disabled state only.

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| | | V _{CC} = 1.8 V ± 0.15 V | | V _{CC} = 2.5 V ± 0.2 V | | V _{CC} = 2.7 V | | V _{CC} = 3.3 V ± 0.3 V | | UNIT |
|--------------------|---------------------------------|-------------------------------------|-----|------------------------------------|-----|-------------------------|-----|------------------------------------|-----|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| f _{clock} | Clock frequency | (1) | | (1) | | 150 | | 150 | | MHz |
| t _w | Pulse duration, CLK high or low | (1) | | (1) | | 3.3 | | 3.3 | | ns |
| t _{su} | Setup time, data before CLK | (1) | | (1) | | 1.9 | | 1.9 | | ns |
| t _h | Hold time, data after CLK | (1) | | (1) | | 1.5 | | 1.5 | | ns |

(1) This information was not available at the time of publication.

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$ | | $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ | | $V_{CC} = 2.7\text{ V}$ | | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | | UNIT |
|-------------|-----------------|----------------|---|-----|--|-----|-------------------------|-----|--|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| f_{max} | | | (1) | | (1) | | 150 | | 150 | | MHz |
| t_{pd} | CLK | Q | (1) | (1) | (1) | (1) | 8.5 | | 2.2 | 7.3 | ns |
| t_{en} | \overline{OE} | Q | (1) | (1) | (1) | (1) | 8.8 | | 1.3 | 7.6 | ns |
| t_{dis} | \overline{OE} | Q | (1) | (1) | (1) | (1) | 6.8 | | 1.6 | 6.2 | ns |
| $t_{sk(o)}$ | | | | | | | | | | 1 | ns |

(1) This information was not available at the time of publication.

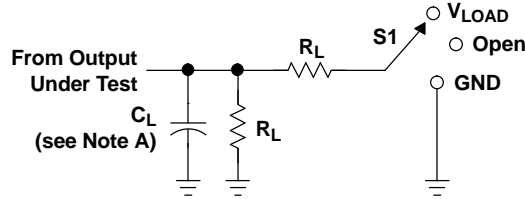
Operating Characteristics

$T_A = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | $V_{CC} = 1.8\text{ V}$ | $V_{CC} = 2.5\text{ V}$ | $V_{CC} = 3.3\text{ V}$ | UNIT |
|-----------|--|--------------------|-------------------------|-------------------------|-------------------------|------|
| | | | TYP | TYP | TYP | |
| C_{pd} | Power dissipation capacitance per flip-flop | Outputs enabled | (1) | (1) | 65 | pF |
| | | Outputs disabled | (1) | (1) | 48 | |

(1) This information was not available at the time of publication.

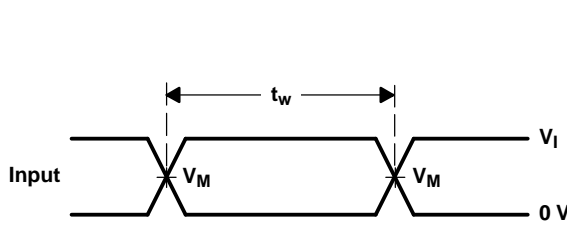
PARAMETER MEASUREMENT INFORMATION



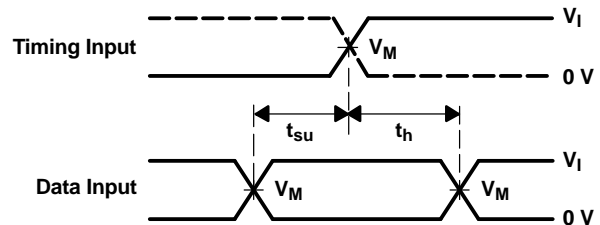
LOAD CIRCUIT

| TEST | S1 |
|-------------------|------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | V_{LOAD} |
| t_{PHZ}/t_{PZH} | GND |

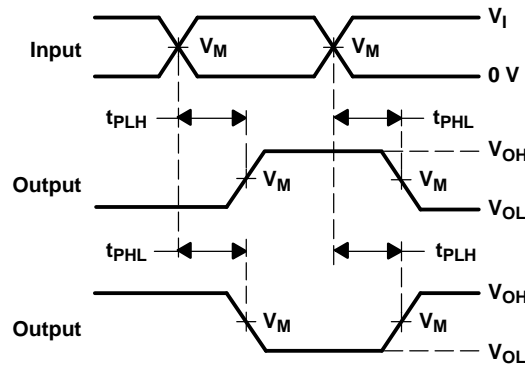
| V_{CC} | INPUTS | | V_M | V_{LOAD} | C_L | R_L | V_{Δ} |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
| | V_I | t_r/t_f | | | | | |
| $1.8\text{ V} \pm 0.15\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k Ω | 0.15 V |
| $2.5\text{ V} \pm 0.2\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| 2.7 V | 2.7 V | $\leq 2.5\text{ ns}$ | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| $3.3\text{ V} \pm 0.3\text{ V}$ | 2.7 V | $\leq 2.5\text{ ns}$ | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |



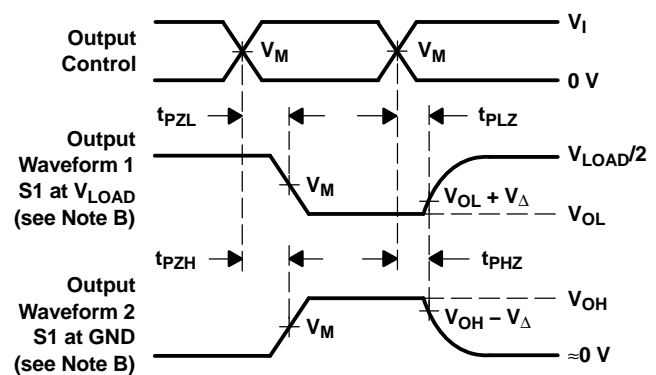
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74LVC821ADBR | ACTIVE | SSOP | DB | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LC821A | Samples |
| SN74LVC821ADBRG4 | ACTIVE | SSOP | DB | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LC821A | Samples |
| SN74LVC821ADGVR | ACTIVE | TVSOP | DGV | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LC821A | Samples |
| SN74LVC821ADW | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVC821A | Samples |
| SN74LVC821ADWG4 | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVC821A | Samples |
| SN74LVC821ADWR | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVC821A | Samples |
| SN74LVC821APW | ACTIVE | TSSOP | PW | 24 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LC821A | Samples |
| SN74LVC821APWR | ACTIVE | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LC821A | Samples |
| SN74LVC821APWRE4 | ACTIVE | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LC821A | Samples |
| SN74LVC821APWT | ACTIVE | TSSOP | PW | 24 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LC821A | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC821ADBR | SSOP | DB | 24 | 2000 | 330.0 | 16.4 | 8.2 | 8.8 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LVC821ADGVR | TVSOP | DGV | 24 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LVC821ADWR | SOIC | DW | 24 | 2000 | 330.0 | 24.4 | 10.75 | 15.7 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74LVC821APWR | TSSOP | PW | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |
| SN74LVC821APWT | TSSOP | PW | 24 | 250 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC821ADBR | SSOP | DB | 24 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74LVC821ADGVR | TVSOP | DGV | 24 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74LVC821ADWR | SOIC | DW | 24 | 2000 | 350.0 | 350.0 | 43.0 |
| SN74LVC821APWR | TSSOP | PW | 24 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74LVC821APWT | TSSOP | PW | 24 | 250 | 367.0 | 367.0 | 38.0 |

PW0024A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220208/A 02/2017

NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

DW (R-PDSO-G24)

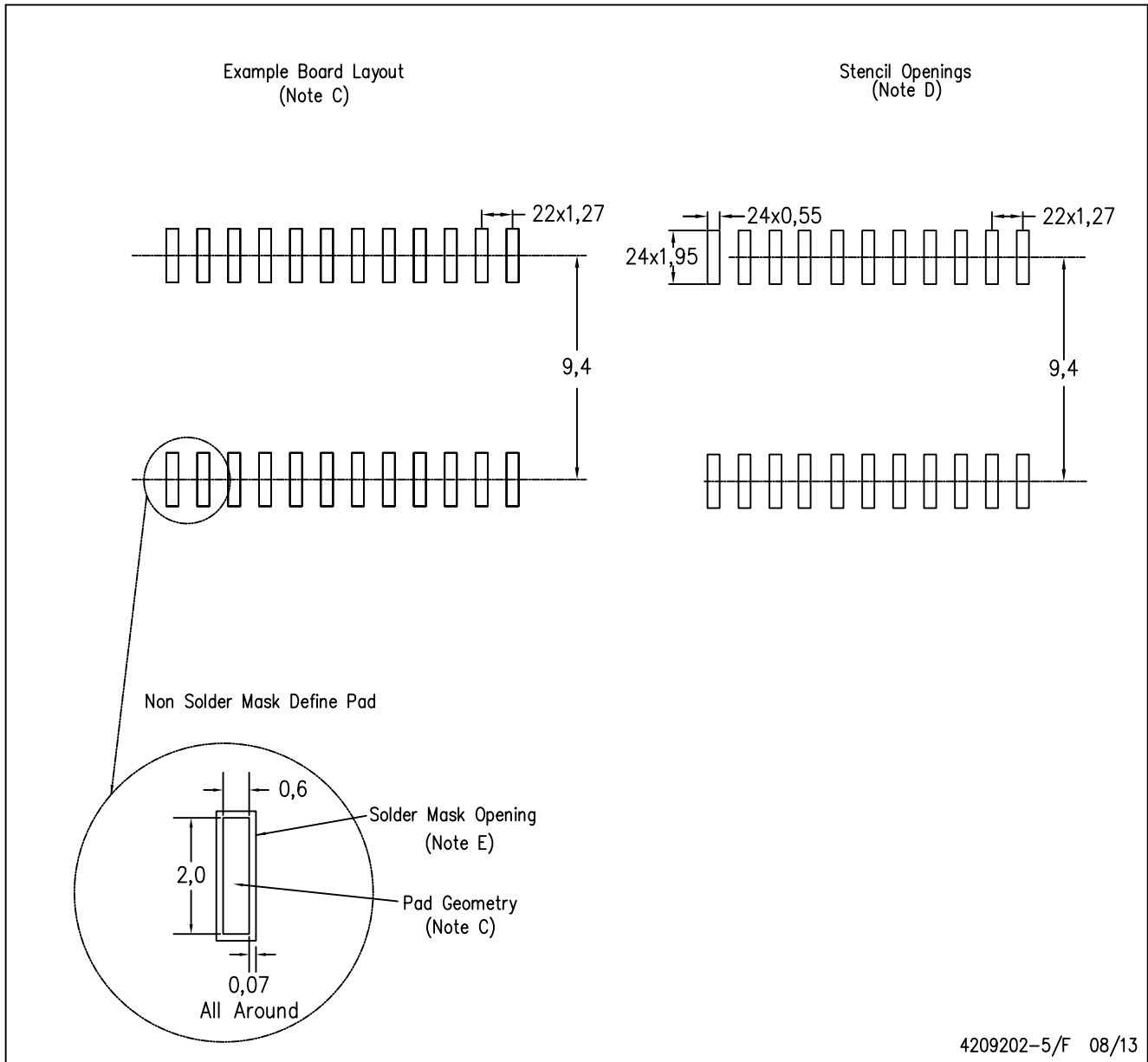
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AD.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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