



SN74LVCHR16245A 16-Bit Bus Transceiver With 3-State Outputs

1 Features

- Member of the Texas Instruments Widebus™ Family
- Operates From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 4.8 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- Bus Hold on Data Inputs Eliminates the Need for External Pullup or Pulldown Resistors
- All Outputs Have Equivalent 26- Ω Series Resistors, So No External Resistors Are Required
- I_{off} Supports Live Insertion, Partial Power-Down Mode, and Back-Drive Protection
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model
 - 200-V Machine Model

2 Applications

- Telecom Infrastructures
- Industrial Transport
- Wireless Infrastructures
- Servers
- Tests and Measurements

3 Description

This 16-bit (dual-octal) noninverting bus transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVCHR16245A device is designed for asynchronous communication between data buses. The control-function implementation minimizes external-timing requirements.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVCHR16245A	TSSOP (48)	12.50 mm × 6.10 mm
	SSOP (48)	15.88 mm × 7.49 mm
	TVSOP (48)	9.70 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic

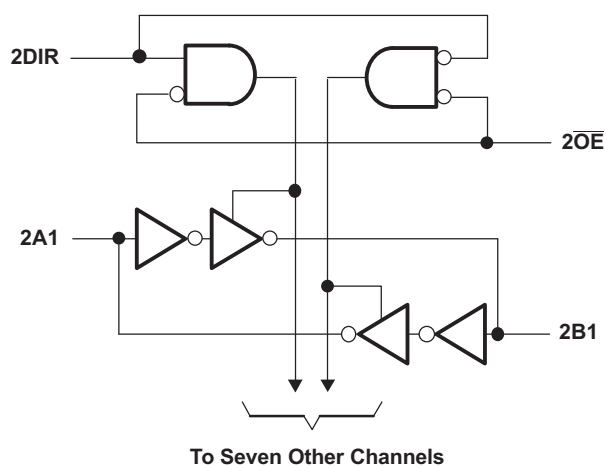
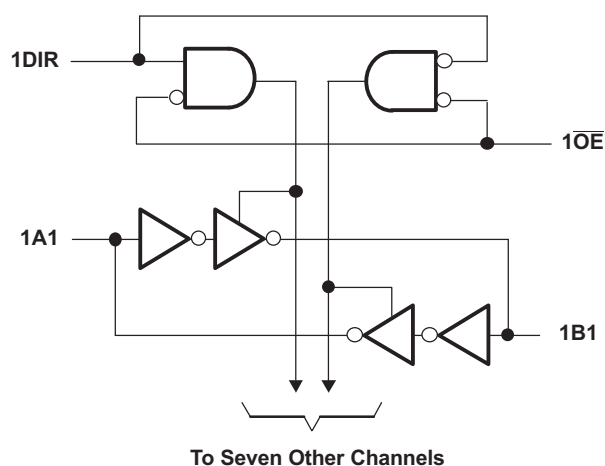


Table of Contents

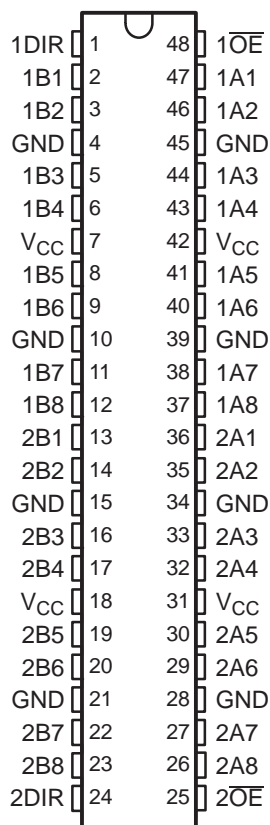
1 Features	1	9.1 Overview	11
2 Applications	1	9.2 Functional Block Diagram	11
3 Description	1	9.3 Feature Description	12
4 Simplified Schematic	1	9.4 Device Functional Modes	12
5 Revision History	2	10 Application and Implementation	13
6 Pin Configuration and Functions	3	10.1 Application Information	13
7 Specifications	6	10.2 Typical Application	13
7.1 Absolute Maximum Ratings	6	11 Power Supply Recommendations	15
7.2 Handling Ratings	6	12 Layout	15
7.3 Recommended Operating Conditions	7	12.1 Layout Guidelines	15
7.4 Thermal Information	7	12.2 Layout Example	15
7.5 Electrical Characteristics	8	13 Device and Documentation Support	16
7.6 Switching Characteristics	9	13.1 Trademarks	16
7.7 Operating Characteristics	9	13.2 Electrostatic Discharge Caution	16
7.8 Typical Characteristics	9	13.3 Glossary	16
8 Parameter Measurement Information	10	14 Mechanical, Packaging, and Orderable Information	16
9 Detailed Description	11		

5 Revision History

Changes from Revision P (December 2005) to Revision Q	Page
• Updated document to new TI data sheet format.	1
• Removed Ordering Information table.	1
• Changed I_{off} bullet in Features.	1
• Added Applications.	1
• Added Pin Functions table.	3
• Added Handling Ratings table.	6
• Changed MAX operating temperature to 125°C in Recommended Operating Conditions table.	7
• Added Thermal Information table.	7
• Added Typical Characteristics.	9
• Added Detailed Description section.	11
• Added Application and Implementation section.	13
• Added Power Supply Recommendations and Layout sections.	15

6 Pin Configuration and Functions

**DGG, DGV, OR DL PACKAGE
(TOP VIEW)**



Pin Functions

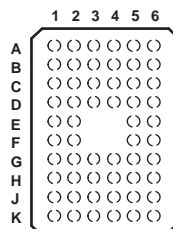
PIN		I/O	DESCRIPTION
NO.	NAME		
1	1DIR	I	Direction pin 1
2	1B1	I/O	1B1 input or output
3	1B2	I/O	1B2 input or output
4	GND	—	Ground pin
5	1B3	I/O	1B3 input or output
6	1B4	I/O	1B4 input or output
7	V _{CC}	—	Power pin
8	1B5	I/O	1B5 input or output
9	1B6	I/O	1B6 input or output
10	GND	—	Ground pin
11	1B7	I/O	1B7 input or output
12	1B8	I/O	1B8 input or output
13	2B1	I/O	2B1 input or output
14	2B2	I/O	2B2 input or output
15	GND	—	Ground pin
16	2B3	I/O	2B3 input or output
17	2B4	I/O	2B4 input or output
18	V _{CC}	—	Power pin

SN74LVCHR16245A

SCAS582Q – NOVEMBER 1996 – REVISED OCTOBER 2014

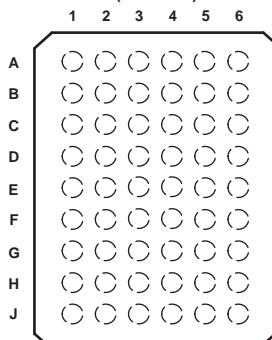
www.ti.com
Pin Functions (continued)

PIN		I/O	DESCRIPTION
NO.	NAME		
19	2B5	I/O	2B5 input or output
20	2B6	I/O	2B6 input or output
21	GND	—	Ground pin
22	2B7	I/O	2B7 input or output
23	2B8	I/O	2B8 input or output
24	2DIR	I	Direction pin 2
25	2OE	I	Output Enable 2
26	2A8	I/O	2A8 input or output
27	2A7	I/O	2A7 input or output
28	GND	—	Ground pin
29	2A6	I/O	2A6 input or output
30	2A5	I/O	2A5 input or output
31	V _{CC}	—	Power pin
32	2A4	I/O	2A4 input or output
33	2A3	I/O	2A3 input or output
34	GND	—	Ground pin
35	2A2	I/O	2A2 input or output
36	2A1	I/O	2A1 input or output
37	1A8	I/O	1A8 input or output
38	1A7	I/O	1A7 input or output
39	GND	—	Ground pin
40	1A6	I/O	1A6 input or output
41	1A5	I/O	1A5 input or output
42	V _{CC}	—	Power pin
43	1A4	I/O	1A4 input or output
44	1A3	I/O	1A3 input or output
45	GND	—	Ground pin
46	1A2	I/O	1A2 input or output
47	1A1	I/O	1A1 input or output
48	1OE	I	Output Enable 1

**GQL OR ZQL PACKAGE
(TOP VIEW)**

**Table 1. Pin Assignments⁽¹⁾
(56-Ball GQL or ZQL Package)**

	1	2	3	4	5	6
A	1DIR	NC	NC	NC	NC	1 $\overline{\text{OE}}$
B	1B2	1B1	GND	GND	1A1	1A2
C	1B4	1B3	V _{CC}	V _{CC}	1A3	1A4
D	1B6	1B5	GND	GND	1A5	1A6
E	1B8	1B7			1A7	1A8
F	2B1	2B2			2A2	2A1
G	2B3	2B4	GND	GND	2A4	2A3
H	2B5	2B6	V _{CC}	V _{CC}	2A6	2A5
J	2B7	2B8	GND	GND	2A8	2A7
K	2DIR	NC	NC	NC	NC	2 $\overline{\text{OE}}$

(1) NC – No internal connection

**GRD OR ZRD PACKAGE
(TOP VIEW)**

**Table 2. Pin Assignments⁽¹⁾
(54-Ball GRD or ZRD Package)**

	1	2	3	4	5	6
A	1B1	NC	1DIR	1 $\overline{\text{OE}}$	NC	1A1
B	1B3	1B2	NC	NC	1A2	1A3
C	1B5	1B4	V _{CC}	V _{CC}	1A4	1A5
D	1B7	1B6	GND	GND	1A6	1A7
E	2B1	1B8	GND	GND	1A8	2A1
F	2B3	2B2	GND	GND	2A2	2A3
G	2B5	2B4	V _{CC}	V _{CC}	2A4	2A5
H	2B7	2B6	NC	NC	2A6	2A7
J	2B8	NC	2DIR	2 $\overline{\text{OE}}$	NC	2A8

(1) NC – No internal connection

7 Specifications

7.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	–0.5	6.5	V
V _I	Input voltage range ⁽²⁾	–0.5	6.5	V
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	–0.5	6.5	V
V _O	Voltage range applied to any output in the high or low state ⁽²⁾⁽³⁾	–0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		–50 mA
I _{OK}	Output clamp current	V _O < 0		–50 mA
I _O	Continuous output current		±50	mA
	Continuous current through each V _{CC} or GND		±100	mA

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

7.2 Handling Ratings

		MIN	MAX	UNIT
T _{stg}	Storage temperature range	−65	150	°C
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾		V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾		

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	Operating	1.65	3.6
		Data retention only	1.5	
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	
		V _{CC} = 2.3 V to 2.7 V	1.7	
		V _{CC} = 2.7 V to 3.6 V	2	
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}	
		V _{CC} = 2.3 V to 2.7 V	0.7	
		V _{CC} = 2.7 V to 3.6 V	0.8	
V _I	Input voltage	0	5.5	V
V _O	Output voltage	High or low state	0	V _{CC}
		3-state	0	5.5
I _{OH}	High-level output current	V _{CC} = 1.65 V	–2	
		V _{CC} = 2.3 V	–4	
		V _{CC} = 2.7 V	–8	
		V _{CC} = 3 V	–12	
I _{OL}	Low-level output current	V _{CC} = 1.65 V	2	
		V _{CC} = 2.3 V	4	
		V _{CC} = 2.7 V	8	
		V _{CC} = 3 V	12	
Δt/Δv	Input transition rise or fall rate		10	ns/V
T _A	Operating free-air temperature	–40	125	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74LVCHR16245A			UNIT
		DGG	DGV	DL	
		48 PINS			
R _{θJA}	Junction-to-ambient thermal resistance	64.3	78.4	68.4	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	17.6	30.7	34.7	
R _{θJB}	Junction-to-board thermal resistance	31.5	41.8	41.0	
ψ _{JT}	Junction-to-top characterization parameter	1.1	3.8	12.3	
ψ _{JB}	Junction-to-board characterization parameter	31.2	41.3	40.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}		I _{OH} = −100 μA		1.65 V to 3.6 V	V _{CC} − 0.2			V
		I _{OH} = −2 mA		1.65 V	1.2			
		I _{OH} = −4 mA		2.3 V	1.7			
			2.7 V	2.2				
		I _{OH} = −6 mA		3 V	2.4			
		I _{OH} = −8 mA		2.7 V	2			
		I _{OH} = −12 mA		3 V	2			
V _{OL}		I _{OL} = 100 μA		1.65 V to 3.6 V			0.2	V
		I _{OL} = 2 mA		1.65 V			0.45	
		I _{OL} = 4 mA		2.3 V			0.7	
			2.7 V			0.4		
		I _{OL} = 6 mA		3 V			0.55	
		I _{OL} = 8 mA		2.7 V			0.6	
		I _{OL} = 12 mA		3 V			0.8	
I _I	Control inputs	V _I = 0 to 5.5 V		3.6 V			±5	μA
I _{I(hold)}	A or B port	V _I = 0.58 V		1.65 V	15		μA	
		V _I = 1.07 V			−15			
		V _I = 0.7 V		2.3 V	45			
		V _I = 1.7 V			−45			
		V _I = 0.8 V		3 V	75			
		V _I = 2 V			−75			
		V _I = 0 to 3.6 V ⁽²⁾		3.6 V	±500			
I _{off}		V _I or V _O = 5.5 V		0			±10	μA
I _{OZ} ⁽³⁾		V _O = 0 V or (V _{CC} to 5.5 V)		2.3 V to 3.6 V			±5	μA
I _{CC}		V _I = V _{CC} or GND		3.6 V			20	μA
		3.6 V ≤ V _I ≤ 5.5 V ⁽⁴⁾					20	
ΔI _{CC}		One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND		2.7 V to 3.6 V			500	μA
C _i	Control inputs	V _I = V _{CC} or GND		3.3 V			3	pF
C _{io}	A or B port	V _O = V _{CC} or GND		3.3 V			12	pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

(3) For the total leakage current in an I/O port, please consult the I_{I(hold)} specification for the input voltage condition 0 V < V_I < V_{CC}, and the I_{OZ} specification for the input voltage conditions V_I = 0 V or V_I = V_{CC} to 5.5 V. The bus-hold current, at input voltages greater than V_{CC}, is negligible.

(4) This applies in the disabled state only.

7.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

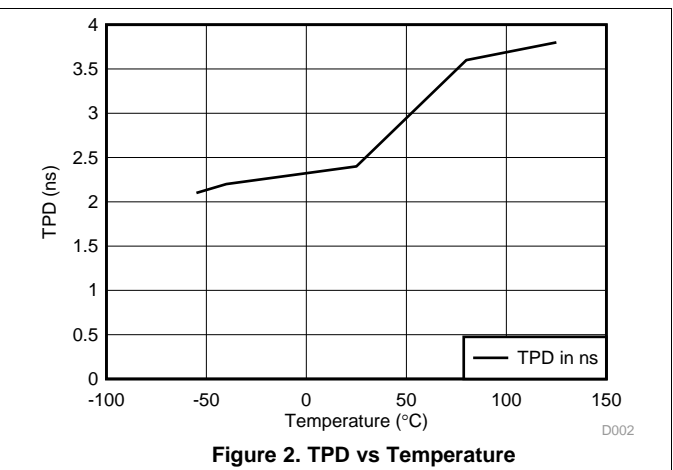
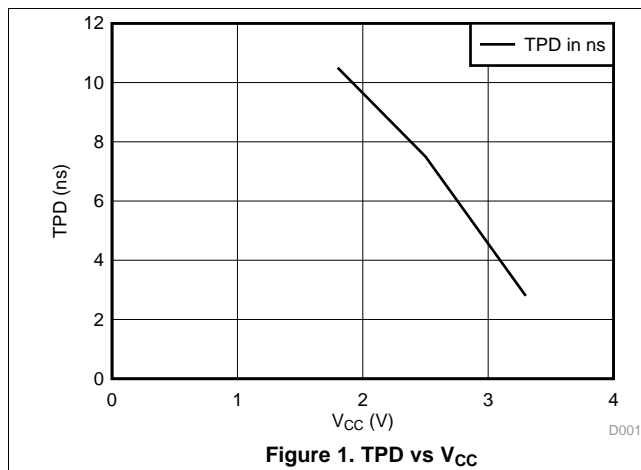
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	1	12.5	1	9.5	1	5.7	1.5	4.8	ns
t_{en}	\overline{OE}	A or B	1	15.8	1	12.2	1	7.9	1.5	6.3	ns
t_{dis}	\overline{OE}	A or B	1	19.2	1	11.9	1	8.3	2.2	7.4	ns

7.7 Operating Characteristics

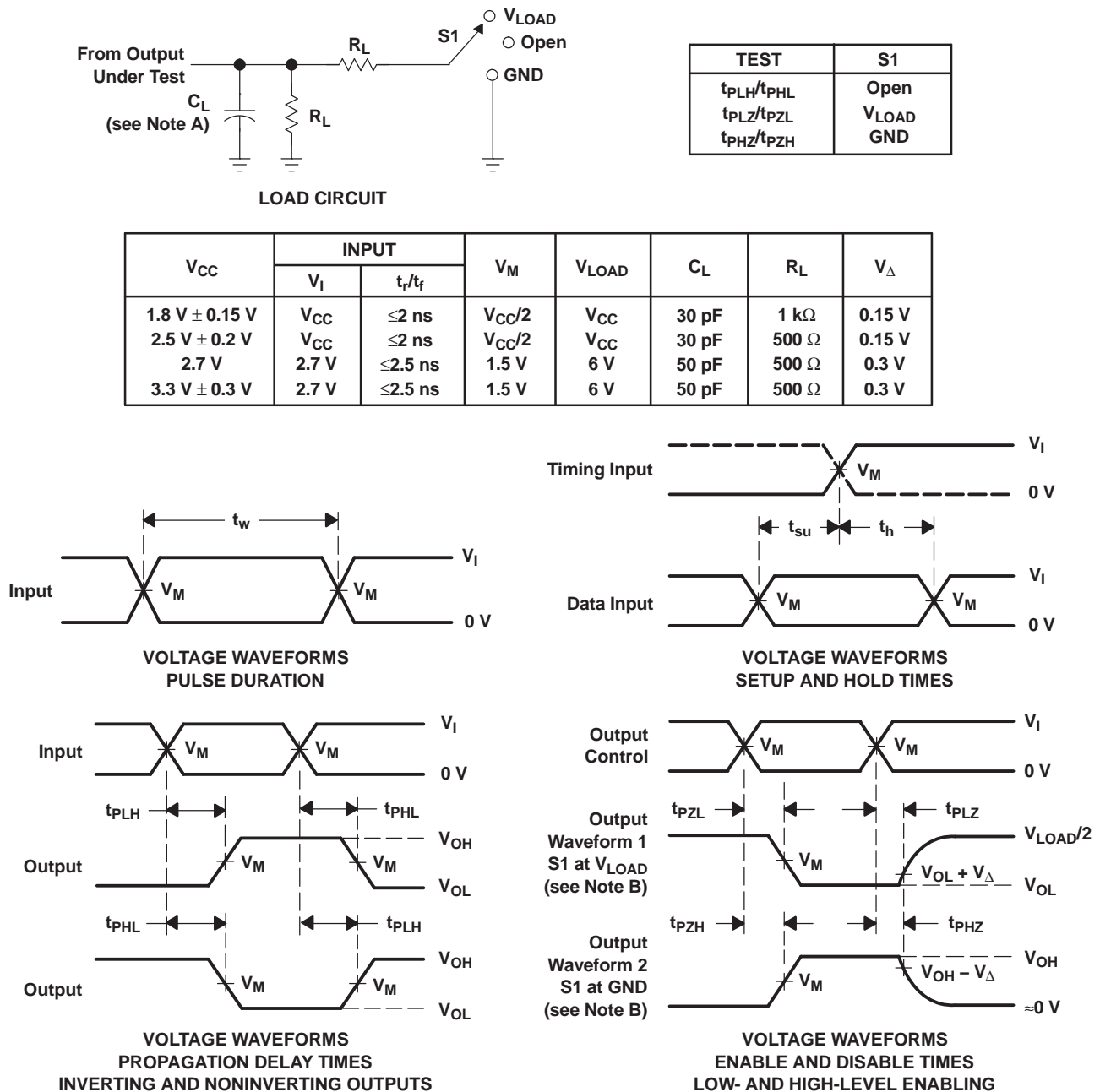
$T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	UNIT
				TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	$f = 10\text{ MHz}$	36	36	39	pF
		Outputs disabled		3	3	4	

7.8 Typical Characteristics



8 Parameter Measurement Information



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

9.3 Feature Description

- Wide operating voltage range
 - Operates from 1.65 V to 3.6 V
- Allows down voltage translation
 - Inputs accept voltages to 5.5 V
- I_{off} feature
 - Allows voltages on the inputs and outputs when V_{CC} is 0 V
- All outputs have equivalent 26- Ω series resistors, so no external resistors are required
- Bus hold on data inputs eliminates the need for external pullup or pulldown resistors

9.4 Device Functional Modes

Table 3. Function Table⁽¹⁾
(Each 8-bit Section)

CONTROL INPUTS		OUTPUT CIRCUITS		OPERATION
\overline{OE}	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A bus
L	H	Hi-Z	Enabled	A data to B bus
H	X	Hi-Z	Hi-Z	Isolation

(1) Input circuits of the data I/Os always are active.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The SN74LVCHR16245A device is a 16-bit bidirectional transceiver. This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so that the buses are effectively isolated. The device has 5.5-V tolerant inputs at any valid V_{CC} which allows the device to be used in multi-power systems and used for down translation. All outputs have equivalent 26- Ω series resistors, so no external resistors are required. The Bus Hold feature eliminates the need for external pullup or pulldown resistors on unused or floating inputs.

10.2 Typical Application

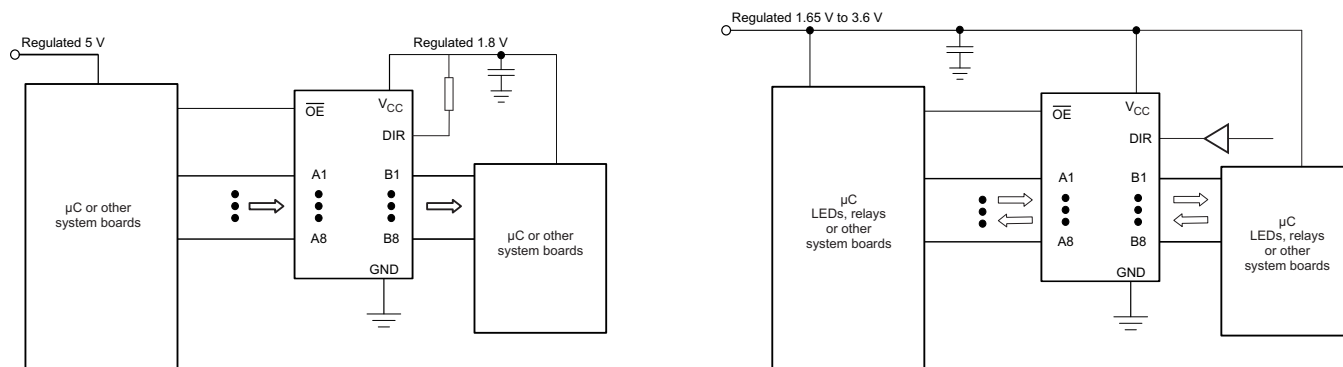


Figure 5. Typical Application Schematic

10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

Typical Application (continued)

10.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
 - Rise time and fall time specifications, see $\Delta t/\Delta V$ in the [Recommended Operating Conditions](#) table.
 - Specified high and low levels, see V_{IH} and V_{IL} in the [Recommended Operating Conditions](#) table.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC} .
2. Recommend Output Conditions:
 - Load currents should not exceed 50 mA per output and 100 mA total for the part.
 - Outputs should not be pulled above V_{CC} .

10.2.3 Application Curves

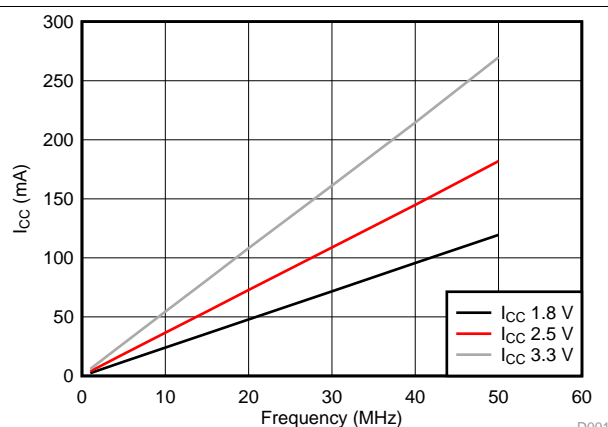


Figure 6. I_{CC} vs Frequency

D001

11 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended. If there are multiple V_{CC} pins, 0.01 μF or 0.022 μF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

12 Layout

12.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in [Figure 7](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

12.2 Layout Example

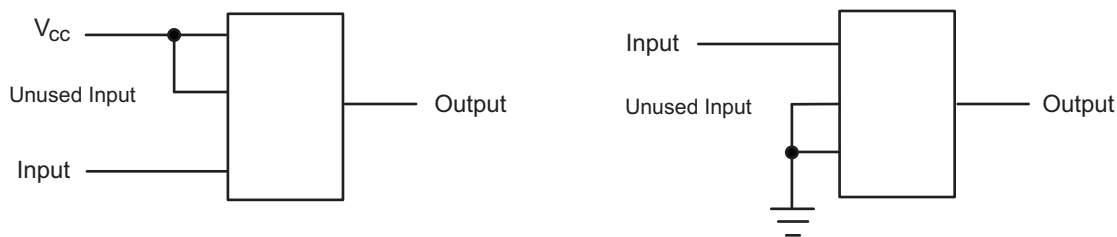


Figure 7. Layout Diagram

13 Device and Documentation Support

13.1 Trademarks

Widebus is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74LVCHR162245ADLG4	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(LVCHR162245A, LVC HR16245A)
74LVCHR16245AGRG4	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVCHR16245A
74LVCHR16245AVRG4	Active	Production	TVSOP (DGV) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LDR245A
74LVCHR16245AVRG4.B	Active	Production	TVSOP (DGV) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LDR245A
SN74LVCHR162245ADL	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(LVCHR162245A, LVC HR16245A)
SN74LVCHR16245AGR	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVCHR16245A
SN74LVCHR16245AGR.B	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVCHR16245A
SN74LVCHR16245ALR	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(LVCHR162245A, LVC HR16245A)
SN74LVCHR16245ALR.B	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(LVCHR162245A, LVC HR16245A)
SN74LVCHR16245AVR	Active	Production	TVSOP (DGV) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LDR245A
SN74LVCHR16245AVR.B	Active	Production	TVSOP (DGV) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LDR245A

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74LVCHR16245AVRG4	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1
SN74LVCHR16245AGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74LVCHR16245ALR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
SN74LVCHR16245AVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

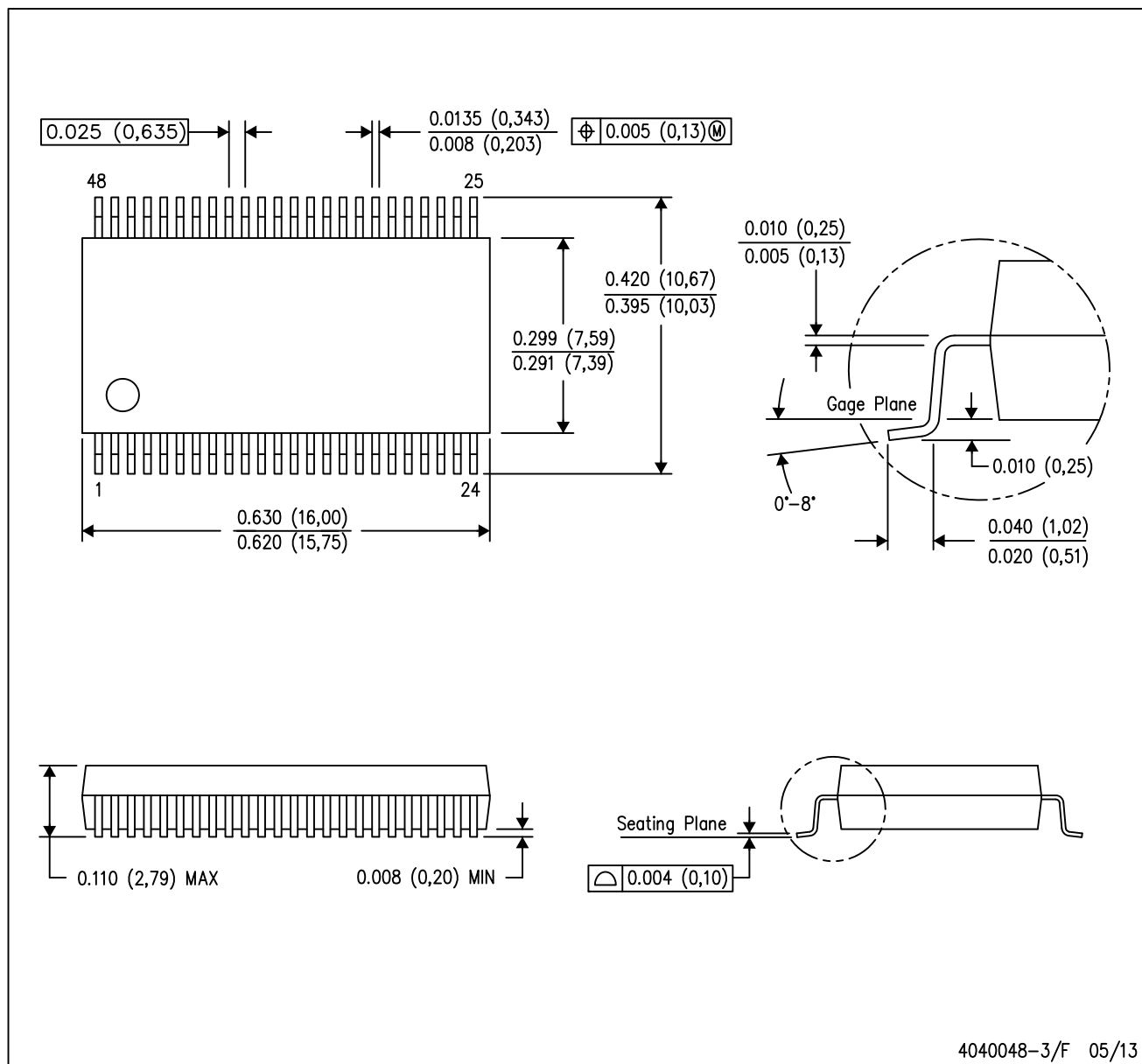


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74LVCHR16245AVRG4	TVSOP	DGV	48	2000	353.0	353.0	32.0
SN74LVCHR16245AGR	TSSOP	DGG	48	2000	356.0	356.0	45.0
SN74LVCHR16245ALR	SSOP	DL	48	1000	356.0	356.0	53.0
SN74LVCHR16245AVR	TVSOP	DGV	48	2000	353.0	353.0	32.0

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE

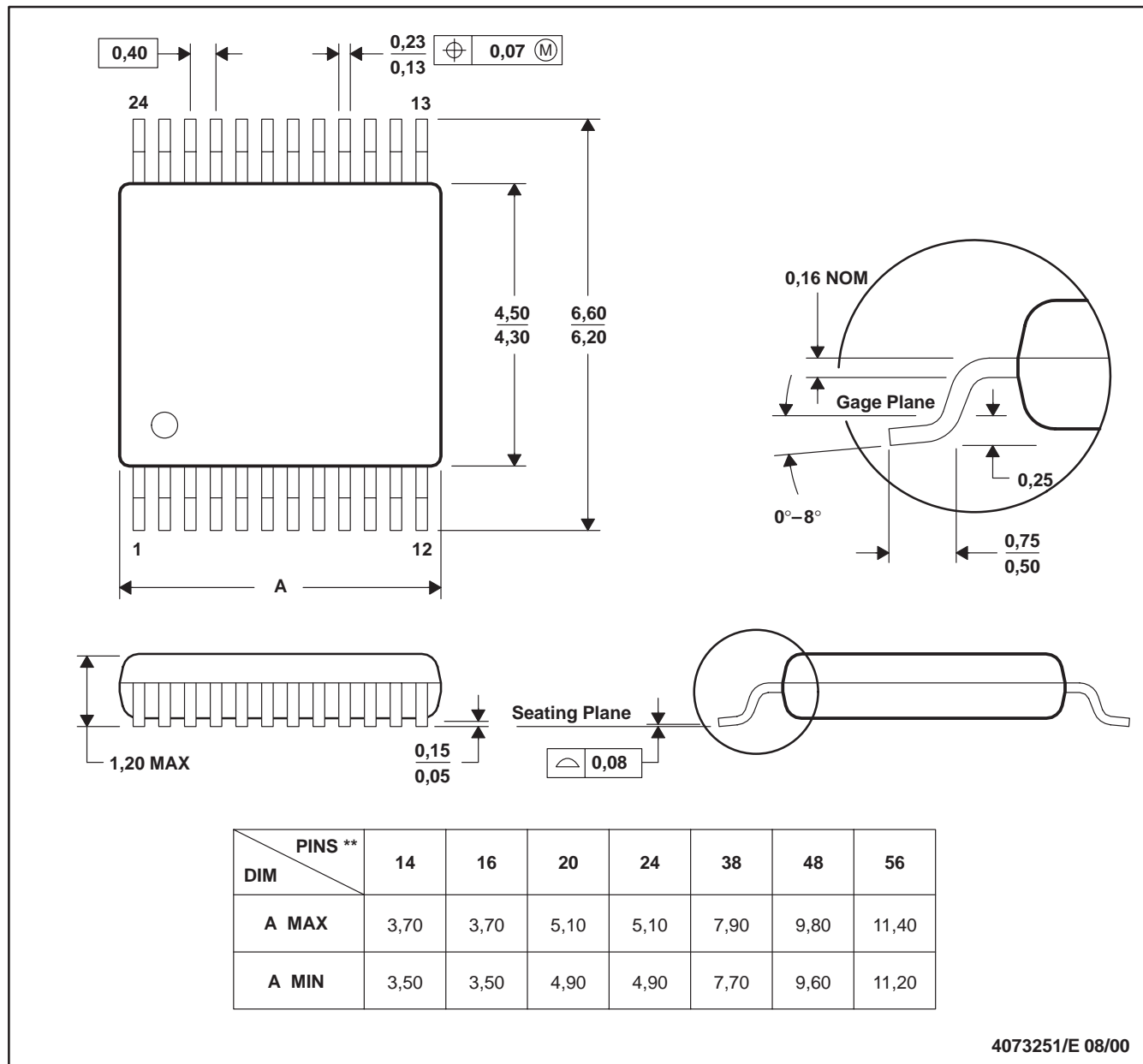


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MO-118

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

EXAMPLE BOARD LAYOUT

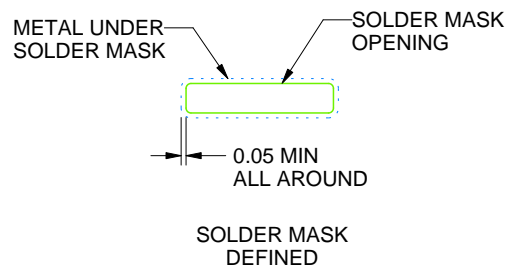
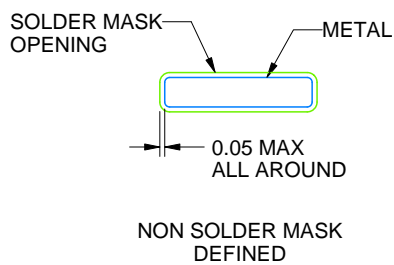
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

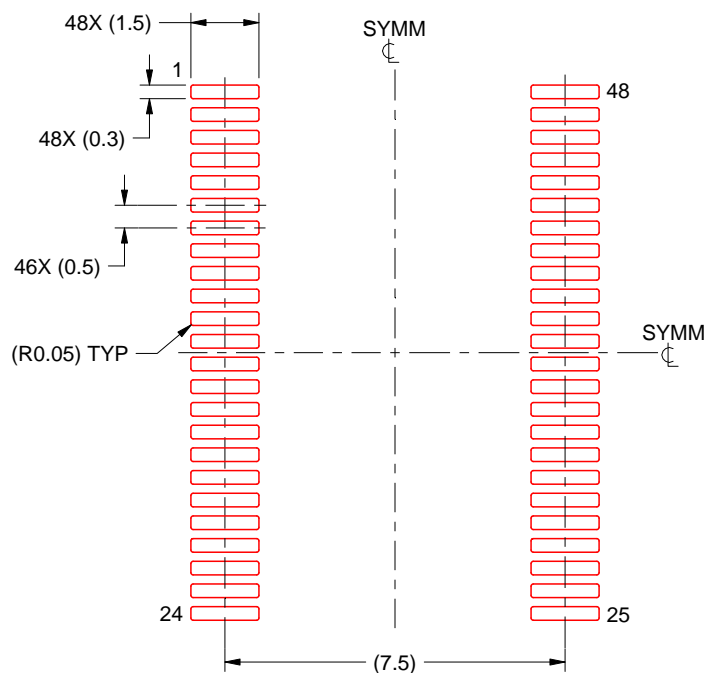
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4214859/B 11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025