

SN74SSTV16859

13-BIT TO 26-BIT REGISTERED BUFFER WITH SSTL_2 INPUTS AND OUTPUTS

SCES297D – FEBRUARY 2000 – REVISED AUGUST 2004

- Member of the Texas Instruments Widebus™ Family
- 1-to-2 Outputs to Support Stacked DDR DIMMs
- Supports SSTL_2 Data Inputs
- Outputs Meet SSTL_2 Class II Specifications
- Differential Clock (CLK and $\overline{\text{CLK}}$) Inputs
- Supports LVCMOS Switching Levels on the $\overline{\text{RESET}}$ Input
- $\overline{\text{RESET}}$ Input Disables Differential Input Receivers, Resets All Registers, and Forces All Outputs Low
- Pinout Optimizes DIMM PCB Layout
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

**DGG PACKAGE
(TOP VIEW)**

Q13A	1	64	V _{DDQ}
Q12A	2	63	GND
Q11A	3	62	D13
Q10A	4	61	D12
Q9A	5	60	V _{CC}
V _{DDQ}	6	59	V _{DDQ}
GND	7	58	GND
Q8A	8	57	D11
Q7A	9	56	D10
Q6A	10	55	D9
Q5A	11	54	GND
Q4A	12	53	D8
Q3A	13	52	D7
Q2A	14	51	$\overline{\text{RESET}}$
GND	15	50	GND
Q1A	16	49	$\overline{\text{CLK}}$
Q13B	17	48	CLK
V _{DDQ}	18	47	V _{DDQ}
Q12B	19	46	V _{CC}
Q11B	20	45	V _{REF}
Q10B	21	44	D6
Q9B	22	43	GND
Q8B	23	42	D5
Q7B	24	41	D4
Q6B	25	40	D3
GND	26	39	GND
V _{DDQ}	27	38	V _{DDQ}
Q5B	28	37	V _{CC}
Q4B	29	36	D2
Q3B	30	35	D1
Q2B	31	34	GND
Q1B	32	33	V _{DDQ}

description/ordering information

This 13-bit to 26-bit registered buffer is designed for 2.3-V to 2.7-V V_{CC} operation.

All inputs are SSTL_2, except the LVCMOS reset ($\overline{\text{RESET}}$) input. All outputs are SSTL_2, Class II compatible.

The SN74SSTV16859 operates from a differential clock (CLK and $\overline{\text{CLK}}$). Data are registered at the crossing of CLK going high and $\overline{\text{CLK}}$ going low.

ORDERING INFORMATION

T _A	PACKAGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	QFN – RGQ (Tin–Pb Finish)	Tape and reel	SN74SSTV16859RGQR
	QFN – RGQ (Matte–Tin Finish)		
	TSSOP – DGG	Tape and reel	SN74SSTV16859DGGR

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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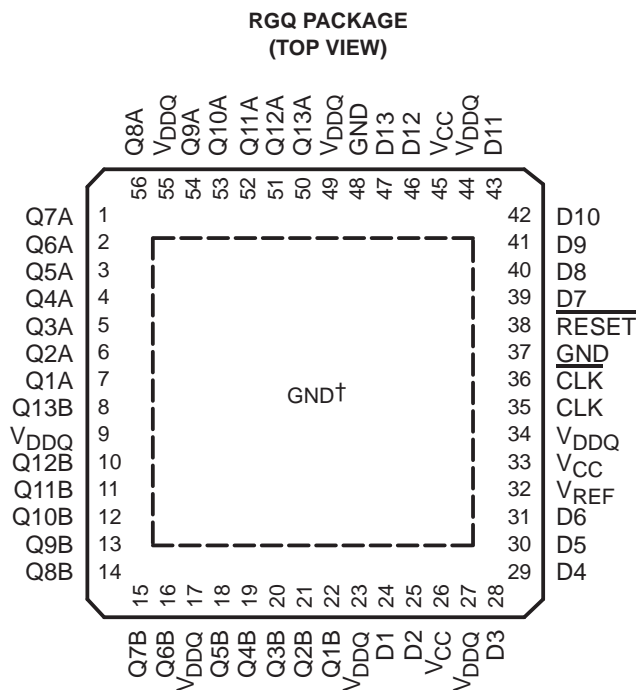
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description/ordering information (continued)

The device supports low-power standby operation. When $\overline{\text{RESET}}$ is low, the differential input receivers are disabled, and undriven (floating) data, clock, and reference voltage (V_{REF}) inputs are allowed. In addition, when $\overline{\text{RESET}}$ is low, all registers are reset, and all outputs are forced low. The LVCMOS $\overline{\text{RESET}}$ input always must be held at a valid logic high or low level.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{\text{RESET}}$ must be held in the low state during power up.



† The center die pad must be connected to GND.

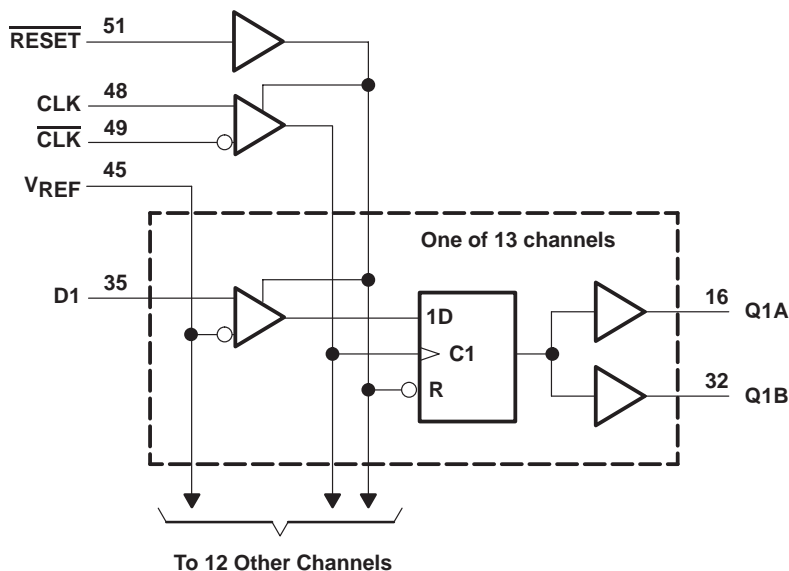
FUNCTION TABLE

INPUTS				OUTPUT
$\overline{\text{RESET}}$	CLK	$\overline{\text{CLK}}$	D	Q
H	↑	↓	H	H
H	↑	↓	L	L
H	L or H	L or H	X	Q_0
L	X or floating	X or floating	X or floating	L

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logic diagram (positive logic)



Pin numbers shown are for the DGG package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} or V_{DDQ}	-0.5 V to 3.6 V
Input voltage range, V_I (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{DDQ} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DDQ}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{DDQ})	± 50 mA
Continuous current through each V_{CC} , V_{DDQ} , or GND	± 100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	55°C/W
(see Note 4): RGQ package	22°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 3.6 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.
 4. The package thermal impedance is calculated in accordance with JESD 51-5.

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recommended operating conditions (see Note 5)

		MIN	NOM	MAX	UNIT	
V _{CC}	Supply voltage	V _{DDQ}		2.7	V	
V _{DDQ}	Output supply voltage	2.3		2.7	V	
V _{REF}	Reference voltage (V _{REF} = V _{DDQ} /2)	1.15	1.25	1.35	V	
V _{TT}	Termination voltage	V _{REF} – 40 mV	V _{REF}	V _{REF} + 40 mV	V	
V _I	Input voltage	0		V _{CC}	V	
V _{IH}	AC high-level input voltage	Data inputs		V _{REF} + 310 mV	V	
V _{IL}	AC low-level input voltage	Data inputs		V _{REF} – 310 mV	V	
V _{IH}	DC high-level input voltage	Data inputs		V _{REF} + 150 mV	V	
V _{IL}	DC low-level input voltage	Data inputs		V _{REF} – 150 mV	V	
V _{IH}	High-level input voltage	RESET		1.7	V	
V _{IL}	Low-level input voltage	RESET		0.7	V	
V _{ICR}	Common-mode input voltage range	CLK, CLK		0.97	1.53	V
V _{I(PP)}	Peak-to-peak input voltage	CLK, CLK		360	mV	
I _{OH}	High-level output current			–20	mA	
I _{OL}	Low-level output current			20		
T _A	Operating free-air temperature	0		70	°C	

NOTE 5: The RESET input of the device must be held at valid logic voltage levels (not floating) to ensure proper device operation. The differential inputs must not be floating unless RESET is low. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC} †	MIN	TYP‡	MAX	UNIT
V _{IK}		I _I = –18 mA	2.3 V			–1.2	V
V _{OH}		I _{OH} = –100 μA	2.3 V to 2.7 V	V _{DDQ} – 0.2			V
		I _{OH} = –16 mA	2.3 V	1.95			
V _{OL}		I _{OL} = 100 μA	2.3 V to 2.7 V			0.2	V
		I _{OL} = 16 mA	2.3 V			0.35	
I _I	All inputs	V _I = V _{CC} or GND	2.7 V			±5	μA
I _{CC}	Static standby	RESET = GND	2.7 V			10	μA
	Static operating	RESET = V _{CC} , V _I = V _{IH(AC)} or V _{IL(AC)}				40	
I _{CCD}	Dynamic operating – clock only	RESET = V _{CC} , V _I = V _{IH(AC)} or V _{IL(AC)} , CLK and CLK switching 50% duty cycle	2.5 V			30	μA/ MHz
	Dynamic operating – per each data input	RESET = V _{CC} , V _I = V _{IH(AC)} or V _{IL(AC)} , CLK and CLK switching 50% duty cycle, One data input switching at one-half clock frequency, 50% duty cycle				10	
r _{OH}	Output high	I _{OH} = –20 mA	2.3 V to 2.7 V	7		20	Ω
r _{OL}	Output low	I _{OL} = 20 mA	2.3 V to 2.7 V	7		20	Ω
r _{O(Δ)}	r _{OH} – r _{OL}	I _O = 20 mA, T _A = 25°C, One output	2.5 V			6	Ω
C _i §	Data inputs	V _I = V _{REF} ± 310 mV	2.5 V	2.5	3	3.5	pF
	CLK, CLK	V _{ICR} = 1.25 V, V _{I(PP)} = 360 mV		2.5	3	3.5	
	RESET	V _I = V _{CC} or GND		3			

† For this test condition, V_{DDQ} always is equal to V_{CC}.

‡ All typical values are at V_{CC} = 2.5 V, T_A = 25°C.

§ Measured with 50-MHz input frequency for the QFN package and 10-MHz input frequency for the TSSOP package



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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}^\dagger$		UNIT
		MIN	MAX	
f_{clock}	Clock frequency	200		MHz
t_w	Pulse duration, CLK, $\overline{\text{CLK}}$ high or low	2.5		ns
t_{act}	Differential inputs active time (see Note 6)	22		ns
t_{inact}	Differential inputs inactive time (see Note 7)	22		ns
t_{su}	Setup time, fast slew rate (see Notes 8 and 10)	0.75		ns
	Setup time, slow slew rate (see Notes 9 and 10)	0.9		
t_h	Hold time, fast slew rate (see Notes 8 and 10)	0.75		ns
	Hold time, slow slew rate (see Notes 9 and 10)	0.9		

[†] For this test condition, V_{DDQ} always is equal to V_{CC} .

- NOTES: 6. V_{REF} must be held at a valid input level, and data inputs must be held low for a minimum time of t_{act} max, after $\overline{\text{RESET}}$ is taken high.
7. V_{REF} , data, and clock inputs must be held at valid voltage levels (not floating) for a minimum time of t_{inact} max, after $\overline{\text{RESET}}$ is taken low.
8. For data signal input slew rate $\geq 1\text{ V/ns}$
9. For data signal input slew rate $\geq 0.5\text{ V/ns}$ and $< 1\text{ V/ns}$
10. CLK, $\overline{\text{CLK}}$ signals input slew rates are $\geq 1\text{ V/ns}$.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

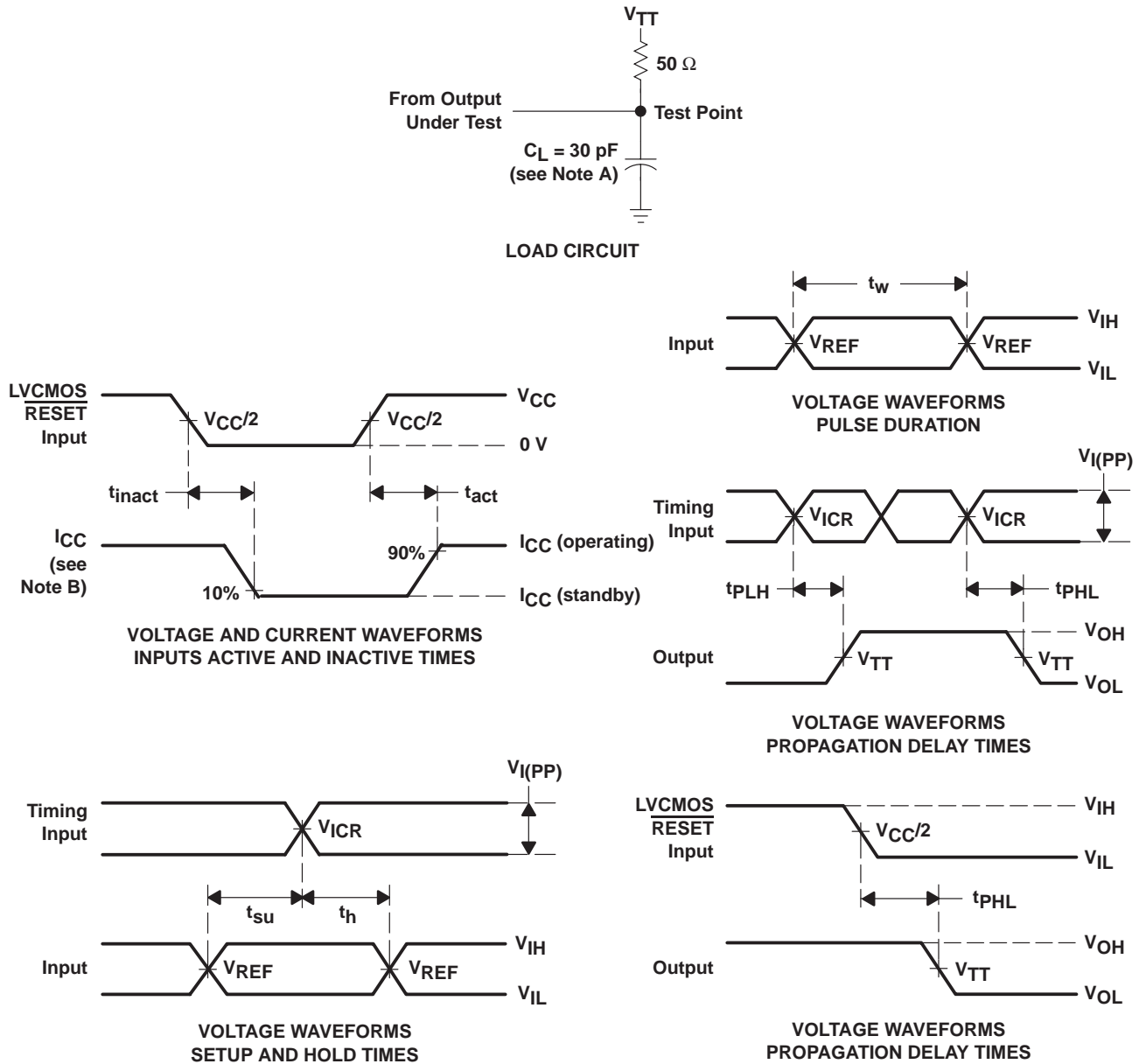
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}^\dagger$		UNIT
			MIN	MAX	
f_{max}			200		MHz
t_{pd}	CLK and $\overline{\text{CLK}}$	Q	1.1	2.8	ns
t_{PHL}	$\overline{\text{RESET}}$	Q	5		ns

[†] For this test condition, V_{DDQ} always is equal to V_{CC} .

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. I_{CC} tested with clock and data inputs held at V_{CC} or GND, and I_O = 0 mA.
 - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, input slew rate = 1 V/ns ±20% (unless otherwise noted).
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. V_{TT} = V_{REF} = V_{DDQ}/2
 - F. V_{IH} = V_{REF} + 310 mV (ac voltage levels) for differential inputs. V_{IH} = V_{CC} for LVC MOS input.
 - G. V_{IL} = V_{REF} - 310 mV (ac voltage levels) for differential inputs. V_{IL} = GND for LVC MOS input.
 - H. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74SSTV16859DGGRG4	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	0 to 70	SSTV16859	
HPA00022DGGR	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	0 to 70	SSTV16859	
SN74SSTV16859DGGR	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	0 to 70	SSTV16859	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74SSTV16859DGGR	TSSOP	DGG	64	2000	330.0	24.4	8.4	17.3	1.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74SSTV16859DGGR	TSSOP	DGG	64	2000	367.0	367.0	45.0

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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