1 Features
- Design to protect submicron 3-V or 5-V circuits from noise transients
- Port ESD protection capability exceeds:
  - 15-kV human body model
  - 2-kV machine model
- Available in a WCSP chip-scale package
- Stand-off voltage: 6 V (minimum)
- Low current leakage: 1-µA maximum at 6 V
- Low capacitance: 35-pF (typical)

2 Applications
- USB full-speed host, HUB, or peripheral
- Ports

3 Description
The SN65220 device is a dual, and the SN65240 and SN75240 devices are quadruple, unidirectional transient voltage suppressors (TVS). These devices provide electrical noise transient protection to Universal Serial Bus (USB) low and full-speed ports. The input capacitance of 35 pF makes it unsuitable for high-speed USB 2.0 applications.

Any cabled I/O can be subjected to electrical noise transients from various sources. These noise transients can cause damage to the USB transceiver or the USB ASIC if they are of sufficient magnitude and duration.

The SN65220, SN65240, and SN75240 devices ESD performance is measured at the system level, according to IEC61000-4-2; system design, however, impacts the results of these tests. To accomplish a high compliance level, careful board design and layout techniques are required.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN65220</td>
<td>SOT-23</td>
<td>2.90 mm × 1.60 mm</td>
</tr>
<tr>
<td></td>
<td>DSBGA (4)</td>
<td>0.925 mm × 0.925 mm</td>
</tr>
<tr>
<td>SN65240</td>
<td>PDIP (8)</td>
<td>9.09 mm × 6.35 mm</td>
</tr>
<tr>
<td>SN75240</td>
<td>TSSOP (8)</td>
<td>3.00 mm × 4.40 mm</td>
</tr>
</tbody>
</table>

(1) See the orderable addendum at the end of the data sheet for all available packages.
Table of Contents

1 Features.................................................................1
2 Applications.........................................................1
3 Description.........................................................1
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4 Revision History
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (April 2021) to Revision J (August 2022) Page
• Updated the SN65220, SN65240, and SN75240 suppressors in the Device Comparison table..........................3

Changes from Revision H (May 2015) to Revision I (April 2021) Page
• Updated the numbering format for tables, figures and cross-references throughout the document ..................1
• Updated the units for resistance from O to Ω in the Simplified Schematic figure........................................1
• Updated the units from O to Ω in the Typical Application Schematic for ESD Protection of USB Transceivers figure .................................................................8
• Updated the units from O to Ω in the Layout Example of a 4-Layer Board With SN65220 figure.....................10

Changes from Revision G (August 2008) to Revision H (May 2015) Page
• Added Pin Configuration and Functions section, ESD table, Thermal Information table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section ..........1
## 5 Device Comparison Table

<table>
<thead>
<tr>
<th>PRODUCT</th>
<th>SUPPRESSORS</th>
<th>$T_A$ - RANGE</th>
<th>PACKAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN65220</td>
<td>2</td>
<td>−40°C to 85°C</td>
<td>WCSP-4</td>
</tr>
<tr>
<td>SN65240</td>
<td>4</td>
<td>−40°C to 85°C</td>
<td>DIP-8</td>
</tr>
<tr>
<td>SN75240</td>
<td>4</td>
<td>0°C to 70°C</td>
<td>TSSOP-8</td>
</tr>
</tbody>
</table>

## 6 Pin Configuration and Functions

![DBV Package, 6-Pin SOT-23](image)

![P, PW Package, 8-Pin PDIP, TSSOP](image)

### Table 6-1. Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>6</td>
<td>Analog input</td>
</tr>
<tr>
<td>B</td>
<td>4</td>
<td>Analog input</td>
</tr>
<tr>
<td>C</td>
<td>2</td>
<td>Analog input</td>
</tr>
<tr>
<td>D</td>
<td>4</td>
<td>Analog input</td>
</tr>
<tr>
<td>GND</td>
<td>2, 5</td>
<td>Power</td>
</tr>
<tr>
<td>NC</td>
<td>1, 3</td>
<td>Internally not connected</td>
</tr>
</tbody>
</table>

![YZB Package, 4-Pin DSBGA](image)

### Table 6-2. Pin Functions

<table>
<thead>
<tr>
<th>NO.</th>
<th>NAME</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>A</td>
<td>Analog input</td>
<td>Transient suppressor input – Line 1</td>
</tr>
<tr>
<td>B1</td>
<td>B</td>
<td>Analog input</td>
<td>Transient suppressor input – Line 2</td>
</tr>
<tr>
<td>A2, B2</td>
<td>GND</td>
<td>Power</td>
<td>Local device ground</td>
</tr>
</tbody>
</table>
# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(P_{\text{D(peak)}})</td>
<td>60</td>
<td>W</td>
<td></td>
</tr>
<tr>
<td>(I_{\text{FSM}})</td>
<td>3</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>(I_{\text{RSM}})</td>
<td>–9</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>(T_{\text{stg}})</td>
<td>–65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Section 7.3 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 7.2 ESD Ratings

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{\text{ESD}})</td>
<td>±15000</td>
<td>V</td>
</tr>
<tr>
<td>(V_{\text{ESD}})</td>
<td>±2000</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(T_{\text{A}})</td>
<td>0</td>
<td>70</td>
<td>°C</td>
</tr>
<tr>
<td>(T_{\text{A}})</td>
<td>–40</td>
<td>85</td>
<td>°C</td>
</tr>
</tbody>
</table>

## 7.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1)})</th>
<th>SN65220 (SOT-23)</th>
<th>SN65240, SN75240 (DSBGA)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(R_{\text{JA}})</td>
<td>199.5</td>
<td>70</td>
<td>°C/W</td>
</tr>
<tr>
<td>(R_{\text{JC(top)}})</td>
<td>159.7</td>
<td>1.8</td>
<td>°C/W</td>
</tr>
<tr>
<td>(R_{\text{JB}})</td>
<td>51.1</td>
<td>43.5</td>
<td>°C/W</td>
</tr>
<tr>
<td>(\psi_{\text{JT}})</td>
<td>41</td>
<td>9.2</td>
<td>°C/W</td>
</tr>
<tr>
<td>(\psi_{\text{JB}})</td>
<td>50.5</td>
<td>43.5</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 7.5 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(I_{\text{kg}})</td>
<td>(V_i = 6) V at A, B, C, or D terminals</td>
<td>1</td>
<td></td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>(V_{\text{(BR)}})</td>
<td>(V_i = 1) mA at A, B, C, or D terminals</td>
<td>6.5</td>
<td>7</td>
<td>8</td>
<td>V</td>
</tr>
<tr>
<td>(C_{\text{IN}})</td>
<td>(V_i = 0.4) sin (4E6πt) + 0.5 V</td>
<td>35</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
</tbody>
</table>
7.6 Typical Characteristics

$T_A = 25^\circ C$ unless otherwise noted.

![Figure 7-1. Transient-Voltage-Suppressor Current vs Voltage](image)

8 Parameter Measurement Information

![Figure 8-1. Measurement of Leakage Current](image)

![Figure 8-2. Measurement of Breakdown Voltage](image)
9 Detailed Description

9.1 Overview

The SN65220, SN65240, and SN75240 devices integrate multiple unidirectional transient voltage suppressors (TVS). **Figure 9-1** shows the equivalent circuit diagram of a single TVS diode.

For positive transient voltages, only the Q1 transistor determines the switching characteristic. When the input voltage reaches the Zener voltage, $V_Z$, Zener diode D1 conducts; therefore, allowing for the base-emitter voltage, $V_{BE}$, to increase. At $V_{IN} = V_Z + V_{BE}$, the transistor starts conducting. From then on, its on-resistance decreases linearly with increasing input voltage.

For negative transient voltages, only diode D2 determines the switching characteristic. Here, switching occurs when the input voltage exceeds the diode forward voltage, $V_{FW}$.

![Figure 9-1. TVS Structure and Current — Voltage Characteristic](image)

9.2 Functional Block Diagram

![Functional Block Diagram](image)
9.3 Feature Description
The SN65220, SN65240, and SN75240 family of unidirectional transient voltage suppressors provide transient protection to Universal Serial Bus low and full-speed ports. These TVS diodes provide a minimum breakdown voltage of 6.5-V to protect USB transceivers and USB ASICs typically implemented in 3-V or 5-V digital CMOS technology.

9.4 Device Functional Modes
TVS diodes possess two functional modes, a high-impedance and a conducting mode.

During normal operating conditions, that is in the absence of high voltage transients, the breakdown voltage of TVS diodes is not exceeded and the devices remain high-impedance.

In the presence of high-voltage transients the breakdown voltage is exceeded. The TVS diodes then conduct and become low-impedance. In this mode excessive transient energy is shunted directly to local circuit ground, preventing USB transceivers from electrical damage.
10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The USB has become a popular solution to connect PC peripherals. The USB allows devices to be hot-plugged in and out of the existing PC system without rebooting or turning off the PC. Because frequent human interaction with the USB system occurs as a result of its attractive hot-plugging ability, there is the possibility for large ESD strikes and damage to crucial system elements. The ESD protection included on the existing hardware is typically in the 2-kV to 4-kV range for the human body model (HBD) and 200-V to 300-V for the machine model (MM). The ESD voltage levels found in a normal USB operating environment can exceed these levels. The SN75240, SN65240, and SN65220 devices will increase the robustness of the existing USB hardware to ESD strikes common to the environment in which USB is likely to be used.

10.2 Typical Application

Figure 10-1 shows a typical USB system and application of the SN75240, SN65240, and SN65220 devices. Connections to pin A from the D+ data line, pin B from the D– data line, and the device grounds from the GND line that already exists are necessary to increase the amount of ESD protection provided to the USB port.

The design of the suppressor gives it very low maximum current leakage of 1 μA, a very low typical capacitance of 35 pF, and a standoff voltage minimum of 6 V. Because of these levels, the SN75240, SN65240, and SN65220 devices will provide added protection to the USB system hardware during ESD events without introducing the high capacitance and current leakage levels typical of external transient voltage suppressors. The addition of an SN75240, SN65240, or SN65220 device is beneficial to both full-speed and low-speed USB 1.1 bandwidth standards.

Figure 10-1. Typical Application Schematic for ESD Protection of USB Transceivers
10.2.1 Design Requirements

For this design example, use the parameters listed in Table 10-1 as design parameters.

<table>
<thead>
<tr>
<th>DESIGN PARAMETER</th>
<th>EXAMPLE VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum breakdown voltage (TVS)</td>
<td>6.5 V</td>
</tr>
<tr>
<td>Maximum supply voltage (USB transceiver)</td>
<td>5.5 V</td>
</tr>
<tr>
<td>Typical junction capacitance (TVS)</td>
<td>35 pF</td>
</tr>
<tr>
<td>Maximum data rate (USB transceiver)</td>
<td>12 Mbps</td>
</tr>
</tbody>
</table>

10.2.2 Detailed Design Procedure

To effectively protect USB transceivers, use TVS diodes with breakdown voltages close to 6 V, such as the SN65220, SN65240, or SN75220 devices.

Because of the TVS junction capacitance of 35 pF, apply these TVS diodes only to USB transceivers with full-speed capability that is 12 Mbps maximum.

Place the TVS diodes as close to the board connector as possible to prevent transient energies from entering further board space.

Connect the TVS diode between the data lines (D+, D–) and local circuit ground (GND).

Because noise transient represents high-speed frequencies, ensure low-inductance return paths for the transient currents by providing a solid ground plane and using two VIAs connecting the TVS terminals to ground.

10.2.3 Application Curve

![Figure 10-2. HBM Curve](image-url)
11 Power Supply Recommendations

Unlike other semiconductor components that require a supply voltage to operate, the SN65220, SN65240, and SN75240 transient suppressors are combinations of multiple p-n diodes, activated by transient voltages. Therefore, these transient suppressors do not require external voltage supplies.

12 Layout

12.1 Layout Guidelines

The multiple ground pins provided lower the connection resistance to ground. In order to improve circuit operation, a connection to all ground pins must be provided on the system printed circuit board. Without proper device connection to ground, the speed and protection capability of the device will be degraded.

- The ground termination pads should be connected directly to a ground plane on the board for optimum performance. A single trace ground conductor will not provide an effective path for fast rise-time transient events including ESD due to parasitic inductance.
- Nominal inductive values of a PCB trace are approximately 20 nH/cm. This value may seem small, but an apparent short length of trace may be sufficient to produce significant L(di/dt) effects with fast rise-time ESD spikes.
- Mount the TVS as close as possible to the I/O socket to reduce radiation originating from the transient as it is routed to ground.

Note

Direct connective paths of the traces are taken to the suppressor mounting pads to minimize parasitic inductance in the surge-current conductive path, thus minimizing L(di/dt) effects.

12.2 Layout Example

![Figure 12-1. Layout Example of a 4-Layer Board With SN65220](image-url)
13 Device and Documentation Support

13.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on Subscribe to updates to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.2 Support Resources

TI E2E™ support forums are an engineer’s go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided “AS IS” by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

13.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.5 Glossary

TI Glossary  This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead finish/Ball material</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN65220DBVR</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>DBV</td>
<td>6</td>
<td>3000</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>SADI</td>
<td>Samples</td>
</tr>
<tr>
<td>SN65220DBVRG4</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>DBV</td>
<td>6</td>
<td>3000</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>SADI</td>
<td>Samples</td>
</tr>
<tr>
<td>SN65220DBVT</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>DBV</td>
<td>6</td>
<td>250</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>SADI</td>
<td>Samples</td>
</tr>
<tr>
<td>SN65220DBVTG4</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>DBV</td>
<td>6</td>
<td>250</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>SADI</td>
<td>Samples</td>
</tr>
<tr>
<td>SN65240P</td>
<td>ACTIVE</td>
<td>PDIP</td>
<td>P</td>
<td>8</td>
<td>50</td>
<td>RoHS &amp; Green</td>
<td>N / A for Pkg Type</td>
<td>-40 to 85</td>
<td></td>
<td>SN65240P</td>
<td>Samples</td>
</tr>
<tr>
<td>SN65240PW</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>PW</td>
<td>8</td>
<td>150</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>A65240</td>
<td>Samples</td>
</tr>
<tr>
<td>SN65240PG</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>PW</td>
<td>8</td>
<td>150</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>A65240</td>
<td>Samples</td>
</tr>
<tr>
<td>SN75240P</td>
<td>ACTIVE</td>
<td>PDIP</td>
<td>P</td>
<td>8</td>
<td>50</td>
<td>RoHS &amp; Green</td>
<td>N / A for Pkg Type</td>
<td>0 to 70</td>
<td></td>
<td>SN75240P</td>
<td>Samples</td>
</tr>
<tr>
<td>SN75240PW</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>PW</td>
<td>8</td>
<td>150</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>A75240</td>
<td>Samples</td>
</tr>
<tr>
<td>SN75240PG</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>PW</td>
<td>8</td>
<td>150</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>A75240</td>
<td>Samples</td>
</tr>
<tr>
<td>SN75240PWR</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>PW</td>
<td>8</td>
<td>2000</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>A75240</td>
<td>Samples</td>
</tr>
<tr>
<td>SN75240PWRG4</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>PW</td>
<td>8</td>
<td>2000</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>A75240</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
- **RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
- **Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JIS7098 low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN65220:

- Automotive: SN65220-Q1

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
### TAPE AND REEL INFORMATION

#### TAPE DIMENSIONS

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

#### REEL DIMENSIONS

- **Reel Diameter**: Dimensions designed to accommodate the component width
- **Reel Width (W1)**: Dimension designed to accommodate the component thickness
- **A0**: Overall width of the carrier tape
- **B0**: Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

**Pocket Quadrants**
- Q1
- Q2
- Q3
- Q4

**Sprocket Holes**

**User Direction of Feed**

*All dimensions are nominal*

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<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
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### TAPE AND REEL BOX DIMENSIONS

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*All dimensions are nominal*
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<td>10.2</td>
<td>3600</td>
<td>3.5</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
NOTES:

A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 variation BA.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.
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