SN75468, SN75469

1 Features
• 500-mA Rated Collector Current (Single Output)
• High-Voltage Output 100 V
• Output Clamp Diodes
• Inputs Compatible With Various Types of Logic
• Relay Driver Applications
• Higher-Voltage Versions of ULN2003A and ULN2004A, for Commercial Temperature range

2 Applications
• Relay Drivers
• Hammer Drivers
• Lamp Drivers
• Display Drivers (LED and Gas Discharge)
• Line Drivers
• Logic Buffers

3 Description
The SN75468 and SN75469 are high-voltage, high-current Darlington transistor arrays. Each consists of seven NPN Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of each Darlington pair is 500 mA. The Darlington pairs may be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers.

The SN75468 has a 2700-Ω series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS. The SN75469 has a 10.5-kΩ series base resistor to allow its operation directly with CMOS or PMOS that use supply voltages of 6 to 15 V. The required input current is below that of the SN75468.

4 Simplified Schematic

Device Information(1)

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE (PIN)</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN7546x</td>
<td>D (16)</td>
<td>9.90 mm × 3.91 mm</td>
</tr>
<tr>
<td></td>
<td>N (16)</td>
<td>19.30 mm × 6.35 mm</td>
</tr>
<tr>
<td></td>
<td>NS (16)</td>
<td>10.30 mm × 5.30 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the datasheet.
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5 Revision History

Changes from Revision D (November 2004) to Revision E Page

• Added Applications, Device Information table, Pin Functions table, ESD Ratings table, Thermal Information table, Typical Characteristics, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section ................................................................. 1

• Deleted Ordering Information table ................................................................. 1
# Pin Configuration and Functions

![Pin Configuration Diagram](image)

## Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>B &lt;1:7&gt;</td>
<td>I</td>
<td>Channel 1 through 7 darlington base input</td>
</tr>
<tr>
<td>C &lt;1:7&gt;</td>
<td>O</td>
<td>Channel 1 through 7 darlington collector output</td>
</tr>
<tr>
<td>E</td>
<td>—</td>
<td>Common Emmitter shared by all channels (typically tied to ground)</td>
</tr>
<tr>
<td>COM</td>
<td>I/O</td>
<td>Common cathode node for flyback diodes (required for inductive loads)</td>
</tr>
</tbody>
</table>
7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{CE})</td>
<td>100</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(V_i)</td>
<td>30</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(I_{OK})</td>
<td>500</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>(I_{OK})</td>
<td>500</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>(I_{VEC})</td>
<td>–2.5</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>(T_J)</td>
<td>150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>(T_{stg})</td>
<td>–65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to the emitter/substrate terminal E, unless otherwise noted.

7.2 ESD Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{(ESD)})</td>
<td>±2000</td>
<td>V</td>
</tr>
<tr>
<td>(V_{CDM})</td>
<td>±500</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_i)</td>
<td>0</td>
<td>5</td>
<td>V</td>
</tr>
<tr>
<td>(V_{DC})</td>
<td>0</td>
<td>100</td>
<td>V</td>
</tr>
<tr>
<td>(T_J)</td>
<td>–40</td>
<td>125</td>
<td>°C</td>
</tr>
</tbody>
</table>

7.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1)})</th>
<th>SN7546x</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(R_{JA})</td>
<td>73</td>
<td>°C/W</td>
</tr>
<tr>
<td>(R_{JC(top)})</td>
<td>40.3</td>
<td></td>
</tr>
<tr>
<td>(R_{JB})</td>
<td>38.9</td>
<td></td>
</tr>
<tr>
<td>(\Psi_{JT})</td>
<td>10.9</td>
<td></td>
</tr>
<tr>
<td>(\Psi_{JB})</td>
<td>38.7</td>
<td></td>
</tr>
<tr>
<td>(R_{JC(bot)})</td>
<td>N/A</td>
<td></td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPR953.
# 7.5 Electrical Characteristics

$T_A = 25^\circ C$ (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS (1)</th>
<th>SN75468</th>
<th>SN75469</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{I(oh)}$ On-state input voltage</td>
<td>$V_{CE} = 2 , V$</td>
<td>$I_C = 125 , mA$</td>
<td>$I_C = 200 , mA$</td>
<td>$I_C = 250 , mA$</td>
</tr>
<tr>
<td>$V_{CE(max)}$ Collector-emitter saturation voltage</td>
<td>$I_I = 250 , \mu A$, $I_C = 100 , mA$</td>
<td>$0.9$</td>
<td>$1.1$</td>
<td>$0.9$</td>
</tr>
<tr>
<td></td>
<td>$I_I = 350 , \mu A$, $I_C = 100 , mA$</td>
<td>$1$</td>
<td>$1.3$</td>
<td>$1$</td>
</tr>
<tr>
<td></td>
<td>$I_I = 500 , \mu A$, $I_C = 100 , mA$</td>
<td>$1.2$</td>
<td>$1.6$</td>
<td>$1.2$</td>
</tr>
<tr>
<td>$V_F$ Clamp-diode forward voltage</td>
<td>$I_I = 350 , mA$</td>
<td>$1.7$</td>
<td>$2$</td>
<td>$1.7$</td>
</tr>
<tr>
<td>$I_{CEX}$ collector cutoff current</td>
<td>$V_{CE} = 100 , V$, $I_I = 0$</td>
<td>$50$</td>
<td>$50$</td>
<td>$\mu A$</td>
</tr>
<tr>
<td></td>
<td>$V_{CE} = 100 , V$, $T_A = 70^\circ C$</td>
<td>$I_I = 0$</td>
<td>$100$</td>
<td>$100$</td>
</tr>
<tr>
<td></td>
<td>$V_I = 1 , V$</td>
<td></td>
<td></td>
<td>$500$</td>
</tr>
<tr>
<td>$I_{I(off)}$ Off-state input current</td>
<td>$V_{CE} = 50 , V$, $I_C = 500 , \mu A$, $T_A = 70^\circ C$</td>
<td>$50$</td>
<td>$65$</td>
<td>$50$</td>
</tr>
<tr>
<td>$I_I$ Input current</td>
<td>$V_I = 3.85 , V$</td>
<td>$0.93$</td>
<td>$1.35$</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_I = 5 , V$</td>
<td></td>
<td></td>
<td>$0.35$</td>
</tr>
<tr>
<td></td>
<td>$V_I = 12 , V$</td>
<td></td>
<td></td>
<td>$1$</td>
</tr>
<tr>
<td>$I_R$ Clamp-diode reverse current</td>
<td>$V_R = 100 , V$</td>
<td>$50$</td>
<td>$50$</td>
<td>$\mu A$</td>
</tr>
<tr>
<td></td>
<td>$V_R = 100 , V$, $T_A = 70^\circ C$</td>
<td></td>
<td></td>
<td>$100$</td>
</tr>
<tr>
<td>$C_I$ Input Capacitance</td>
<td>$V_I = 0$, $f = 1 , MHz$</td>
<td>$15$</td>
<td>$25$</td>
<td>$15$</td>
</tr>
</tbody>
</table>

(1) All electrical characteristics are measured with $0.1-\mu F$ capacitors connected at REF, CT, and $V_{CC}$ to GND.

# 7.6 Switching Characteristics

$T_A = 25^\circ C$ free-air temperature

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS (1)</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{PLH}$ Propagation delay time, low-to-high-level output</td>
<td>$V_S = 20 , V$, $R_L = 163 , \Omega$, $C_L = 15 , pF$, See Figure 14</td>
<td>$0.25$</td>
<td>$1$</td>
<td>$\mu s$</td>
<td></td>
</tr>
<tr>
<td>$t_{PHL}$ Propagation delay time, high-to-low-level output</td>
<td></td>
<td>$0.25$</td>
<td>$1$</td>
<td>$\mu s$</td>
<td></td>
</tr>
<tr>
<td>$V_{OH}$ High-level output voltage after switching</td>
<td>$V_S = 50 , V$, $I_O = 300 , mA$, See Figure 14</td>
<td>$V_B = 20$</td>
<td></td>
<td>mV</td>
<td></td>
</tr>
</tbody>
</table>

(1) All switching characteristics are measured with $0.1-\mu F$ capacitors connected at REF and $V_{CC}$ to GND.
7.7 Typical Characteristics

Figure 1. Collector-Emitter Saturation Voltage vs Collector Current (One Darlington)

Figure 2. Collector-Emitter Saturation Voltage vs Total Collector Current (Two Darlingtons in Parallel)

Figure 3. Output Current vs Input Current

Figure 4. D Package Maximum Collector Current vs Duty Cycle

Figure 5. N Package Maximum Collector Current vs Duty Cycle
8 Parameter Measurement Information

Figure 6. $I_{CEX}$

Figure 7. $I_{CES}$

Figure 8. $I_{(off)}$

Figure 9. $I_I$

Figure 10. $V_{(on)}$

Figure 11. $h_{FE}$, $V_{CE(sat)}$

Figure 12. $I_R$

Figure 13. $V_F$
Parameter Measurement Information (continued)

A. The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_O = 50 \, \Omega$.
B. CL includes probe and jig capacitance.
C. For testing the '468, $V_{IH} = 3 \, V$; for the '469, $V_{IH} = 8 \, V$.

Figure 14. Test Circuit and Voltage Waveforms

A. The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_O = 50 \, \Omega$.
B. CL includes probe and jig capacitance.
C. For testing the '468, $V_{IH} = 3 \, V$; for the '469, $V_{IH} = 8 \, V$.

Figure 15. Latch-Up Test Circuit and Voltage Waveforms
9 Detailed Description

9.1 Overview

This standard device has proven ubiquity and versatility across a wide range of applications. This is due to its integration of 7 Darlington transistors that are capable of sinking up to 500 mA and wide GPIO range capability.

The SN75468 comprises seven high voltage, high current NPN Darlington transistor pairs. All units feature a common emitter and open collector outputs. To maximize their effectiveness, these units contain suppression diodes for inductive loads. The SN75468 has a series base resistor to each Darlington pair, thus allowing operation directly with TTL or CMOS operating at supply voltages of 5.0 V or 3.3 V. The SN75468 offers solutions to a great many interface needs, including solenoids, relays, lamps, small motors, and LEDs. Applications requiring sink currents beyond the capability of a single output may be accommodated by paralleling the outputs.

This device can operate over a wide temperature range (–40°C to 105°C).

9.2 Functional Block Diagram

![Functional Block Diagram](image)

9.3 Feature Description

Each channel of SN75468 consists of Darlington connected NPN transistors. This connection creates the effect of a single transistor with a very high current gain ($\beta_2$). This can be as high as 10,000 A/A at certain currents. The very high $\beta$ allows for high output current drive with a very low input current, essentially equating to operation with low GPIO voltages.

The GPIO voltage is converted to base current via the 2.7 kΩ resistor connected between the input and base of the pre-driver Darlington NPN. The 7.2 kΩ & 3.0 kΩ resistors connected between the base and emitter of each respective NPN act as pull-downs and suppress the amount of leakage that may occur from the input.

The diodes connected between the output and COM pin is used to suppress the kick-back voltage from an inductive load that is excited when the NPN drivers are turned off (stop sinking) and the stored energy in the coils causes a reverse current to flow into the coil supply via the kick-back diode.

In normal operation the diodes on base and collector pins to emitter will be reversed biased. If these diode are forward biased, internal parasitic NPN transistors will draw (a nearly equal) current from other (nearby) device pins.

9.4 Device Functional Modes

9.4.1 Inductive Load Drive

When the COM pin is tied to the coil supply voltage, SN75468 is able to drive inductive loads and suppress the kick-back voltage via the internal free wheeling diodes.

9.4.2 Resistive Load Drive

When driving a resistive load, a pull-up resistor is needed in order for SN75468 to sink current and for there to be a logic high level. The COM pin can be left floating for these applications.
10 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information
SN75468 will typically be used to drive a high voltage and/or current peripheral from an MCU or logic device that cannot tolerate these conditions. The following design is a common application of SN75468, driving inductive loads. This includes motors, solenoids & relays. Each load type can be modeled by what’s seen in Figure 16.

10.2 Typical Application

![Figure 16. SN75468 as Inductive Load Driver](image)

10.2.1 Design Requirements
For this design example, use the parameters listed in Table 1 as the input parameters.

<table>
<thead>
<tr>
<th>DESIGN PARAMETER</th>
<th>EXAMPLE VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPIO Voltage</td>
<td>3.3 V or 5.0 V</td>
</tr>
<tr>
<td>Coil Supply Voltage</td>
<td>12 V to 100 V</td>
</tr>
<tr>
<td>Number of Channels</td>
<td>7</td>
</tr>
<tr>
<td>Output Current (R_COIL)</td>
<td>20 mA to 300 mA per channel</td>
</tr>
<tr>
<td>Duty Cycle</td>
<td>100%</td>
</tr>
</tbody>
</table>
10.2.2 Detailed Design Procedure

When using SN75468 in a coil driving application, determine the following:
- Input voltage range
- Temperature range
- Output and drive current
- Power dissipation

10.2.2.1 Drive Current

The coil current is determined by the coil voltage (VSUP), coil resistance & output low voltage (VOL or VCE(SAT)).

\[ I_{COIL} = \frac{(V_{SUP} - V_{CE(SAT)})}{R_{COIL}} \]  

(1)

10.2.2.2 Output Low Voltage

The output low voltage (VOL) is the same thing as VCE(SAT) and can be determined by the Electrical Characteristics table, Figure 1, or Figure 2.

10.2.2.3 Power Dissipation & Temperature

The number of coils driven is dependent on the coil current and on-chip power dissipation. The number of coils driven can be determined by Figure 4 or Figure 5.

For a more accurate determination of number of coils possible, use the below equation to calculate SN75468 on-chip power dissipation \( P_D \):

\[ P_D = \sum_{i=1}^{N} V_{OLi} \times I_{Li} \]

Where:
- \( N \) is the number of channels active together.
- \( V_{OLi} \) is the OUT\( i \) pin voltage for the load current \( I_{Li} \). This is the same as \( V_{CE(SAT)} \)

(2)

In order to guarantee reliability of SN75468 and the system the on-chip power dissipation must be lower that or equal to the maximum allowable power dissipation (PD\(_{(MAX)}\)) dictated by below equation Equation 3.

\[ PD_{(MAX)} = \frac{(T_{J(MAX)} - T_A)}{\theta_{JA}} \]

Where:
- \( T_{J(MAX)} \) is the target maximum junction temperature.
- \( T_A \) is the operating ambient temperature.
- \( \theta_{JA} \) is the package junction to ambient thermal resistance.

(3)

It is recommended to limit SN75468 IC’s die junction temperature to less than 125°C. The IC junction temperature is directly proportional to the on-chip power dissipation.
10.2.3 Application Curves

The following curves were generated with SN75468 driving an OMRON G5NB relay – $V_{in} = 5.0\text{V}$; $V_{sup} = 12\text{ V}$ & $R_{COIL} = 2.8\text{ k\Omega}$

![Graph](image1.png)

![Graph](image2.png)

Figure 17. Output Response With Activation of Coil (Turn On)

Figure 18. Output Response With De-activation of Coil (Turn Off)

10.3 System Examples

![Schematic](image3.png)

Figure 19. TTL to Load Schematic
System Examples (continued)

Figure 20. Buffer to Higher Current Loads Schematic

Figure 21. Pull-up Resistor Schematic
11 Power Supply Recommendations

This part does not need a power supply; however, the COM pin is typically tied to the system power supply. When this is the case, it is very important to make sure that the output voltage does not heavily exceed the COM pin voltage. This will heavily forward bias the fly-back diodes and cause a large current to flow into COM, potentially damaging the on-chip metal or over-heating the part.

12 Layout

12.1 Layout Guidelines

Thin traces can be used on the input due to the low current logic that is typically used to drive SN75468. Care must be taken to separate the input channels as much as possible, as to eliminate cross-talk. Thick traces are recommended for the output, in order to drive whatever high currents that may be needed. Wire thickness can be determined by the trace material's current density and desired drive current.

Since all of the channels currents return to a common emitter, it is best to size that trace width to be very wide. Some applications require up to 2.5 A.

12.2 Layout Example

![Figure 22. Package Layout](image-url)
13 Device and Documentation Support

13.1 Related Links
The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

<table>
<thead>
<tr>
<th>PARTS</th>
<th>PRODUCT FOLDER</th>
<th>SAMPLE &amp; BUY</th>
<th>TECHNICAL DOCUMENTS</th>
<th>TOOLS &amp; SOFTWARE</th>
<th>SUPPORT &amp; COMMUNITY</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN75468</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
</tr>
<tr>
<td>SN75469</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
</tr>
</tbody>
</table>

13.2 Trademarks
All trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

SLYZ022 — Ti Glossary.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing Qty</th>
<th>Package Qty</th>
<th>Pins</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN75468D</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>16</td>
<td>40</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>SN75468</td>
<td>Samples</td>
</tr>
<tr>
<td>SN75468DE4</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>16</td>
<td>40</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>SN75468</td>
<td>Samples</td>
</tr>
<tr>
<td>SN75468DR</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>16</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>SN75468</td>
<td>Samples</td>
</tr>
<tr>
<td>SN75468N</td>
<td>ACTIVE</td>
<td>PDIP</td>
<td>N</td>
<td>16</td>
<td>25</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
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<td>N / A for Pkg Type</td>
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<td>Samples</td>
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</table>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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### TAPE AND REEL INFORMATION

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<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
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*All dimensions are nominal.*
**TAPE AND REEL BOX DIMENSIONS**

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*All dimensions are nominal*
MECHANICAL DATA

D (R-PDSO-G16) PLASTIC SMALL OUTLINE

0.394 (10.00) 0.386 (3.80)

Pin 1 Index Area

0.244 (6.20) 0.228 (5.80)

0.157 (4.00) 0.150 (3.80)

0.020 (0.51) 0.012 (0.31)
⊕ 0.010 (0.25) (10)

0.050 (1.27)

0.069 (1.75) Max

0.004 (0.10)

0.010 (0.25) 0.005 (0.13)

0.010 (0.25) 0.004 (0.10)

Gauge Plane

0.050 (1.27) 0.016 (0.40)

Sealing Plane

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

⚠️ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.

⚠️ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.

E. Reference JEDEC MS-012 variation AC.

4040047-6/M 06/11
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.15.

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MECHANICAL DATA

N (R−PDIP−T**)  PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN

<table>
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<tr>
<th>DIM</th>
<th>PINS **</th>
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<td>0.850 (21.59)</td>
<td>0.940 (23.88)</td>
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</table>

| MS−001 VARIATION | AA | BB | AC | AD |

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

△ Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002
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