SN75ALS174A Quadruple Differential Line Driver

1 Features

- Meets or exceeds the requirements of ANSI EIA/TIA-422-B and RS-485
- High-speed advanced low-power Schottky circuitry
- Designed for up to 20Mbit/s operation in both serial and parallel applications
- Designed for multipoint transmission on long bus lines in noisy environments
- Low supply current requirements 55mA max
- Wide positive and negative input/output bus voltage ranges
- Driver output capacity: 60mA
- Thermal-shutdown protection
- Driver positive- and negative-current limiting
- Functionally interchangeable with SN75174

2 Applications

- Motor drives
- Factory automation and control

3 Description

The SN75ALS174A is a quadruple line driver with tri-state differential outputs. It is designed to meet the requirements of ANSI Standards EIA/TIA-422-B and RS-485. This device is optimized for balanced multipoint bus transmission at rates of up to 20Mbit/s.

Each driver features wide positive and negative common-mode output voltage ranges that make them suitable for party-line applications in noisy environments.

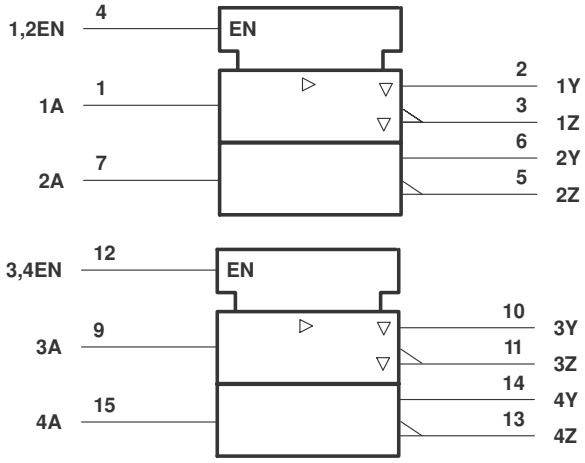
The SN75ALS174A provides positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. Shutdown occurs at a junction temperature of approximately 150°C.

The SN75ALS174A is characterized for operation from 0°C to 70°C.

Package Information

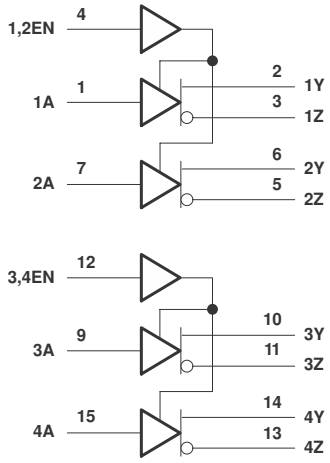
PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
SN75ALS174A	PDIP (N) (16)	19.3mm x 9.4mm
	SOIC (DW) (20)	12.8mm x 10.3mm
	TSSOP (PW) (20)	6.5mm x 6.4mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



A. Pin numbers shown are for the N package.

Logic Symbol [1]



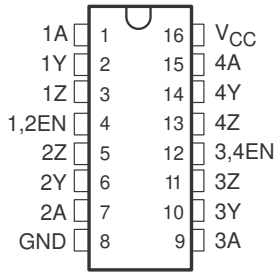
A. Pin numbers shown are for the N package.

Logic Diagram (Positive Logic)

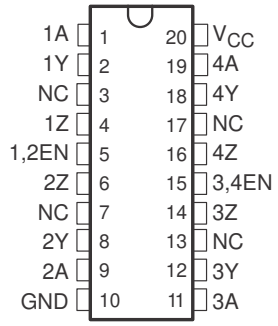
[1] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Table of Contents

4 Pin Configuration and Functions



N Package (Top View)



NC – No internal connection

DW, PW Package (Top View)

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage, V_{CC} (2)	-0.5	7	V
Input voltage, V_I	-0.5	7	V
Output voltage range, V_O	–9	14	V
Continuous total dissipation	See the *Dissipation Rating* table		
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network GND.

5.2 Dissipation Rating Table

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW	596 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2		V_{cc}	V
V_{IL}	Low-level input voltage	0		0.8	V
V_{OC}	Common-mode output voltage	-7		12	V
I_{OH}	High-level output current	0		–60	mA
I_{OL}	Low-level output current	0		60	mA
T_A	Operating free-air temperature	0		70	°C

5.4 Thermal Information

THERMAL METRIC(1)		SN75ALS174A			UNIT
		N (PDIP)	DW (SOIC)	PW	
		16 PINS	20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60.6	66.8	107.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.1	34.4	38.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.6	39.7	53.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	27.5	8.9	3.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	40.3	39	53.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18mA				–1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100Ω	See Note Figure 6-1	1/2 V_{OD1} or 2(2)			V
		R_L = 54Ω		1.5	2.5	5	V
$\|V_{OD3}\|$	Differential output voltage	See (5)		1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage(3)	R_L = 54Ω or 100Ω	See Figure 6-1			±0.2	V
V_{OC}	Common-mode output voltage(4)	R_L = 54Ω or 100Ω	See Figure 6-1			3	V
						–1	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage(3)	R_L = 54Ω or 100Ω	See Figure 6-1			±0.2	V
I_O	Output current with power off	V_{CC} = 0, V_O = –7V to 12V				±100	µA
I_{OZ}	High-impedance-state output current	V_O = –7V to 12V				±100	µA
I_{IH}	High-level input current	V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_I = 0.4V				–100	µA
I_{OS}	Short-circuit output current	V_O = –7V to 12V				±250	mA
I_{CC}	Supply current (all drivers)	No load	Outputs enabled		36	55	mA
			Outputs disabled		16	30	mA

(1) All typical values are at V_{CC} = 5V and T_A = 25°C.
(2) The minimum V_{OD2} with a 100Ω load is either 1/2V_{OD1} or 2V, whichever is greater.
(3) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
(4) In ANSI Standard EIA/TIA-422-B, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
(5) See EIA Standard RS-485, Figures 3-5, Test Termination Measurement 2.

5.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted), C_L = 50pF

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	R_L = 54Ω, See Figure 6-2	9	15	22	ns
t_{PZH}	Output enable time to high level	R_L = 110Ω, See Figure 6-3	30	45	70	ns
t_{PZL}	Output enable time to low level	R_L = 110Ω, See Figure 6-4	25	40	65	ns
t_{PHZ}	Output disable time from high level	R_L = 110Ω, See Figure 6-3	10	20	35	ns
t_{PLZ}	Output disable time from low level	R_L = 110Ω, See Figure 6-4	10	30	45	ns

6 Parameter Measurement Information

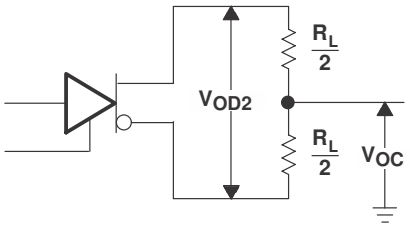
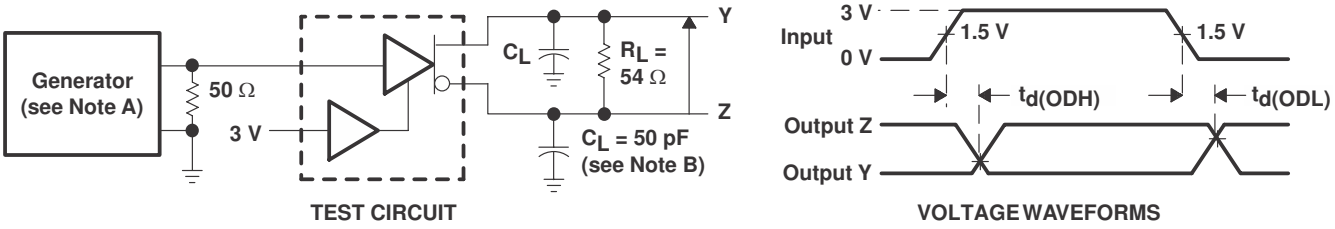
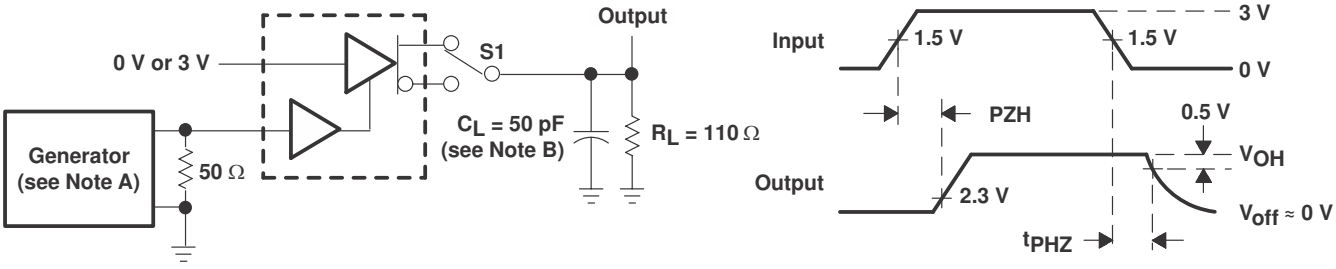


Figure 6-1. Differential and Common-Mode Output Voltages



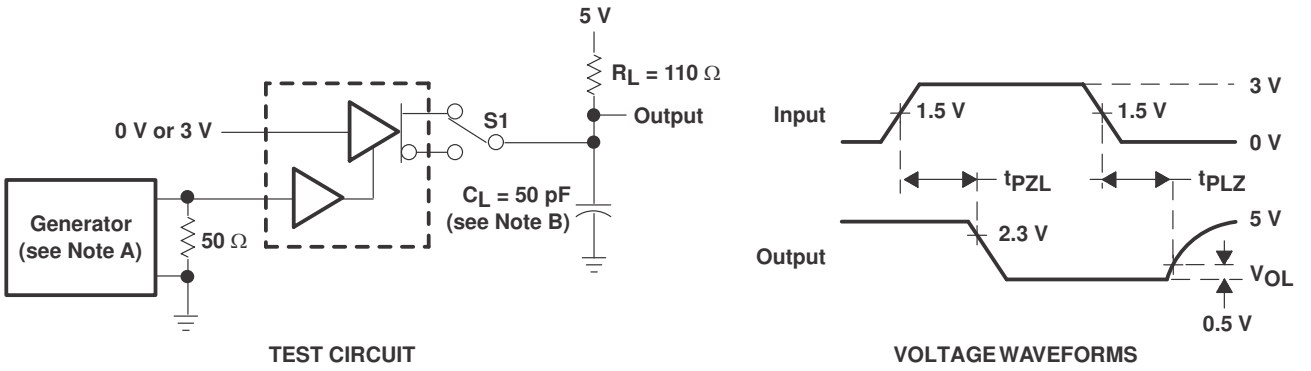
A. The input pulse is supplied by a generator having the following characteristics: PRR = 1MHz, Z_O = 50Ω, duty cycle = 50%, t_f 5ns, t_r 5ns.
B. C_L includes probe and stray capacitance.

Figure 6-2. Differential-Output Test Circuit and Delay and Transition Times Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics: PRR = 1MHz, Z_O = 50Ω, duty cycle = 50%, t_f 10ns, t_r 10ns.
B. C_L includes probe and stray capacitance.

Figure 6-3. Test Circuit and Voltage Waveforms, t_{PZH} and t_{PHZ}



A. The input pulse is supplied by a generator having the following characteristics: PRR = 1MHz, Z_O = 50Ω, duty cycle = 50%, t_f 5ns, t_r 5ns.
B. C_L includes probe and stray capacitance.

Figure 6-4. Test Circuit and Voltage Waveforms, t_{PZL} and t_{PLZ}

7 Detailed Description

7.1 Device Functional Modes

Function Table (each driver)

INPUT A(1) (2)	ENABLES	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

(1) H = high level, L = low level, X = irrelevant.
(2) Z = high impedance (off)

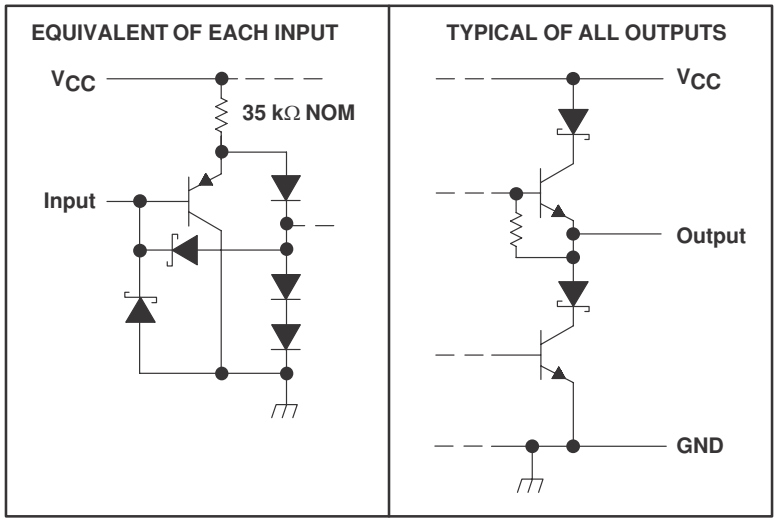


Figure 7-1. Schematics of Inputs and Outputs

8 Device and Documentation Support

8.1 Documentation Support

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (January 2018) to Revision G (April 2024)	Page
• Changed the numbering format for tables, figures, and cross-references throughout the document	1
• Added the *Thermal Information* table	4
• Changed Note A in Figure 6-3	6

Changes from Revision E (April 1998) to Revision F (January 2018)	Page
• Added the PW package, *Applications* list, *Device Information* table, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN75ALS174ADW	Obsolete	Production	SOIC (DW) | 20	-	-	Call TI	Call TI	0 to 70	75ALS174A
SN75ALS174ADWR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS174A
SN75ALS174ADWR.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS174A
SN75ALS174AN	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75ALS174AN
SN75ALS174AN.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75ALS174AN
SN75ALS174APWR	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS174A
SN75ALS174APWR.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS174A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

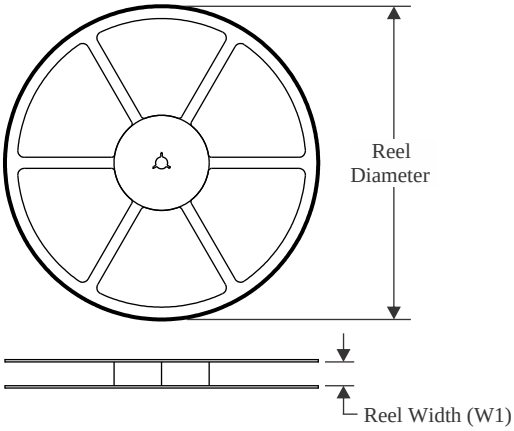
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

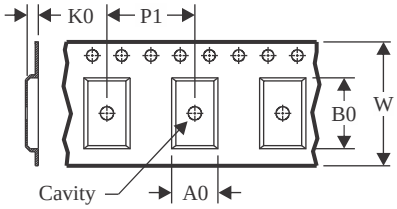
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

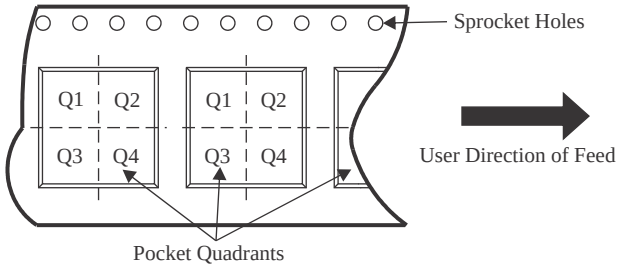


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

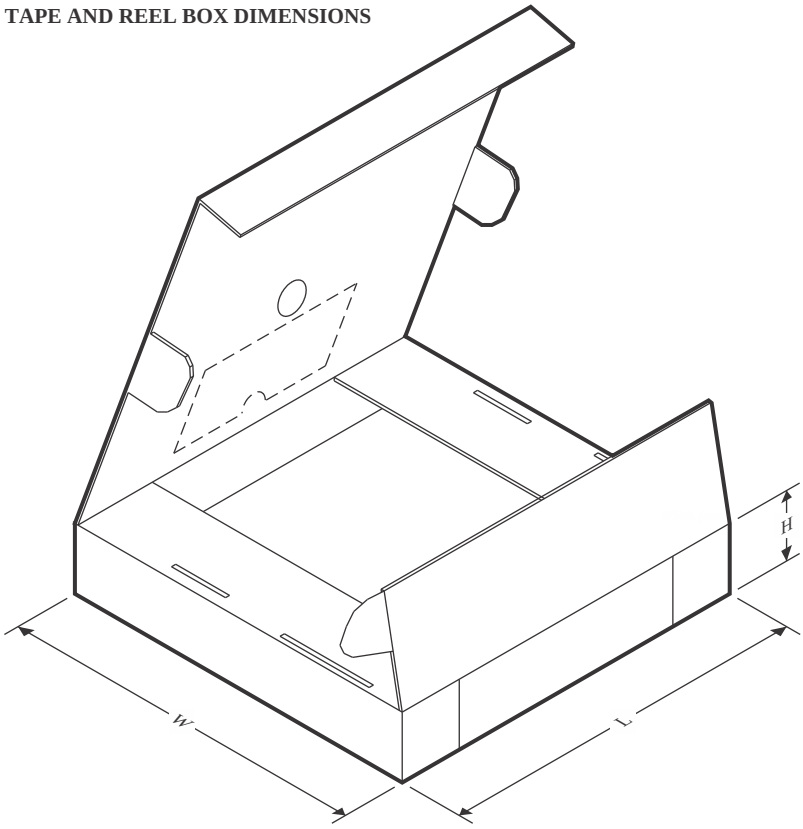
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75ALS174ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN75ALS174APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

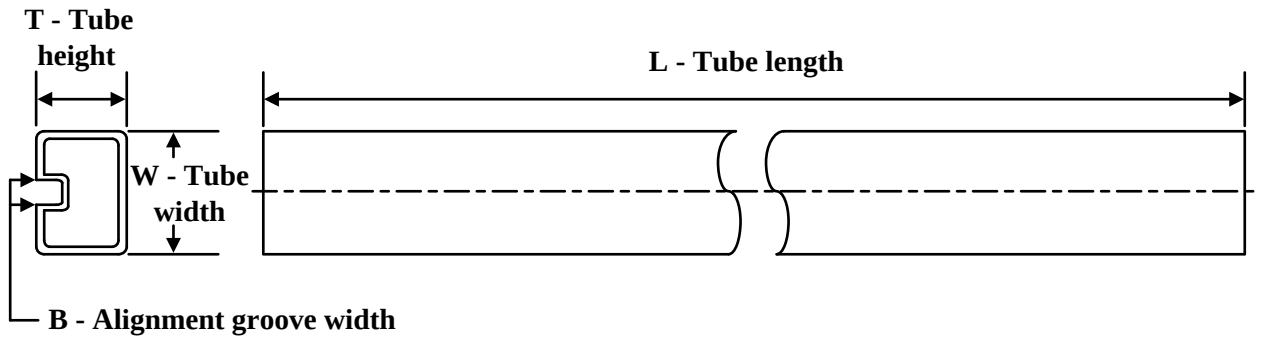
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75ALS174ADWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN75ALS174APWR	TSSOP	PW	20	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

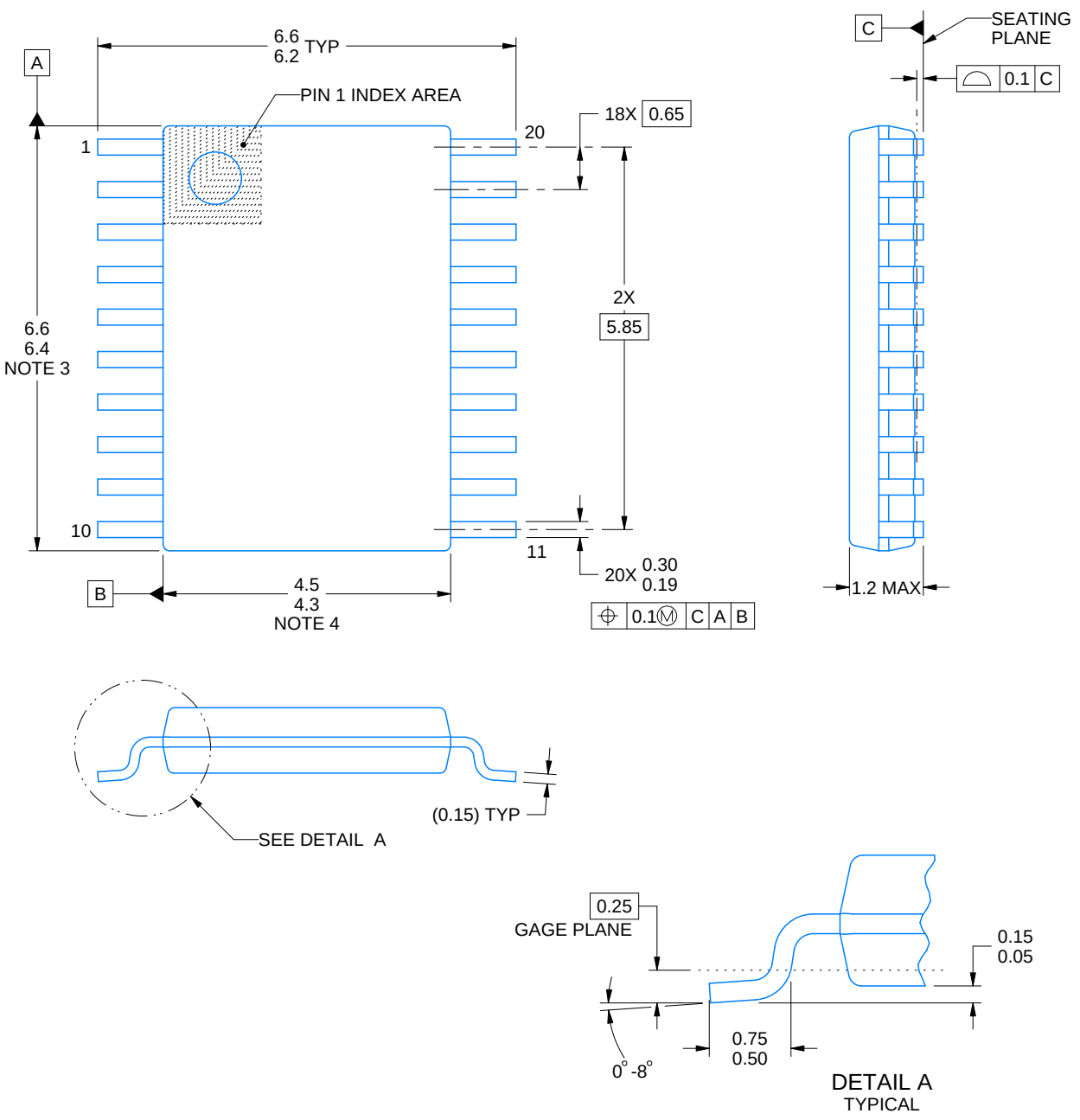
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN75ALS174AN	N	PDIP	16	25	506	13.97	11230	4.32
SN75ALS174AN.A	N	PDIP	16	25	506	13.97	11230	4.32

PACKAGE OUTLINE

PW0020A

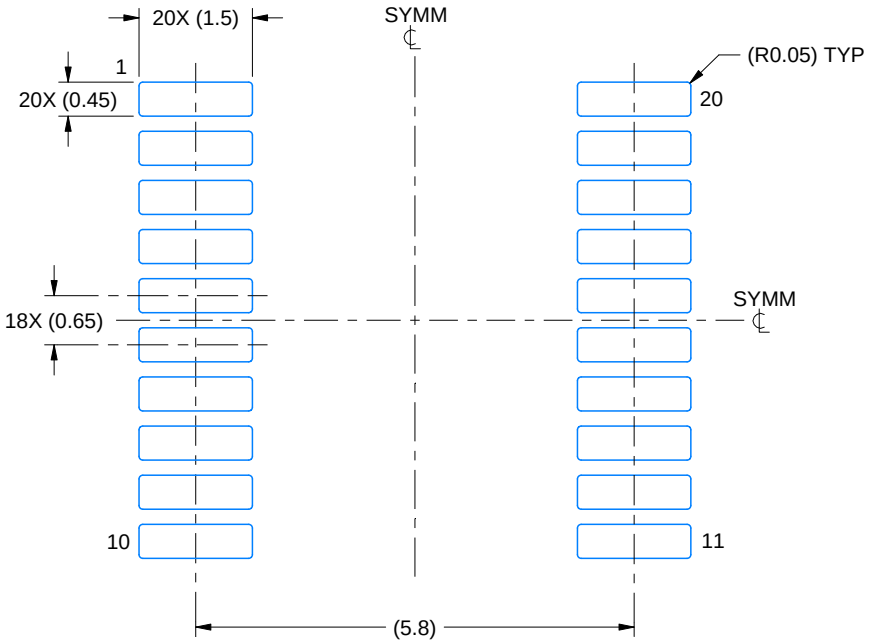
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



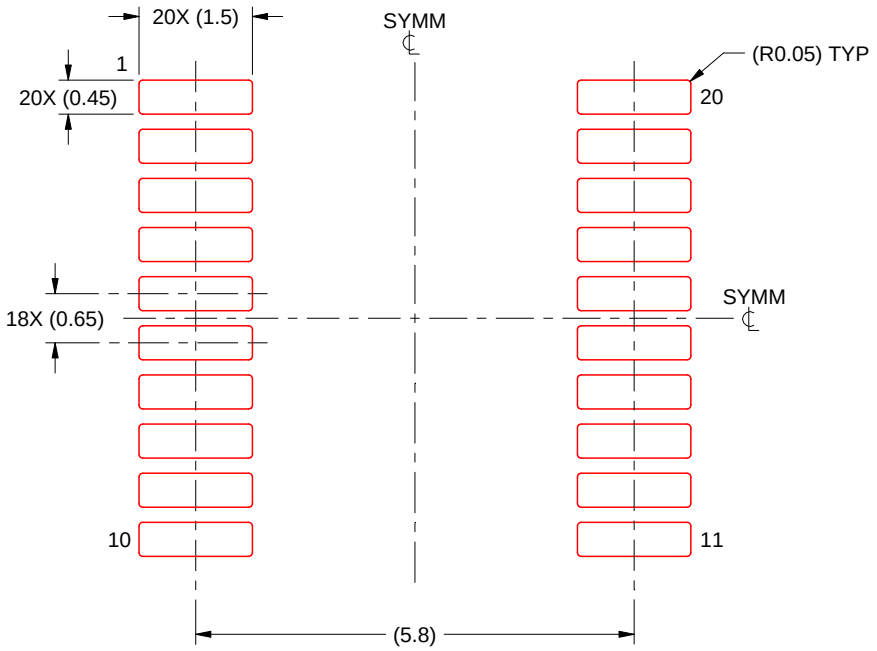
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

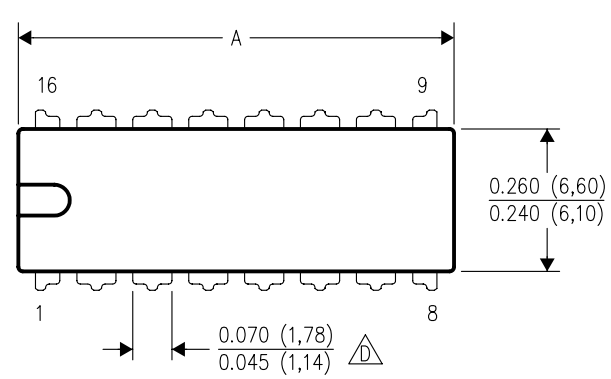
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

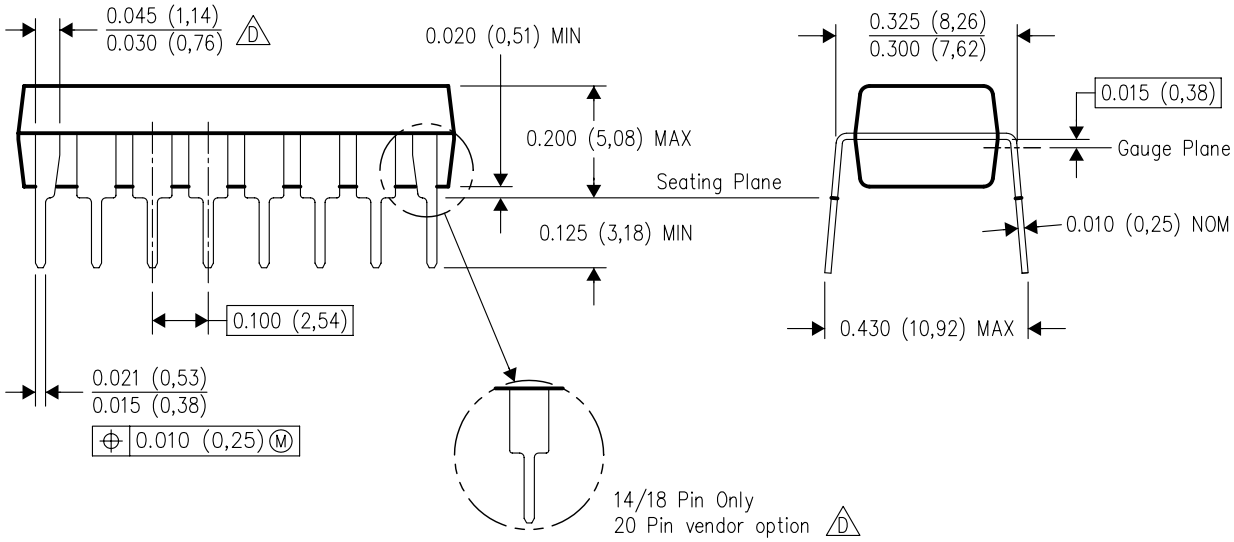
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

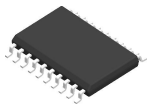


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

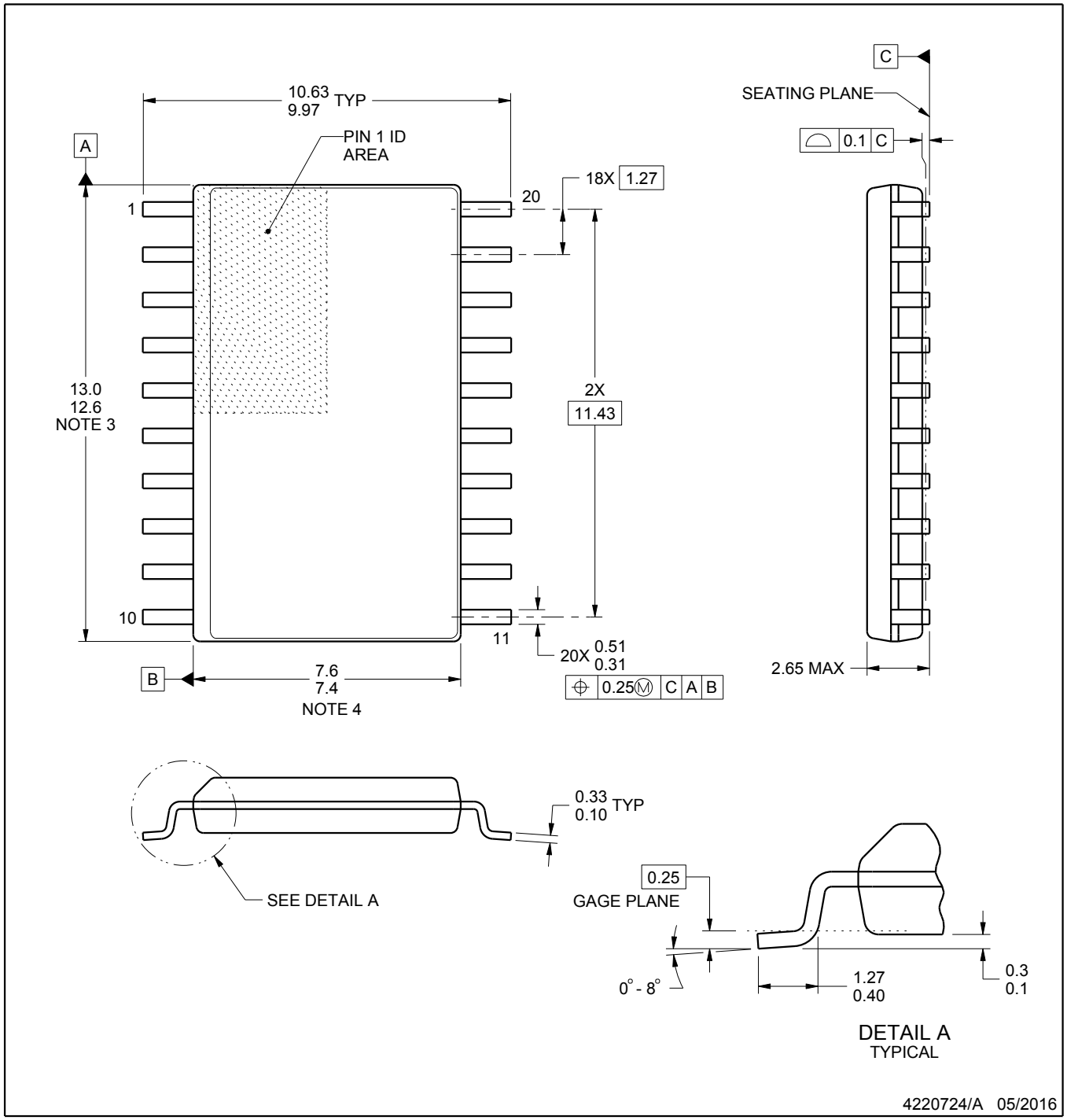


PACKAGE OUTLINE

DW0020A

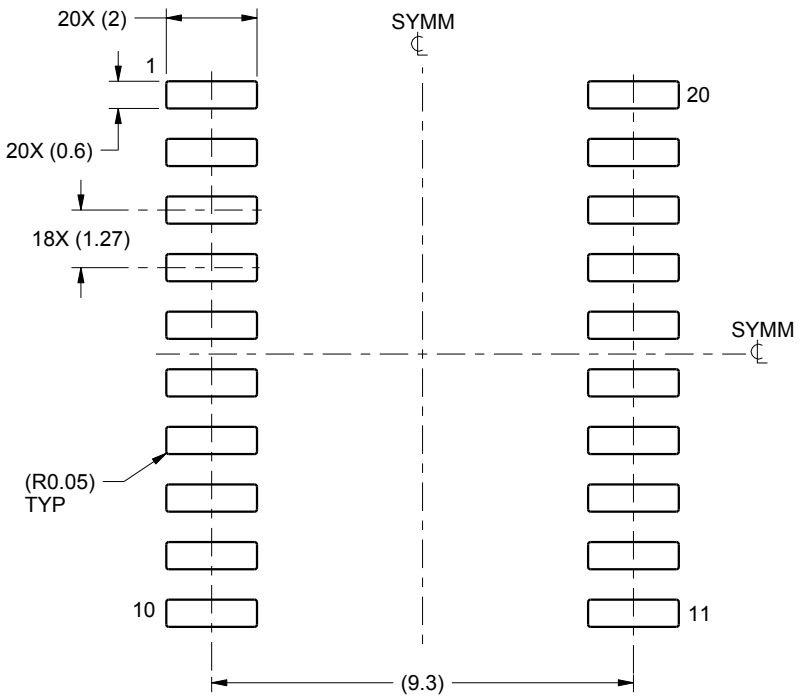
SOIC - 2.65 mm max height

SOIC

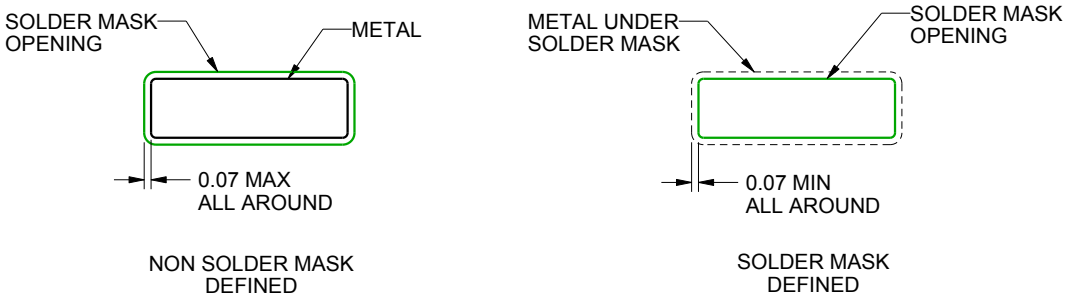


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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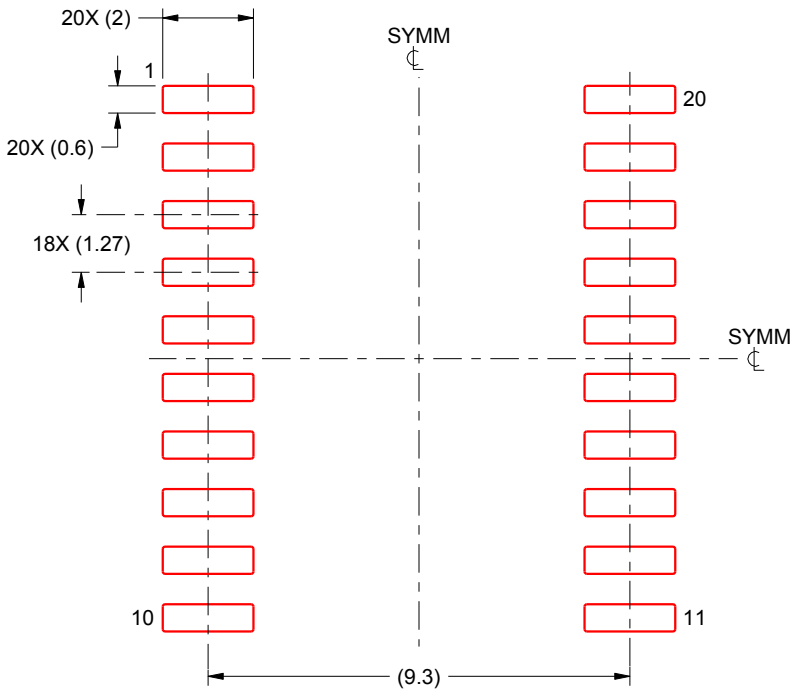
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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