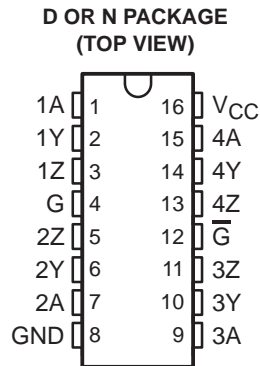


SN75ALS192 QUADRUPLE DIFFERENTIAL LINE DRIVER

SLLS007D – JULY 1985 – REVISED APRIL 1998

- Meets or Exceeds the Requirements of ANSI Standard EIA/TIA-422-B and ITU Recommendation V.11
- Designed to Operate up to 20 Mbaud
- 3-State TTL Compatible
- Single 5-V Supply Operation
- High Output Impedance in Power-Off Condition
- Complementary Output-Enable Inputs
- Improved Replacement for the AM26LS31



description

The four differential line drivers are designed for data transmission over twisted-pair or parallel-wire transmission lines. They meet the requirements of ANSI Standard EIA/TIA-422-B and ITU Recommendations V.11 and are compatible with 3-state TTL circuits. Advanced low-power Schottky technology provides high speed without the usual power penalties. Standby supply current is typically only 26 mA, while typical propagation delay time is less than 10 ns.

High-impedance inputs maintain low input currents, less than 1 μ A for a high level and less than 100 μ A for a low level. Complementary output-enable inputs (G and \overline{G}) allow these devices to be enabled at either a high input level or low input level. The SN75ALS192 is capable of data rates in excess of 20 Mbit/s and is designed to operate with the SN75ALS193 quadruple line receiver.

The SN75ALS192 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each driver)

INPUT A	ENABLES		OUTPUTS	
	G	\overline{G}	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

H = high level, L = low level, X = irrelevant,
Z = high impedance (off)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

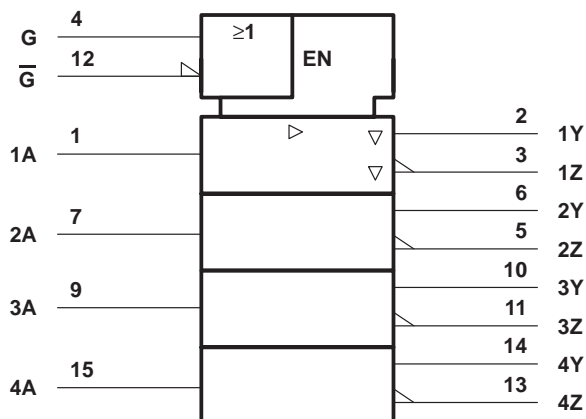
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SN75ALS192 QUADRUPLE DIFFERENTIAL LINE DRIVER

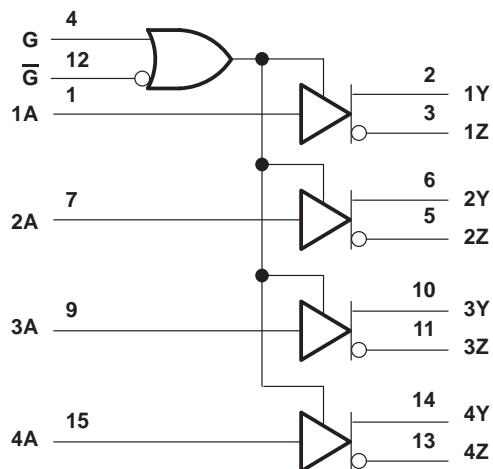
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logic symbol†

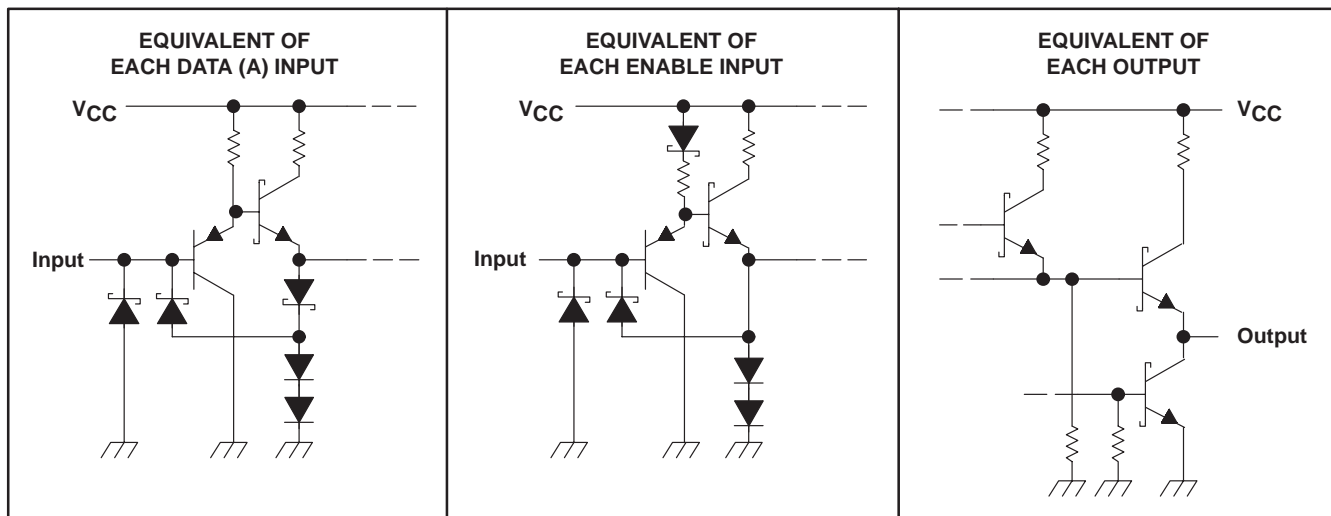


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage, V_I	7 V
Off-state output voltage	6 V
Continuous total dissipation	See Dissipation Rating Table
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values except differential output voltage, V_{OD} , are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	N/A
N	1150 mW	9.2 mW/°C	736 mW	N/A

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			-20	mA
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	0		70	°C

SN75ALS192

QUADRUPLE DIFFERENTIAL LINE DRIVER

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V _{IK}	Input clamp voltage	V _{CC} = MIN,	I _I = -18 mA			-1.5	V
V _{OH}	High-level output voltage	V _{CC} = MIN,	I _{OH} = -20 mA	2.5			V
V _{OL}	Low-level output voltage	V _{CC} = MIN,	I _{OL} = 20 mA			0.5	V
V _O	Output voltage	V _{CC} = MAX,	I _O = 0	0		6	V
V _{OD1}	Differential output voltage	V _{CC} = MIN,	I _O = 0	1.5		6	V
V _{OD2}	Differential output voltage	R _L = 100 Ω,	See Figure 1	1/2 V _{OD1} or 2§			V
Δ V _{OD}	Change in magnitude of differential output voltage¶	R _L = 100 Ω,	See Figure 1			±0.2	V
V _{OC}	Common-mode output voltage#	R _L = 100 Ω,	See Figure 1			±3	V
Δ V _{OC}	Change in magnitude of common-mode output voltage¶	R _L = 100 Ω,	See Figure 1			±0.2	V
I _O	Output current with power off	V _{CC} = 0	V _O = 6 V			100	μA
			V _O = -0.25 V			-100	
I _{OZ}	Off-state (high-impedance state) output current	V _{CC} = MAX	V _O = 0.5 V			-20	μA
			V _O = 2.5 V			20	
I _I	Input current at maximum input voltage	V _{CC} = MAX,	V _I = 7 V			100	μA
I _{IH}	High-level input current	V _{CC} = MAX,	V _I = 2.7 V			20	μA
I _{IL}	Low-level input current	V _{CC} = MAX,	V _I = 0.4 V			-200	μA
I _{OS}	Short-circuit output current	V _{CC} = MAX		-30		-150	mA
I _{CC}	Supply current (all drivers)	V _{CC} = MAX,	All outputs disabled		26	45	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V and T_A = 25°C.

§ The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.

¶ |V_{OD}| and |V_{OC}| are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

In ANSI Standard EIA/TIA-422-B, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

|| Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 2)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t _{PLH}	Propagation delay time, low-to-high-level output	S1 and S2 open,	C _L = 30 pF		6	13	ns
t _{PHL}	Propagation delay time, high-to-low-level output	S1 and S2 open,	C _L = 30 pF		9	14	ns
	Output-to-output skew	S1 and S2 open,	C _L = 30 pF		3	6	ns
t _{PZH}	Output enable time to high level	S1 open and S2 closed			11	15	ns
t _{PZL}	Output enable time to low level	S1 closed and S2 open			16	20	ns
t _{PHZ}	Output disable time from high level	S1 open and S2 closed,	C _L = 10 pF		8	15	ns
t _{PLZ}	Output disable time from low level	S1 and S2 closed,	C _L = 10 pF		18	20	ns



PARAMETER MEASUREMENT INFORMATION

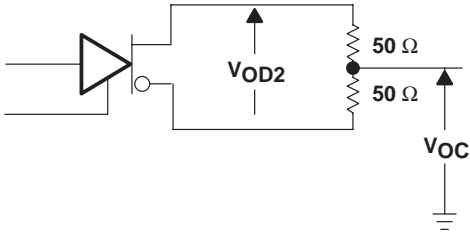
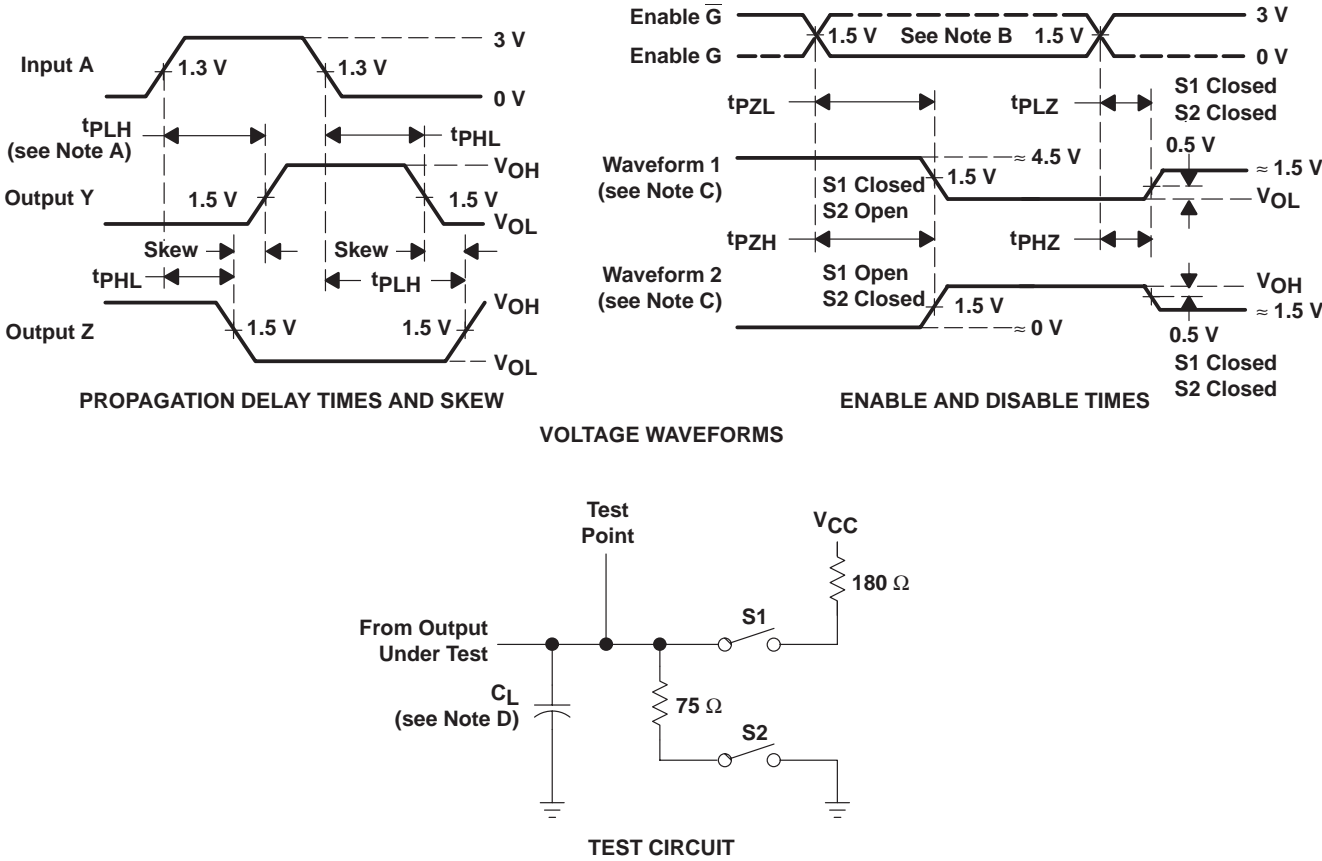


Figure 1. Differential and Common-Mode Output Voltages



- NOTES: A. When measuring propagation delay times and skew, switches S1 and S2 are open.
 B. Each enable is tested separately.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. C_L includes probe and jig capacitance.
 E. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O \approx 50 \Omega$, $t_r \leq 15 \text{ ns}$, and $t_f \leq 6 \text{ ns}$.

Figure 2. Test Circuit and Voltage Waveforms

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TYPICAL CHARACTERISTICS†

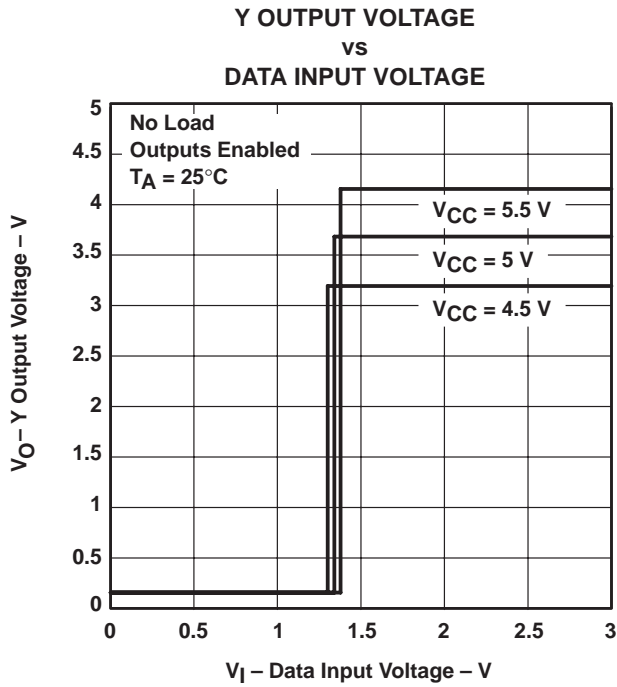


Figure 3

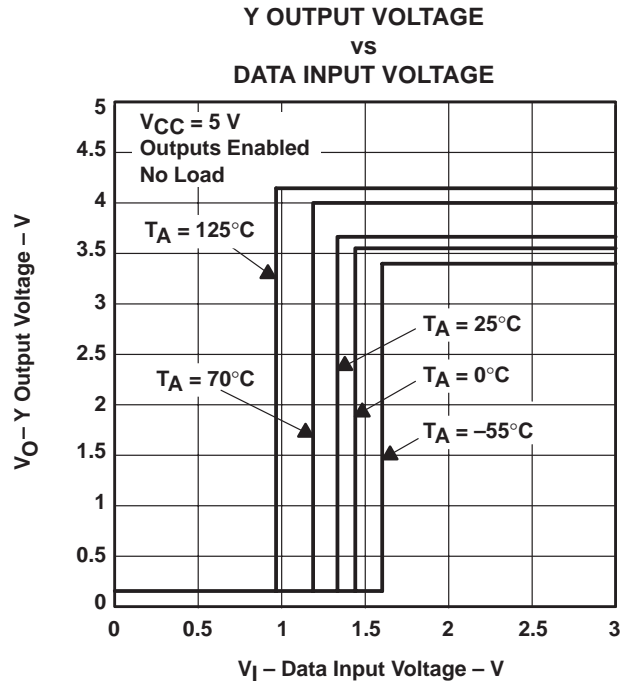


Figure 4

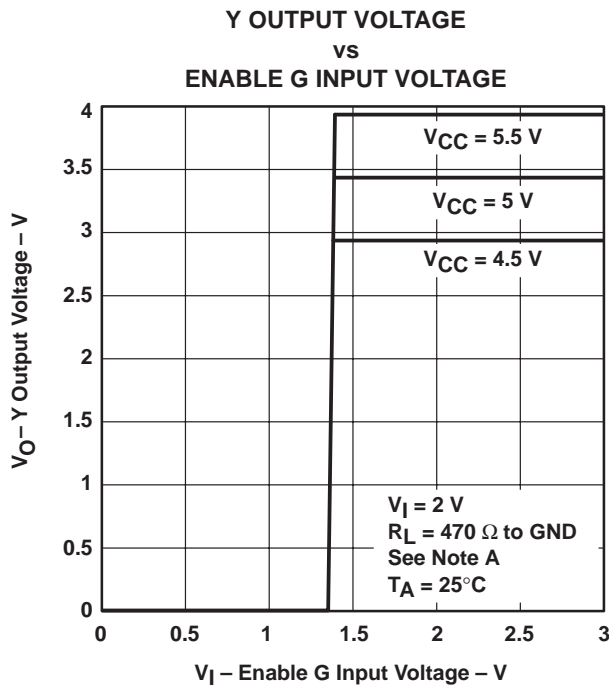


Figure 5

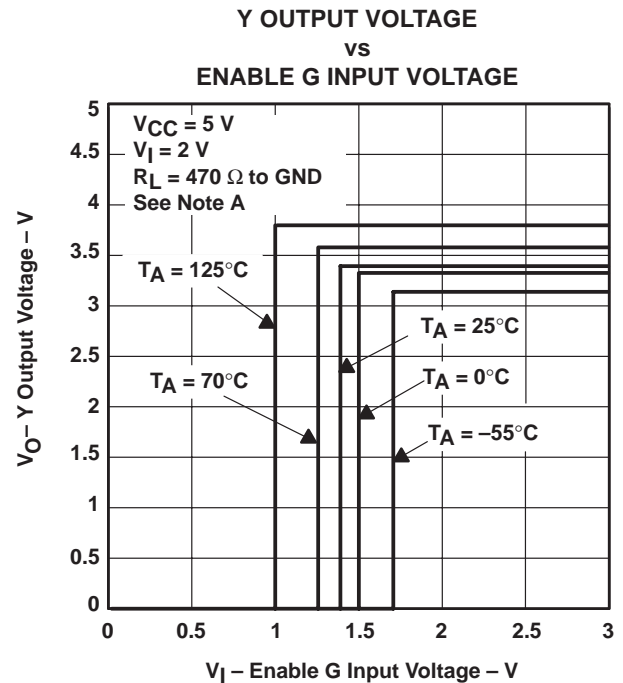


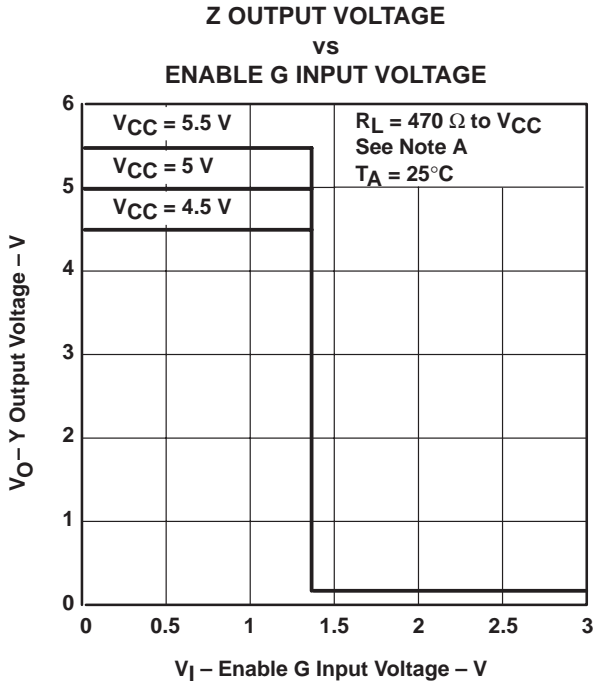
Figure 6

NOTE A: The A input is connected to V_{CC} during the testing of the Y outputs and to ground during the testing of the Z outputs.

NOTE A: The A input is connected to V_{CC} during the testing of the Y outputs and to ground during the testing of the Z outputs.

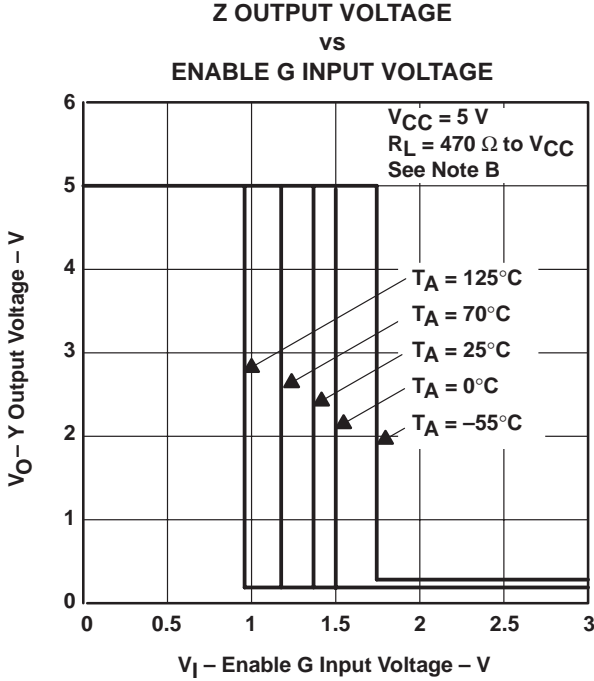
† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

TYPICAL CHARACTERISTICS†



NOTE A: The A input is connected to V_{CC} during the testing of the Y outputs and to ground during the testing of the Z outputs.

Figure 7



NOTE B: The A input is connected to GND during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

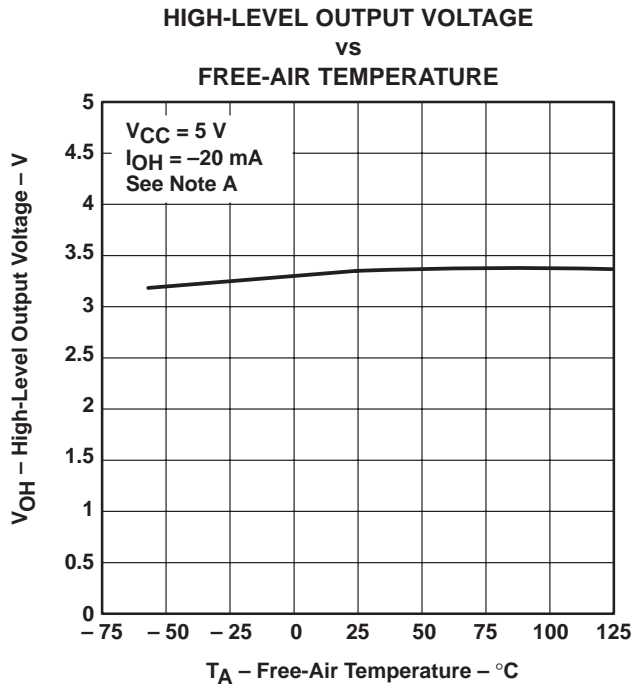
Figure 8

† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

SN75ALS192 QUADRUPLE DIFFERENTIAL LINE DRIVER

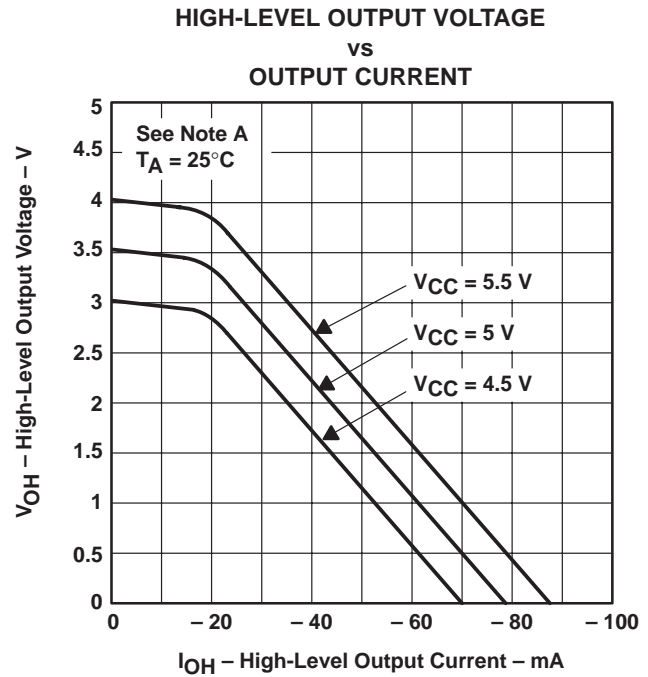
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TYPICAL CHARACTERISTICS†



NOTE A: The A input is connected to V_{CC} during the testing of the Y outputs and to ground during the testing of the Z outputs.

Figure 9

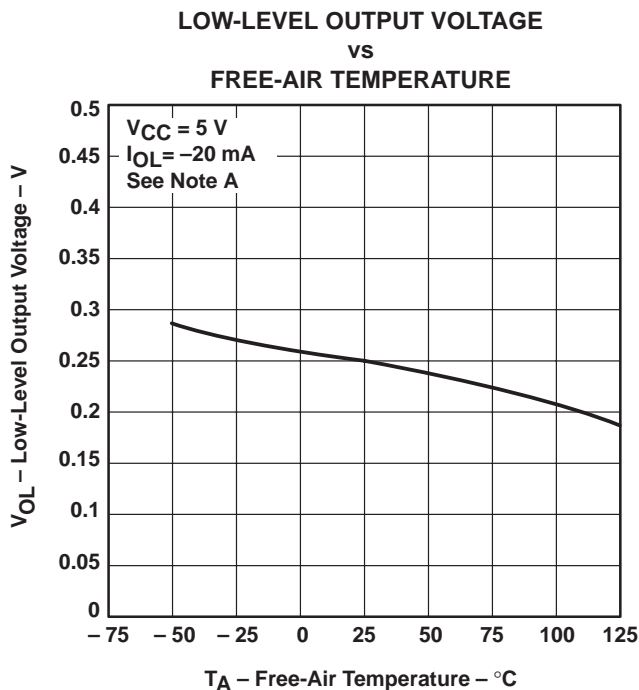


NOTE A: The A input is connected to V_{CC} during the testing of the Y outputs and to ground during the testing of the Z outputs.

Figure 10

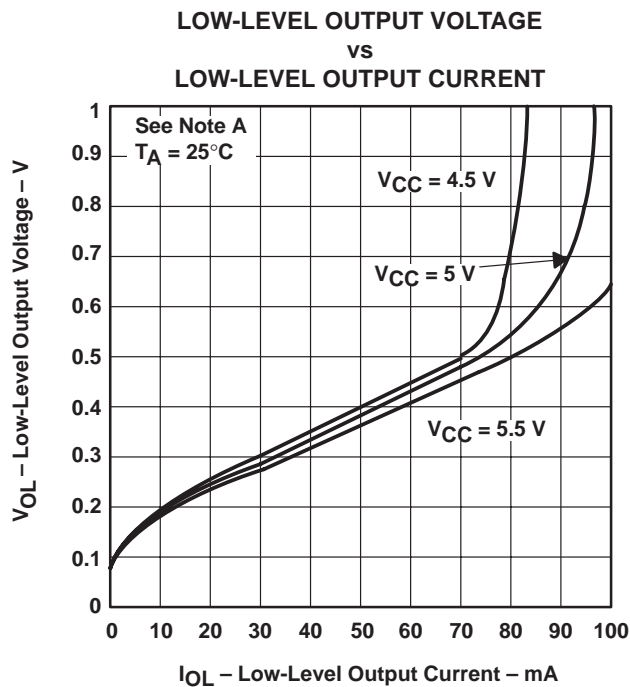
† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

TYPICAL CHARACTERISTICS†



NOTE A: The A input is connected to GND during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

Figure 11



NOTE A: The A input is connected to GND during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

Figure 12

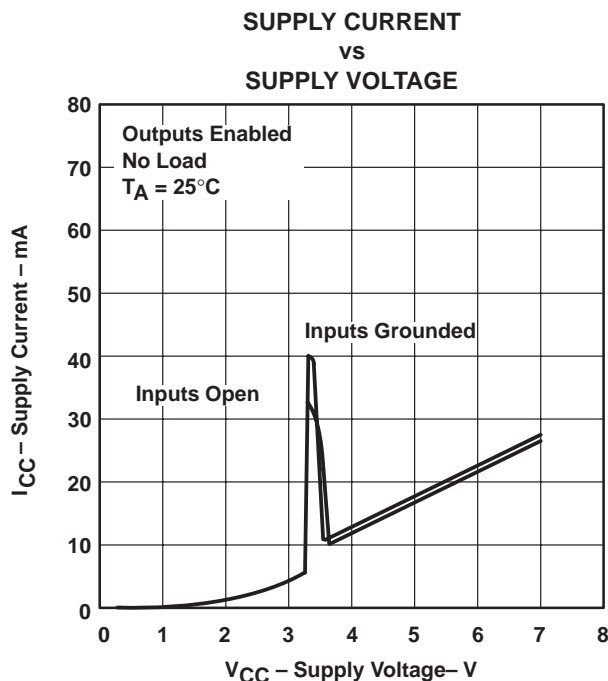


Figure 13

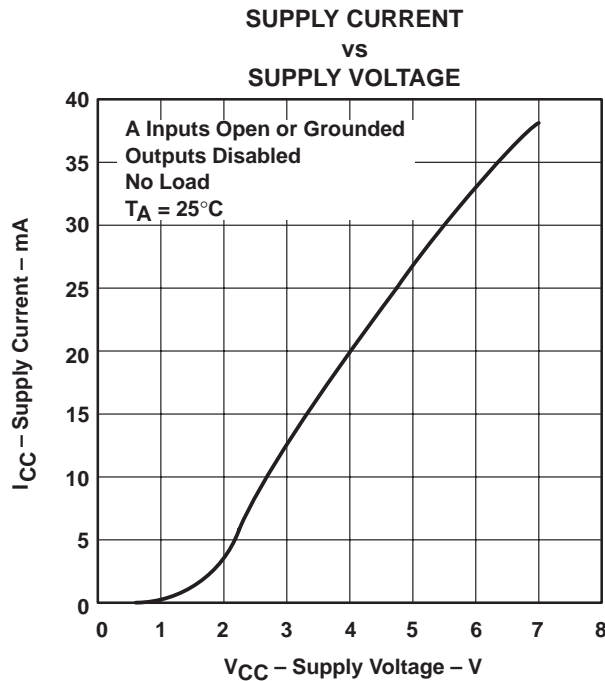


Figure 14

† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

SN75ALS192 QUADRUPLE DIFFERENTIAL LINE DRIVER

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TYPICAL CHARACTERISTICS

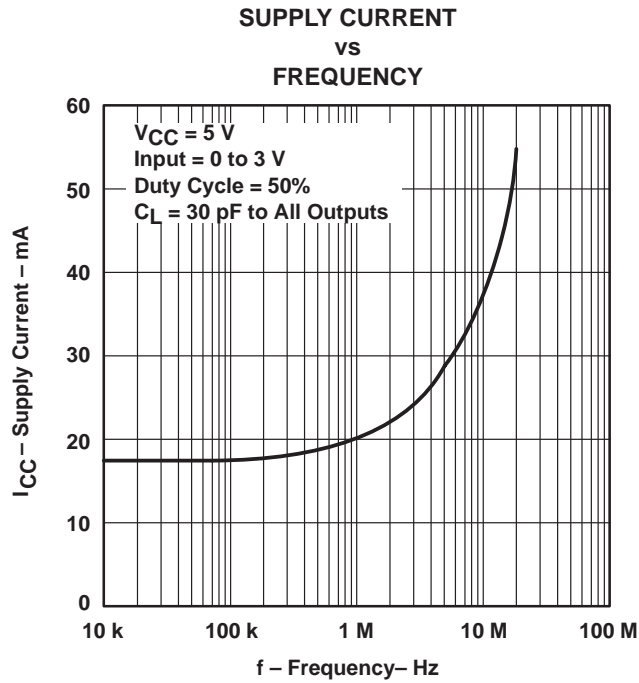


Figure 15

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75ALS192D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS192	Samples
SN75ALS192DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS192	Samples
SN75ALS192N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75ALS192N	Samples
SN75ALS192NE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75ALS192N	Samples
SN75ALS192NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS192	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75ALS192DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN75ALS192NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75ALS192DR	SOIC	D	16	2500	340.5	336.1	32.0
SN75ALS192NSR	SO	NS	16	2000	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN75ALS192D	D	SOIC	16	40	507	8	3940	4.32
SN75ALS192N	N	PDIP	16	25	506	13.97	11230	4.32
SN75ALS192NE4	N	PDIP	16	25	506	13.97	11230	4.32

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002



PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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