SN75ALS193 Quadruple Differential Line Receiver

1 Features

- Meets or exceeds ANSI standard EIA/TIA-422-B and EIA/TIA-423-A and ITU recommendations V.10 and V.11
- Designed for multipoint bus transmission on long bus lines in noisy environments
- 3-state outputs
- Common-mode input voltage range: –7 V to 7 V
- Input sensitivity: ±200 mV
- Input hysteresis: 120-mV typical
- High input impedance: 12-kΩ minimum
- Operates from single 5-V supply
- Low supply current requirement 35-mA maximum
- Improved speed and power version of the AM26LS32A

2 Applications

- Motor drives
- Factory automation and control

3 Description

The SN75ALS193 is a monolithic quadruple line receiver with 3-state outputs designed using advanced low-power Schottky technology. This technology provides combined improvements in bar design, tooling production, and wafer fabrication. This, in turn, provides significantly lower power requirements and permits much higher data throughput than other designs. This device meets the specifications of ANSI Standards EIA/TIA-422-B and EIA/TIA-423-A and ITU Recommendations V.10 and V.11. It features 3-state outputs that permit direct connection to a bus-organized system with a fail-safe design that ensures the outputs will always be high if the inputs are open.

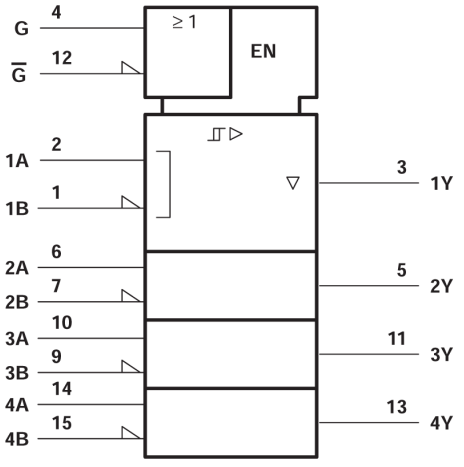
The device is optimized for balanced multipoint bus transmission at rates up to 20 megabits per second. The input features high input impedance, input hysteresis for increased noise immunity, and an input sensitivity of ± 200 mV over a common-mode input voltage range of –7 to 7 V. It also features active-high and active-low enable functions that are common to the four channels. The SN75ALS193 is designed for optimum performance when used with the ’ALS192 quadruple differential line driver.

The SN75ALS193 is characterized for operation from 0°C to 70°C.

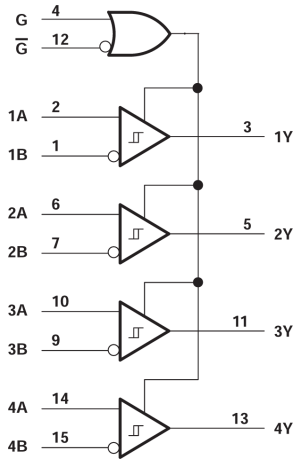
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
SN75ALS193	N (PDIP, 16)	19.3 mm × 9.4 mm
	D (SOIC, 16)	9.9 mm × 6 mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Logic Symbol†



Logic Diagram (Positive Logic)

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Table of Contents

4 Pin Configuration and Functions

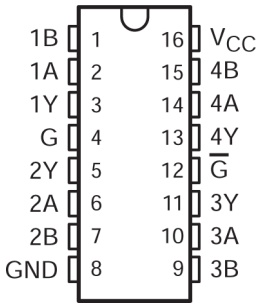


Figure 4-1. D or N Package (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
1B	1	I	Channel 1 Differential Receiver Inverting Input
1A	2	I	Channel 1 Differential Receiver Non-Inverting Input
1Y	3	O	Channel 1 Single Ended Output
G	4	I	Active High Enable
2Y	5	O	Channel 2 Single Ended Output
2A	6	I	Channel 2 Differential Receiver Non-Inverting Input
2B	7	I	Channel 2 Differential Receiver Inverting Input
GND	8	GND	Device GND
3B	9	I	Channel 3 Differential Receiver Inverting Input
3A	10	I	Channel 3 Differential Receiver Non-Inverting Input
3Y	11	O	Channel 3 Single Ended Output
$\overline{G}$	12	I	Active Low Enable
4Y	13	O	Channel 4 Single Ended Output
4A	14	I	Channel 4 Differential Receiver Non-Inverting Input
4B	15	I	Channel 4 Differential Receiver Inverting Input
V_{CC}	16	PWR	Device VCC (4.75V to 5.25V)

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage, see (2)		7	V
V_I	Input voltage, A or B		±15	V
V_{ID}	Differential input voltage, see (3)		±15	V
V_I	Enable input voltage		7	V
I_{OL}	Low-level output current		50	mA
	Continuous total dissipation	See *Dissipation Rating* table		
T_A	Operating free-air temperature range	0	70	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds		300	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential input voltage, are with respect to network ground terminal.
(3) Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.

5.2 Dissipation Rating

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING
N	1150 mW	9.2 mW/°C	736 mW

5.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±7	V
Differential input voltage, V_{ID}			±12	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			–400	µA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0	70		°C

5.4 Thermal Information

THERMAL METRIC(1)		SN75ALS193		UNIT
		N (PDIP)	D (SOIC)	
		16 Pins	16 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60.6	84.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.1	43.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.6	43.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	27.5	10.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	40.3	42.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.5 Electrical Characteristics

over recommended range of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		MIN	TYP[2]	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage					200	mV
V_{IT-}	Negative-going input threshold voltage			–200[3]			mV
V_{hys}	Hysteresis voltage (V_{IT+} -V_{IT-})				120		mV
V_{IK}	Enable-input clamp voltage	V_{CC} = MIN,	I_I = –18 mA			–1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = –400 µA,	V_{ID} = 200 mV, See Figure 1	2.5	1.6		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{ID} = –200 mV, See Figure 1	I_{OL} = 8 mA			0.45	V
			I_{OL} = 16 mA			0.5	
I_{OZ}	High-impedance-state output current	V_{CC} = MAX	V_O = 2.4 V			20	µA
			V_O = 0.4 V			–20	
I_I	Line input current	Other input at 0, See [4]	V_{CC} = MIN, V_I = 15 V		0.7	1.2	mA
			V_{CC} = MIN, V_I = –15 V		–1.0	–1.7	
I_{IH}	High-level enable-input current	V_{CC} = MAX	V_{IH} = 2.7 V			20	µA
			V_{IH} = MAX			100	
I_{IL}	Low-level enable-input current	V_{CC} = MAX,	V_{IL} = 0.4 V			–100	µA
	Input resistance			12	18		kΩ
I_{OS}	Short-circuit output current	V_{CC} = MAX, V_O = 0,	V_{ID} = 3 V, See [5]	–15	–78	–130	mA
I_{CC}	Supply current	V_{CC} = MAX,	Outputs disabled		22	35	mA

(1) For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.
(2) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(3) The algebraic convention, in which the less positive limit is designated minimum, is used in this data sheet for threshold voltage levels only.
(4) Refer to ANSI Standard EIA/TIA-422-B and EIA/TIA-423-A for exact conditions.
(5) Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

5.6 Switching Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = –2.5 V to 2.5 V			15	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF	See Figure 6-1		15	22	
t_{PZH}	Output enable time to high level	C_L =15 pF	See Figure 6-2		13	25	
					11	25	
t_{PHZ}	Output disable time from high level	C_L = 5 pF	See Figure 6-2		13	25	
					15	22	

5.7 Typical Characteristics

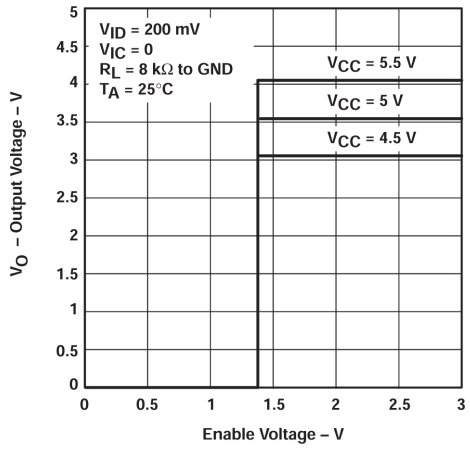


Figure 5-1. Output Voltage vs Enable Voltage

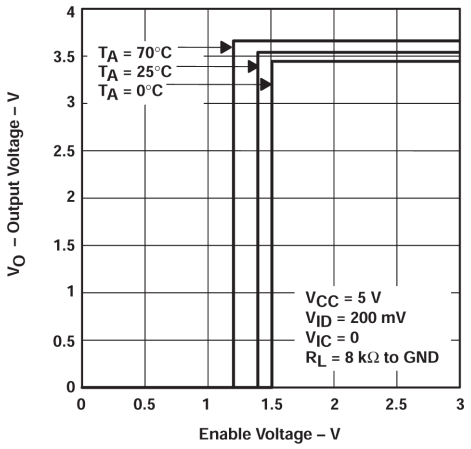


Figure 5-2. Output Voltage vs Enable Voltage

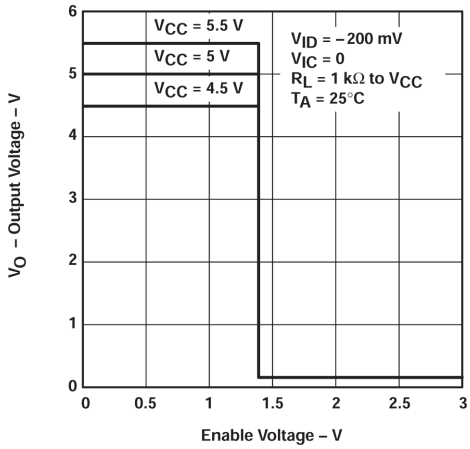


Figure 5-3. Output Voltage vs Enable Voltage

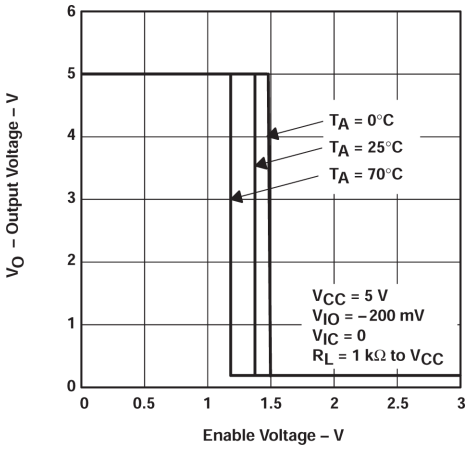


Figure 5-4. Output Voltage vs Enable Voltage

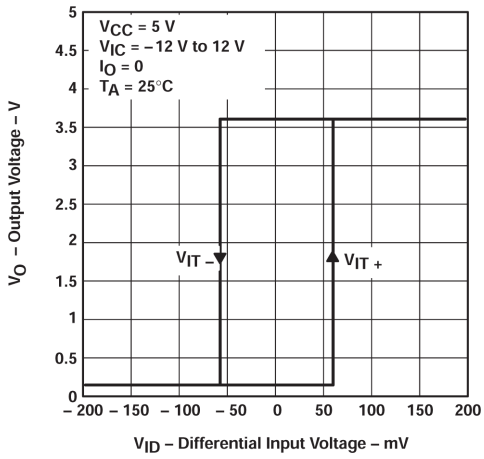


Figure 5-5. Output Voltage vs Differential Input Voltage

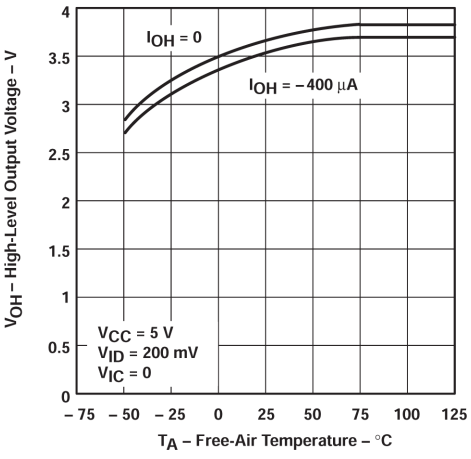


Figure 5-6. High-level Output Voltage vs Free-air Temperature

5.7 Typical Characteristics (continued)

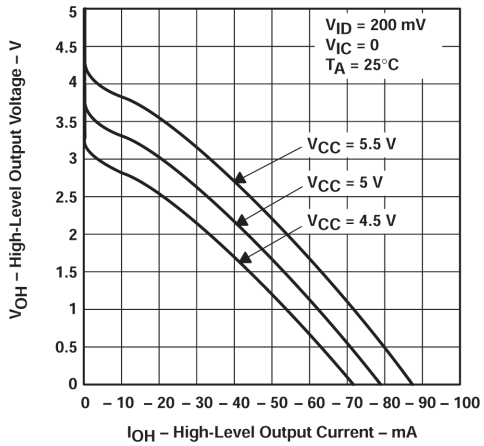


Figure 5-7. High-level Output Voltage vs High-level Output Current

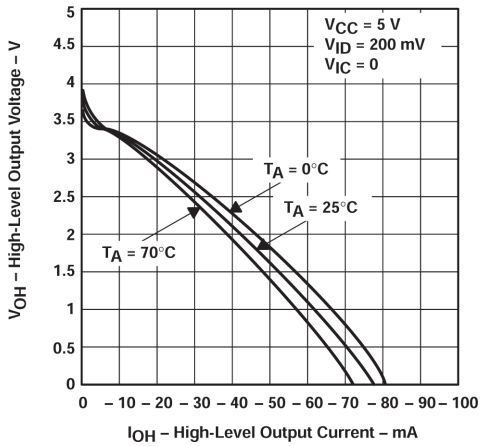


Figure 5-8. High-level Output Voltage vs High-level Output Current

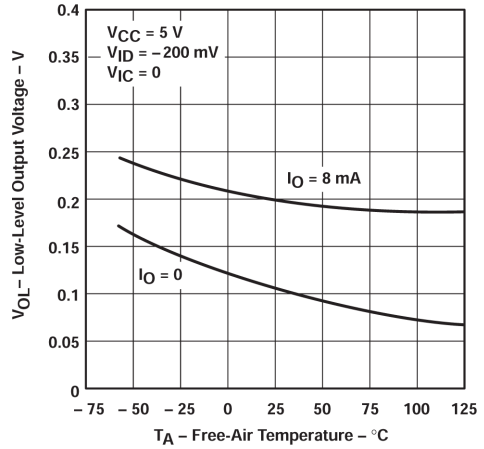


Figure 5-9. Low-level Output Voltage vs Free-air Temperature

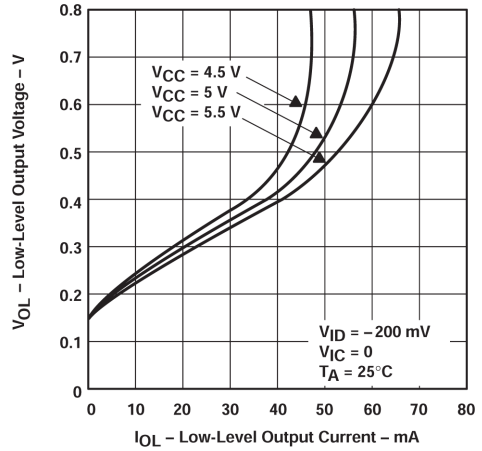


Figure 5-10. Low-level Output Voltage vs Low-level Output Current

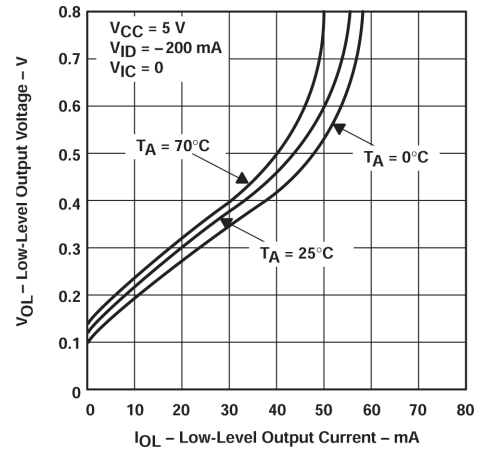


Figure 5-11. Low-level Output Voltage vs Low-level Output Current

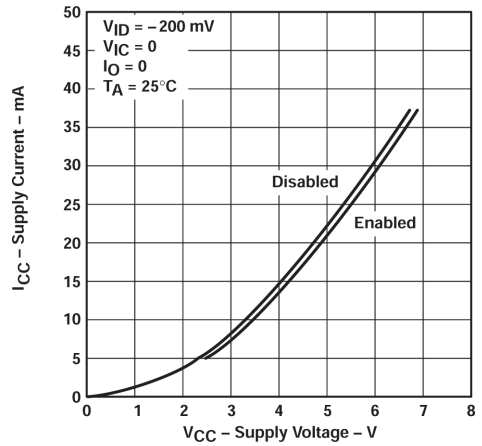


Figure 5-12. Supply Current vs Supply Voltage

5.7 Typical Characteristics (continued)

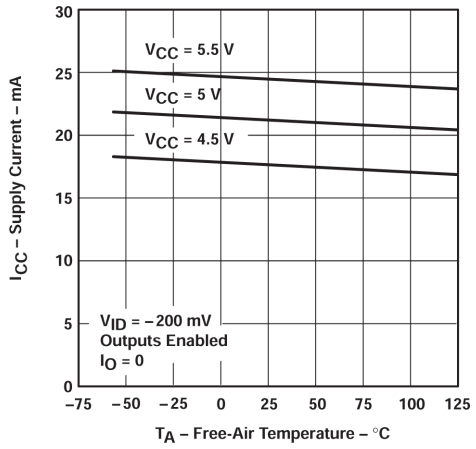


Figure 5-13. Supply Current vs Free-air Temperature

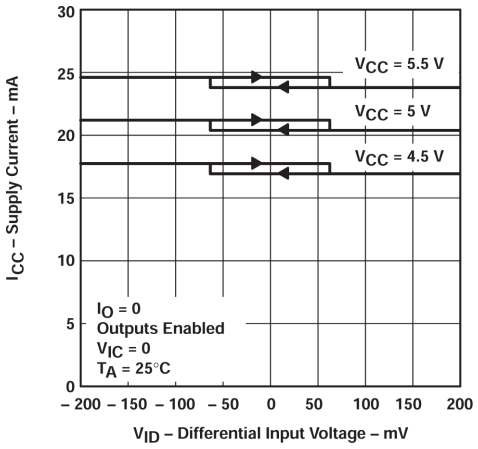


Figure 5-14. Supply Current vs Differential Input Voltage

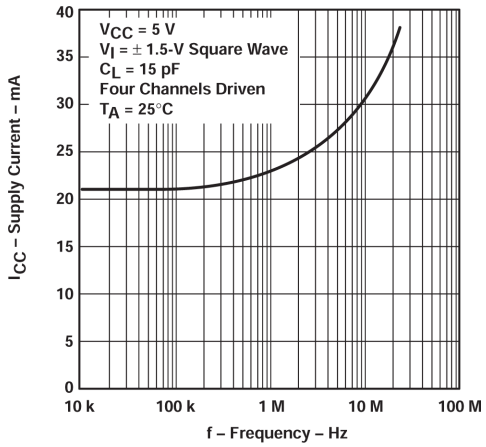


Figure 5-15. Supply Current vs Frequency

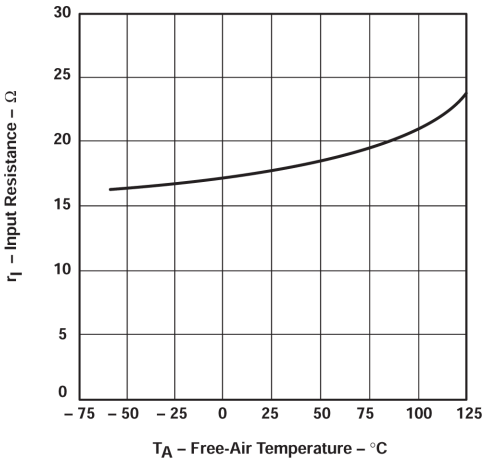


Figure 5-16. Input Resistance vs Free-air Temperature

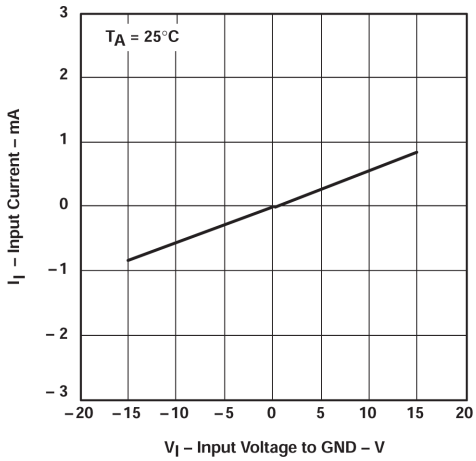


Figure 5-17. Input Current vs Input Voltage to GND

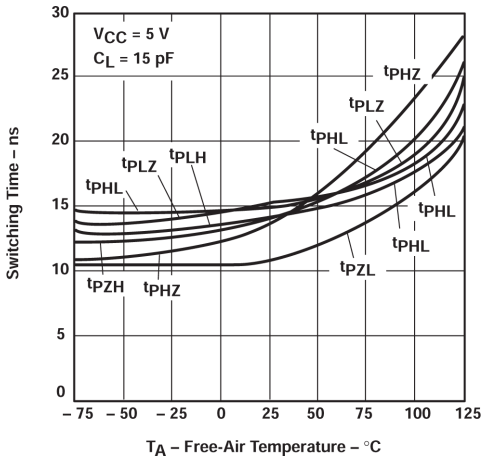


Figure 5-18. Switching Time vs Free-air Temperature

5.7 Typical Characteristics (continued)

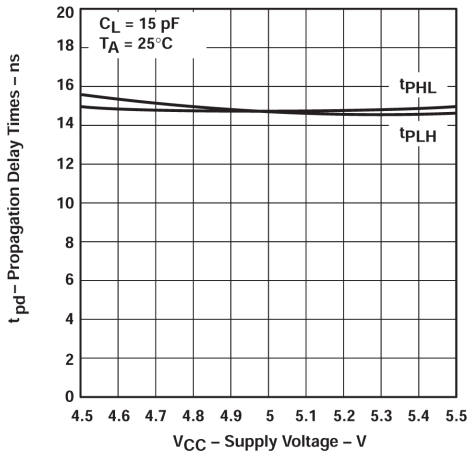


Figure 5-19. Propagation Delay Time vs Supply Voltage

6 Parameter Measurement Information

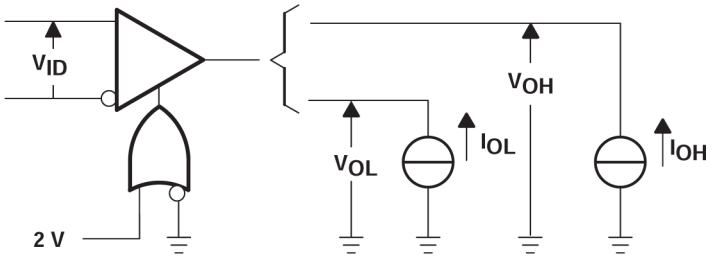
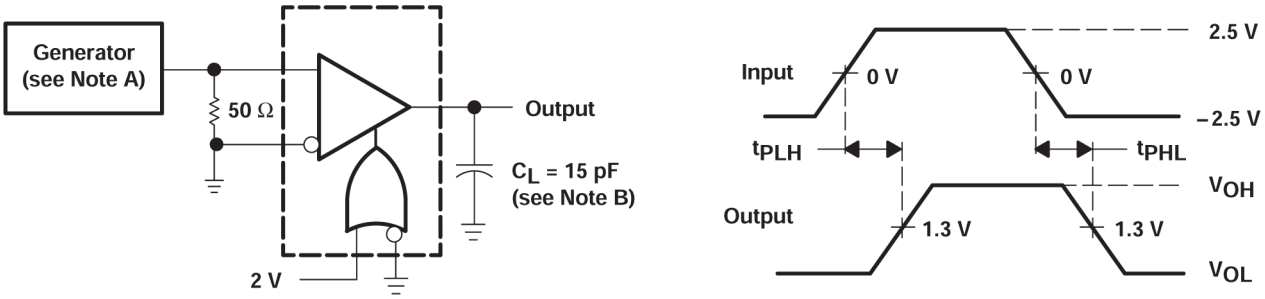


Figure 6-1. V_{OH}, V_{OL}

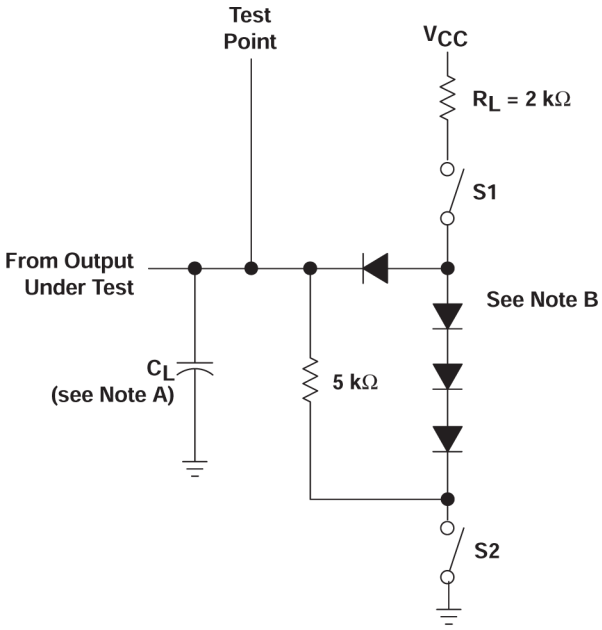


TEST CIRCUIT VOLTAGE WAVEFORMS

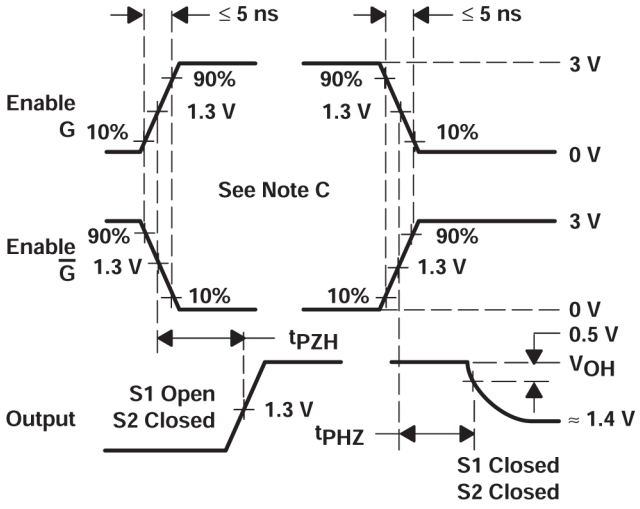
A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, Z_O = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns.

B. C_L includes probe and jig capacitance.

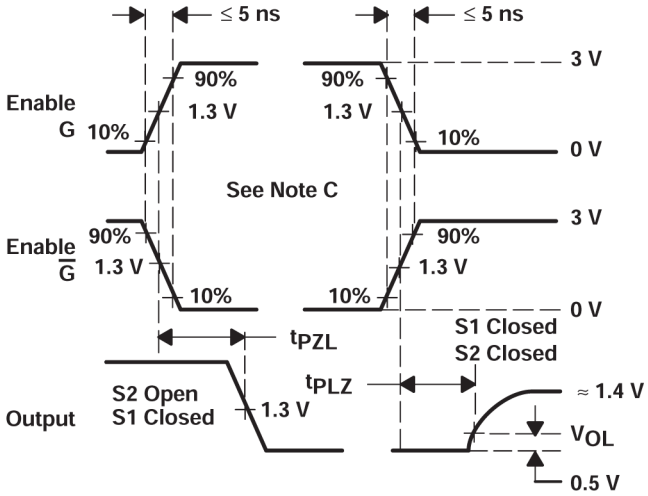
Figure 6-2. Test Circuit and Voltage Waveforms



LOAD CIRCUIT



VOLTAGE WAVEFORMS FOR t_{PHZ}, t_{PZH}



VOLTAGE WAVEFORMS FOR t_{PLZ}, t_{PZL}

A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Enable G is tested with $\overline{G}$ high; $\overline{G}$ is tested with G low.

Figure 6-3. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Device Functional Modes

Table 7-1. Function Table (Each Receiver)

DIFFERENTIAL INPUTS A – B[1]	ENABLES		OUTPUT Y
	G	$\overline{G}$	
$V_{ID} \geq 0.2$ V	H	X	H
	X	L	H
–0.2 $V_{ID} < V_{ID} < 0.2$ V	H	X	?
	X	L	?
$V_{ID} \leq -0.2$ V	H	X	L
	X	L	L
X	L	H	Z
Open	H	X	H
	X	L	H

(1) H = high level, L = low level, X = irrelevant, ? = indeterminate, Z = high impedance (off)

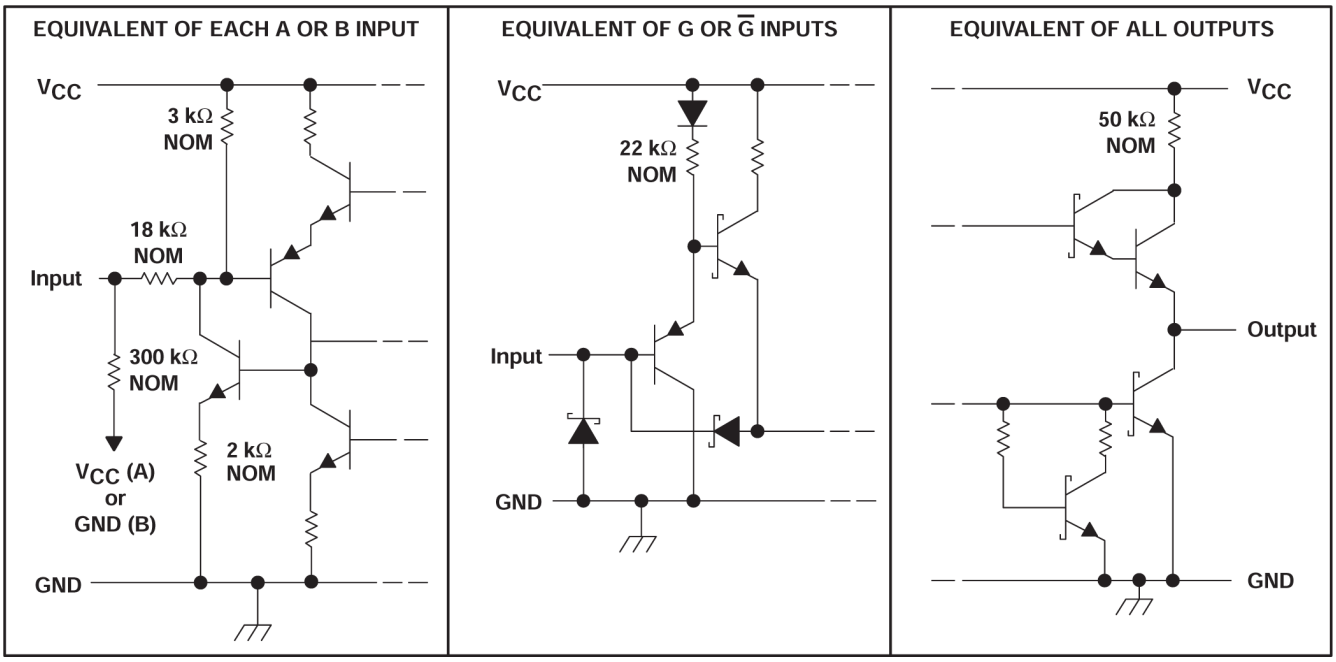


Figure 7-1. Schematics of Inputs and Outputs

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (May 1995) to Revision E (October 2023)	Page
• Changed the numbering format for tables, figures, and cross-references throughout the document	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75ALS193D	LIFEBUY	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS193	
SN75ALS193DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS193	Samples
SN75ALS193N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	(SN75ALS193N, SN7A LS193N)	Samples
SN75ALS193NE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	(SN75ALS193N, SN7A LS193N)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

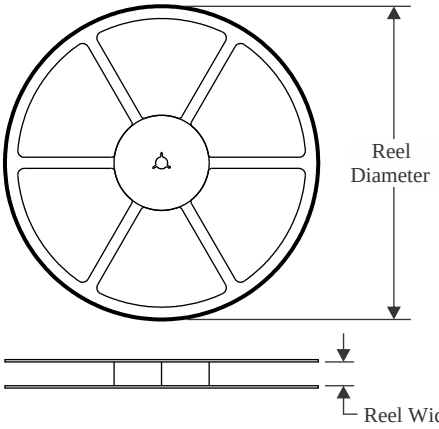
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

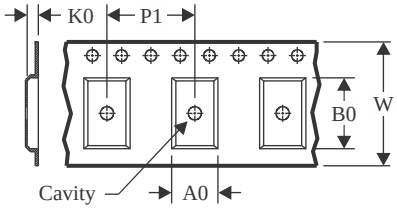
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

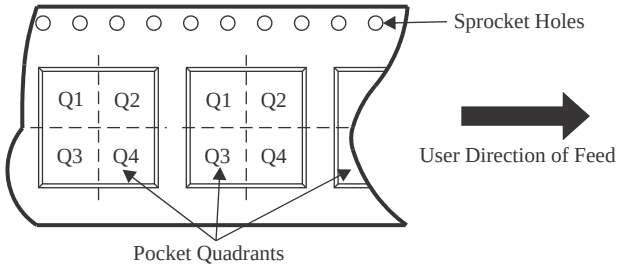


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

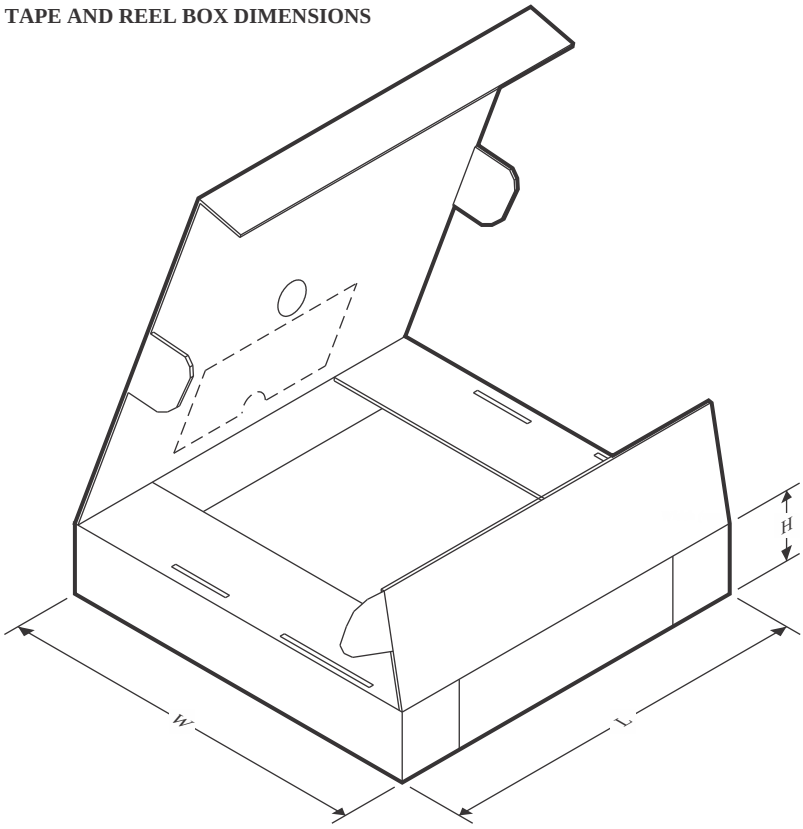
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75ALS193DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

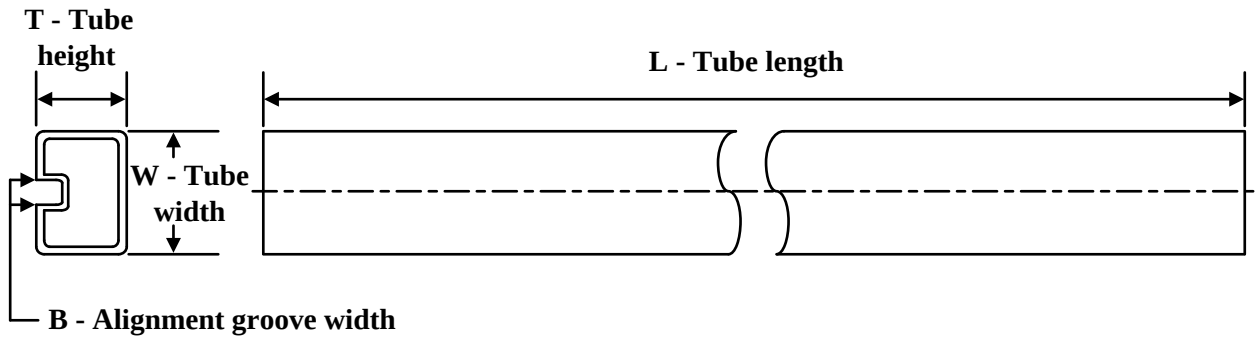
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75ALS193DR	SOIC	D	16	2500	353.0	353.0	32.0

TUBE



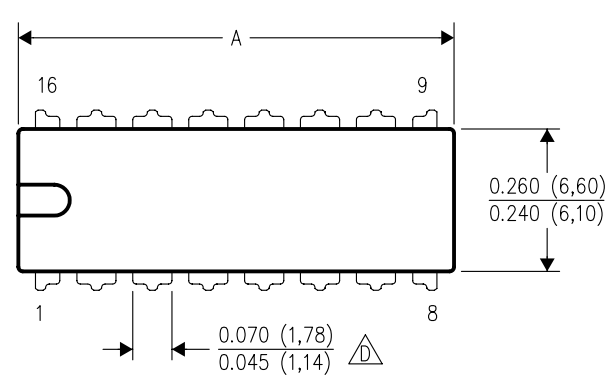
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN75ALS193D	D	SOIC	16	40	507	8	3940	4.32
SN75ALS193N	N	PDIP	16	25	506	13.97	11230	4.32
SN75ALS193N	N	PDIP	16	25	506	13.97	11230	4.32
SN75ALS193NE4	N	PDIP	16	25	506	13.97	11230	4.32
SN75ALS193NE4	N	PDIP	16	25	506	13.97	11230	4.32

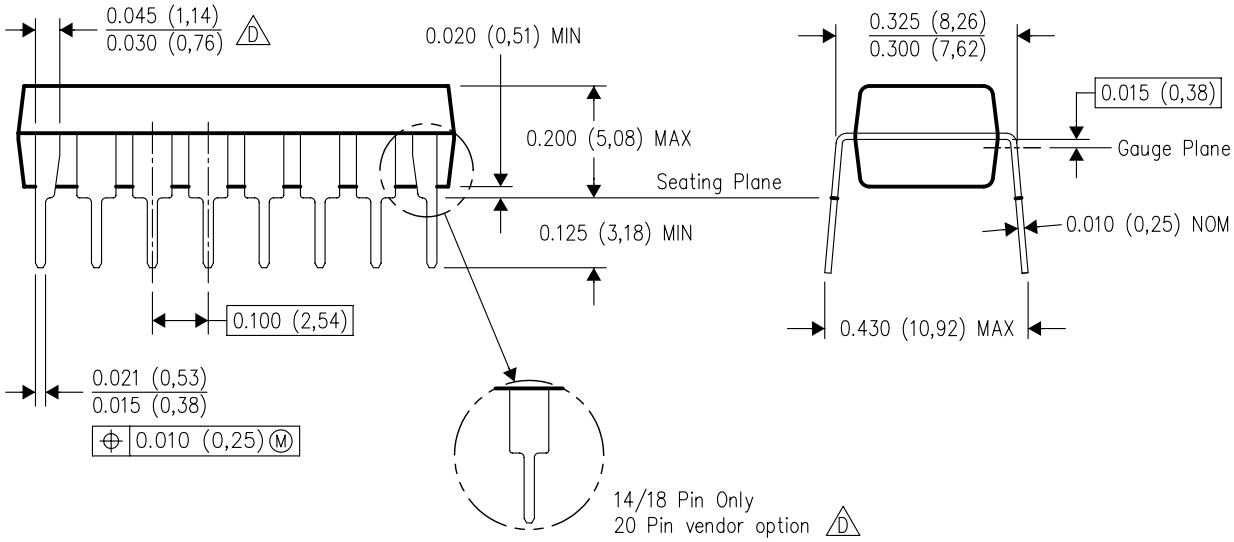
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



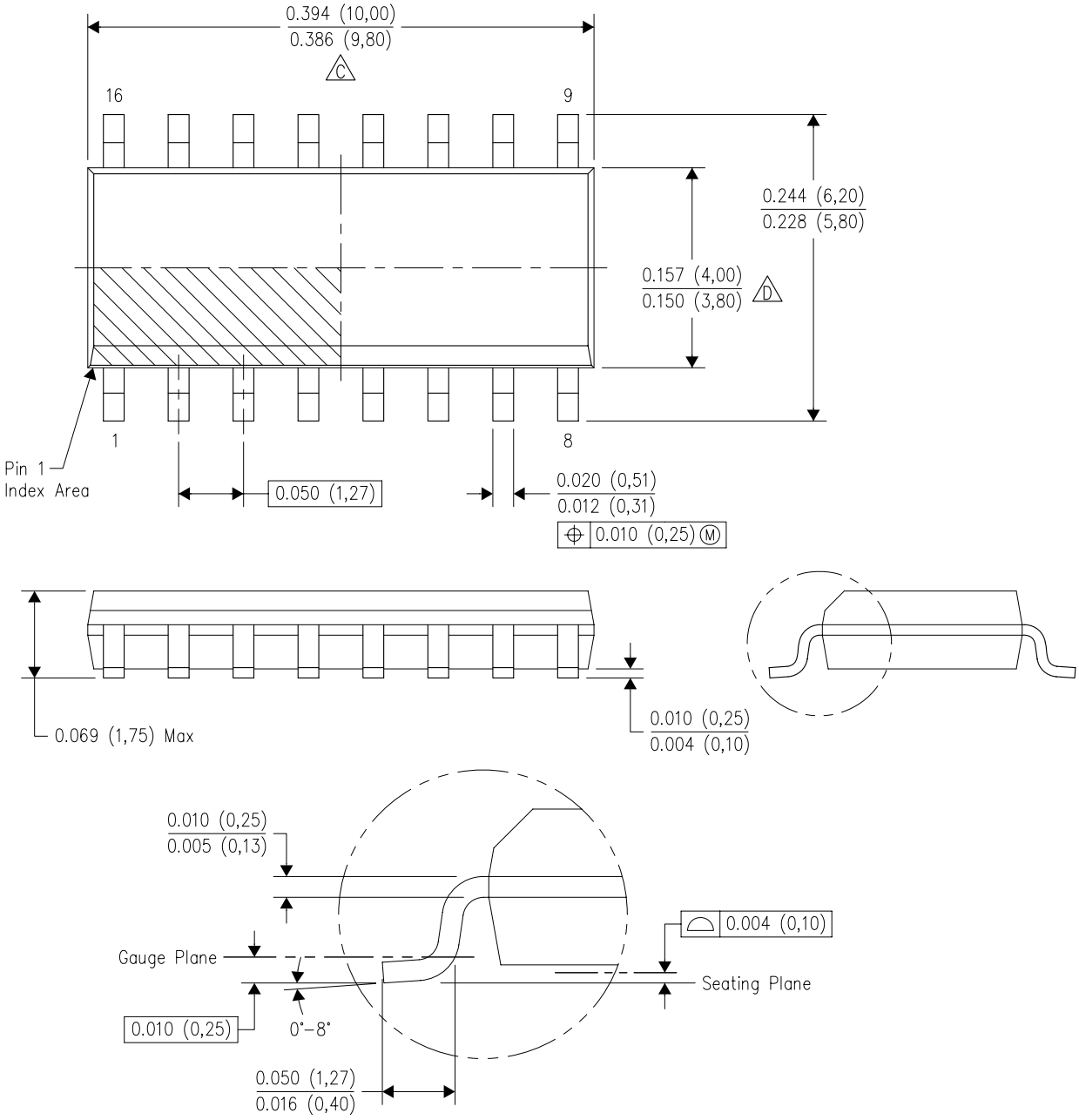
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

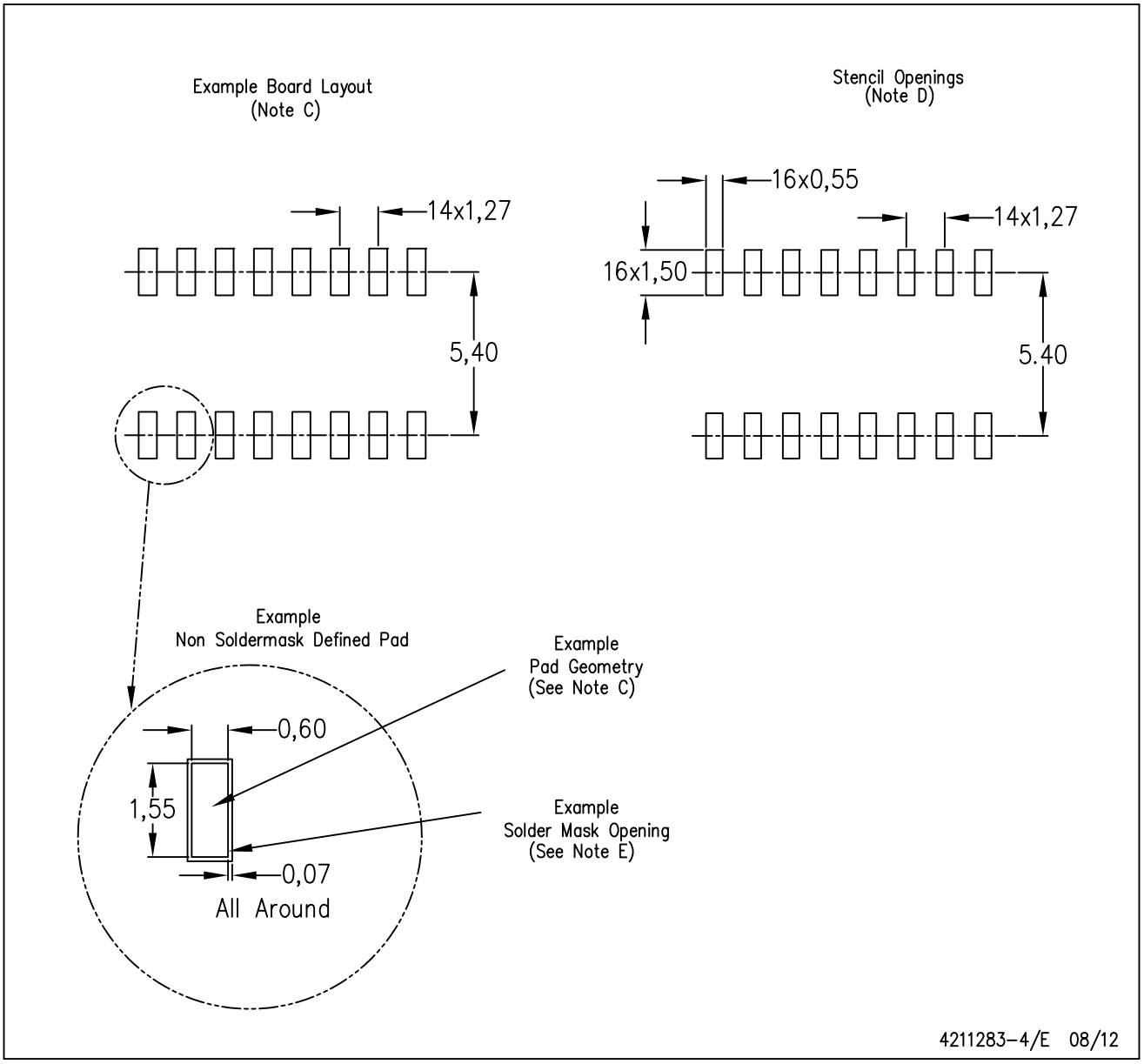
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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