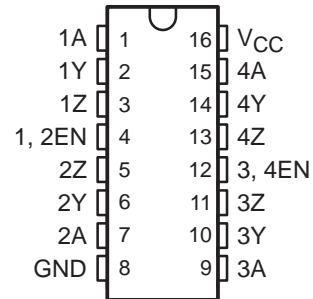


# SN55ALS194, SN75ALS194 QUADRUPLE DIFFERENTIAL LINE DRIVERS

SLLS009D – OCTOBER 1985 – REVISED MAY 1995

- Meet or Exceed the Requirements of ANSI Standard EIA/TIA-422-B and ITU Recommendation V.11
- Designed to Operate Up to 20 Mbaud
- 3-State TTL-Compatible Outputs
- Single 5-V Supply Operation
- High Output Impedance in Power-Off Condition
- Two Pairs of Drivers, Independently Enabled
- Designed as Improved Replacements for the MC3487

SN55ALS194 . . . J OR W PACKAGE  
SN75ALS194 . . . D OR N PACKAGE  
(TOP VIEW)



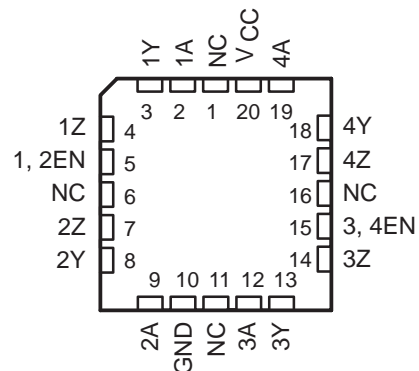
## description

These four differential line drivers are designed for data transmission over twisted-pair or parallel-wire transmission lines. They meet the requirements of ANSI Standard EIA/TIA-422-B and ITU Recommendation V.11 and are compatible with 3-state TTL circuits. Advanced low-power Schottky technology provides high speed without the usual power penalty. Standby supply current is typically only 26 mA. Typical propagation delay time is less than 10 ns, and enable/disable times are typically less than 16 ns.

High-impedance inputs keep input currents low: less than 1  $\mu$ A for a high level and less than 100  $\mu$ A for a low level. The driver circuits can be enabled in pairs by separate active-high enable inputs. The SN55ALS194 and SN75ALS194 are capable of data rates in excess of 20 megabits per second and are designed to operate with the SN55ALS195 and SN75ALS195 quadruple line receivers.

The SN55ALS194 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN75ALS194 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN55ALS194 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE  
(each driver)

INPUTS A	OUTPUT EN	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

H = high level, L = low level, X = irrelevant,  
Z = high impedance



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

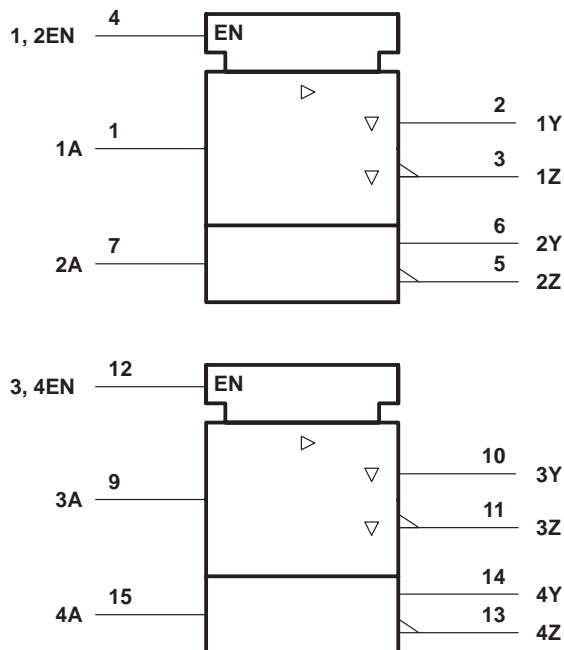
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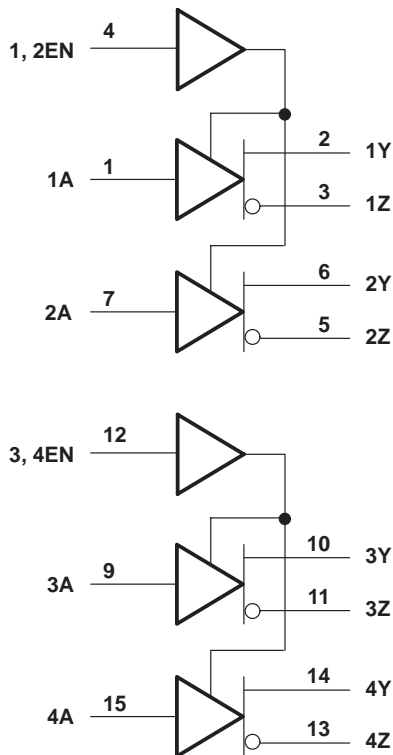
# SN55ALS194, SN75ALS194 QUADRUPLE DIFFERENTIAL LINE DRIVERS

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## logic symbol†



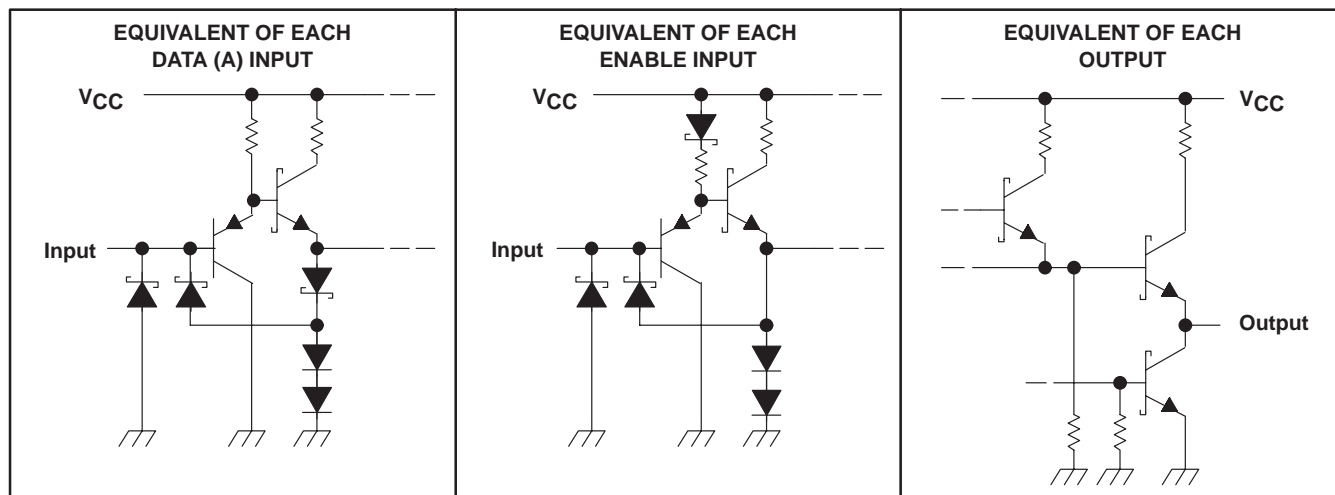
## logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the D, J, N, and W packages.

## schematics of inputs and outputs



# SN55ALS194, SN75ALS194 QUADRUPLE DIFFERENTIAL LINE DRIVERS

SLLS009D – OCTOBER 1985 – REVISED MAY 1995

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage, $V_I$	5.5 V
Output voltage, $V_O$	7 V
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, $T_A$ : SN55ALS194	– 55°C to 125°C
SN75ALS194	0°C to 70°C
Storage temperature range, $T_{stg}$	– 65°C to 150°C
Case temperature for 60 seconds, $T_C$ : FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or W package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal

**DISSIPATION RATING TABLE**

PACKAGE	$T_A \leq 25^\circ\text{C}$	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$	$T_A = 125^\circ\text{C}$
	POWER RATING		POWER RATING	POWER RATING
D	950 mW	7.6 mW/°C	608 mW	N/A
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	N/A
W	1000 mW	8.0 mW/°C	640 mW	200 mW

## recommended operating conditions‡

	SN55ALS194			SN75ALS194			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level input voltage, $V_{IH}$	All inputs, $T_A = 25^\circ\text{C}$		2	2		V	
	A inputs, $T_A = \text{Full range}$		2	2			
	EN inputs, $T_A = \text{Full range}$		2.1	2			
Low-level input voltage, $V_{IL}$			0.8	0.8		V	
High-level output current, $I_{OH}$			– 20	– 20		mA	
Low-level output current, $I_{OL}$	$T_A = 25^\circ\text{C}$		48	48		mA	
	$T_A = \text{Full range}$		20	48			
Operating free-air temperature, $T_A$	– 55		125	0		70	°C

‡ Full range is  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$  for SN55ALS194 and  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$  for SN75ALS194.

# SN55ALS194, SN75ALS194 QUADRUPLE DIFFERENTIAL LINE DRIVERS

SLLS009D – OCTOBER 1985 – REVISED MAY 1995

**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN,	I <sub>I</sub> = -18 mA			-1.5	V
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = MIN, I <sub>OH</sub> = -20 mA	SN55ALS194	2.4			V
			SN75ALS194	2.5			
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN,	I <sub>OL</sub> = MAX			0.5	V
V <sub>O</sub>	Output voltage	I <sub>O</sub> = 0		0		6	V
V <sub>OD1</sub>	Differential output voltage	I <sub>O</sub> = 0		1.5		6	V
V <sub>OD2</sub>	Differential output voltage	R <sub>L</sub> = 100 Ω, See Figure 1		1/2 V <sub>OD1</sub> or 2§			V
Δ V <sub>OD</sub>	Change in magnitude of differential output voltage¶					±0.4	V
V <sub>OC</sub>	Common-mode output voltage					±3	V
Δ V <sub>OC</sub>	Change in magnitude of common-mode output voltage¶					±0.4	V
I <sub>O</sub>	Output current with power off	V <sub>CC</sub> = 0	V <sub>O</sub> = 6 V			100	μA
			V <sub>O</sub> = -0.25 V			-100	
I <sub>OZ</sub>	High-impedance-state output current	V <sub>CC</sub> = MAX, Output enables at 0.8 V	V <sub>O</sub> = 2.7 V			100	μA
			V <sub>O</sub> = 0.5 V			-100	
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 5.5 V			100	μA
I <sub>IH</sub>	High-level input current	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 2.7 V			50	μA
I <sub>IL</sub>	Low-level input current	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 0.5 V			-200	μA
I <sub>OS</sub>	Short-circuit output current#	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 2 V	-40		-140	mA
I <sub>CC</sub>	Supply current (all drivers)	V <sub>CC</sub> = MAX,	All outputs disabled		26	45	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ The minimum V<sub>OD2</sub> with a 100-Ω load is either 1/2 V<sub>OD1</sub> or 2 V, whichever is greater.

¶ Δ|V<sub>OD</sub>| and Δ|V<sub>OC</sub>| are the changes in magnitude of V<sub>OD</sub> and V<sub>OC</sub>, respectively, that occur when the input is changed from a high level to a low level.

# Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

## switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	SN55ALS194			SN75ALS194			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
t <sub>PLH</sub>	Propagation delay time, low- to high-level output		6	13		6	13	ns
t <sub>PHL</sub>	Propagation delay time, high- to low-level output		9	14		9	14	ns
	Output-to-output skew		3.5	6		3.5	6	ns
t <sub>t(OD)</sub>	Differential output transition time		8	14		8	14	ns
t <sub>PZH</sub>	Output enable time to high level		9	12		9	12	ns
t <sub>PZL</sub>	Output enable time to low level		12	20		12	20	ns
t <sub>PHZ</sub>	Output disable time from high level		9	15		9	14	ns
t <sub>PLZ</sub>	Output disable time from low level		12	15		12	15	ns



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# SN55ALS194, SN75ALS194 QUADRUPLE DIFFERENTIAL LINE DRIVERS

SLLS009D – OCTOBER 1985 – REVISED MAY 1995

## SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	EIA/TIA-422-B
$V_O$	$V_{oa}, V_{ob}$
$ V_{OD1} $	$V_o$
$ V_{OD2} $	$V_t (R_L = 100 \Omega)$
$\Delta  V_{OD} $	$  V_t  -  \bar{V}_t  $
$V_{OC}$	$ V_{os} $
$\Delta  V_{OC} $	$ V_{os} - \bar{V}_{os} $
$I_{OS}$	$ I_{sa} ,  I_{sb} $
$I_O$	$ I_{xa} ,  I_{xb} $

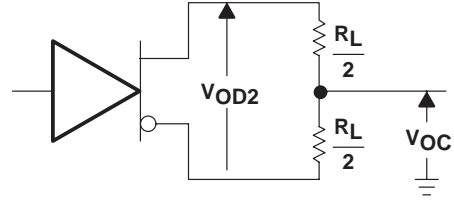
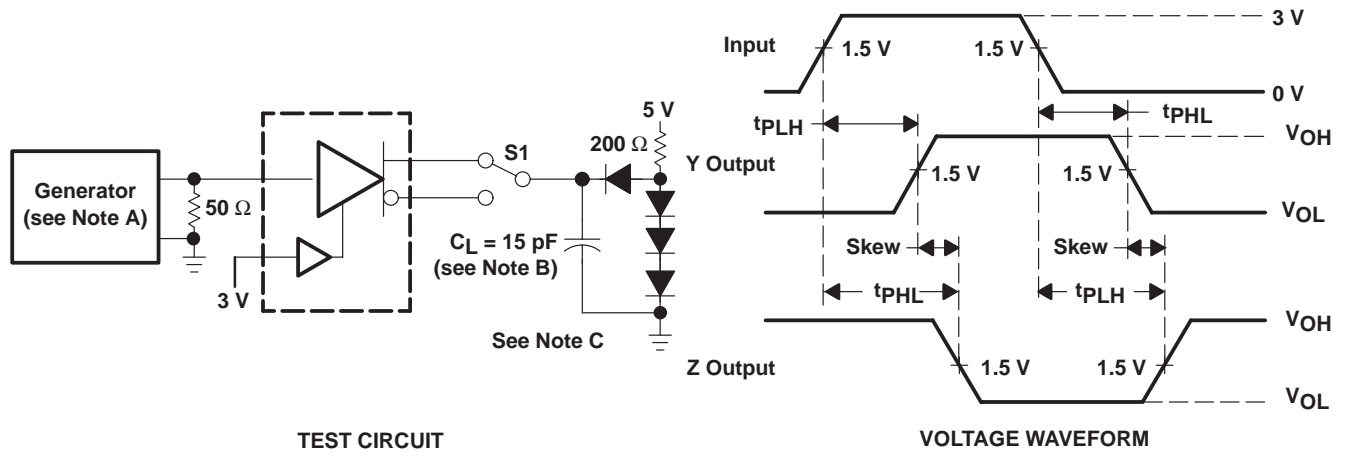


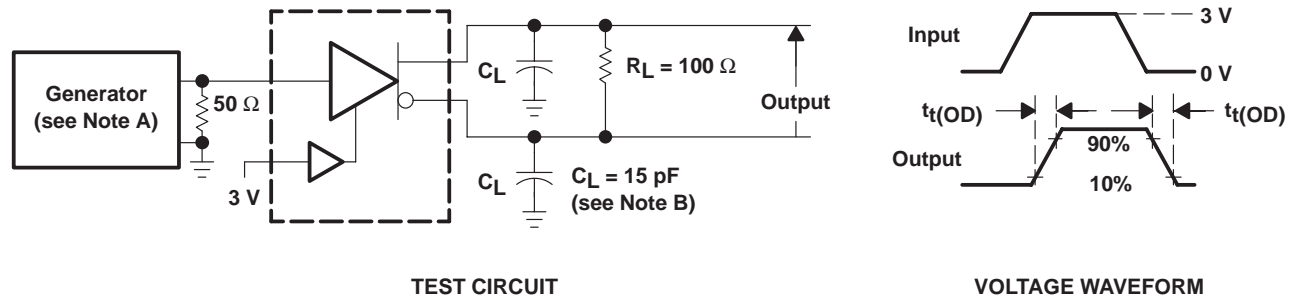
Figure 1. Driver  $V_{OD}$  and  $V_{OC}$

## PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The input pulse is supplied by a generator having the following characteristics:  $t_r \leq 5$  ns,  $t_f \leq 5$  ns,  $PRR \leq 1$  MHz, duty cycle  $\leq 50\%$ ,  $Z_O \approx 50 \Omega$ .  
 B.  $C_L$  includes probe and stray capacitance.  
 C. All diodes are 1N916 or 1N3064.

Figure 2. Test Circuit and Voltage Waveform



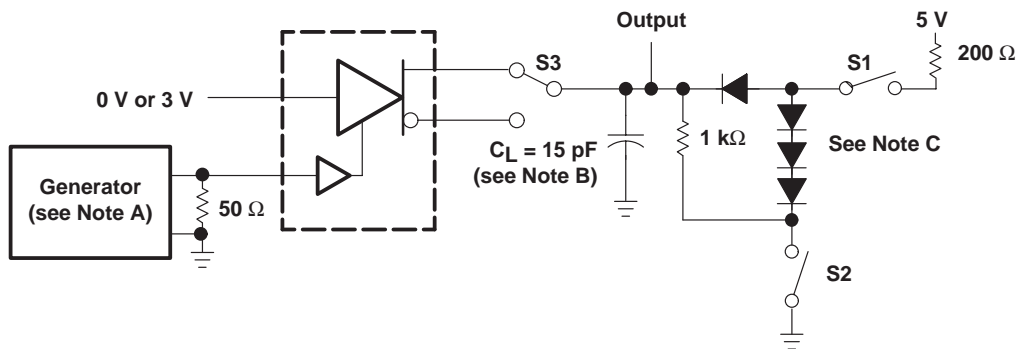
- NOTES: A. The input pulse is supplied by a generator having the following characteristics:  $t_r \leq 5$  ns,  $t_f \leq 5$  ns,  $PRR \leq 1$  MHz, duty cycle  $\leq 50\%$ ,  $Z_O \approx 50 \Omega$ .  
 B.  $C_L$  includes probe and stray capacitance.

Figure 3. Differential-Output Test Circuit and Voltage Waveform

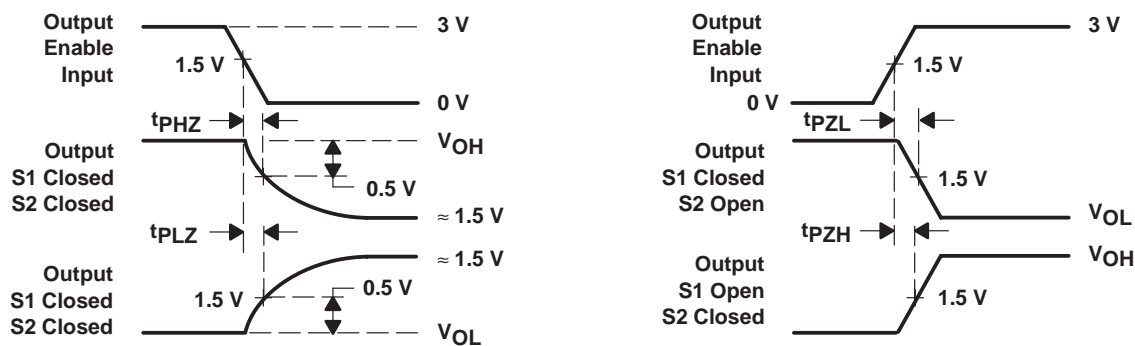
# SN55ALS194, SN75ALS194 QUADRUPLE DIFFERENTIAL LINE DRIVERS

SLLS009D – OCTOBER 1985 – REVISED MAY 1995

## PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

- NOTES: A. The input pulse is supplied by a generator having the following characteristics:  $t_r \leq 5 \text{ ns}$ ,  $t_f \leq 5 \text{ ns}$ ,  $\text{PRR} \leq 1 \text{ MHz}$ , duty cycle  $\leq 50\%$ ,  $Z_0 \approx 50 \Omega$ .  
 B.  $C_L$  includes probe and stray capacitance.  
 C. All diodes are 1N916 or 1N3064.

Figure 4. Driver Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS†

Y OUTPUT VOLTAGE  
 vs  
 DATA INPUT VOLTAGE

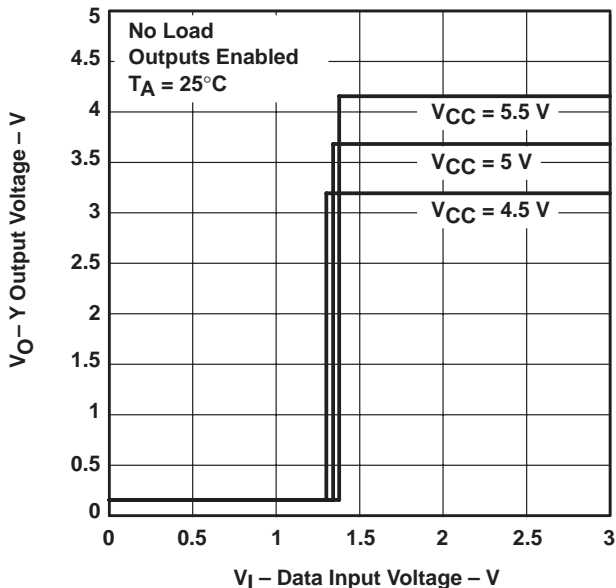


Figure 5

Y OUTPUT VOLTAGE  
 vs  
 DATA INPUT VOLTAGE

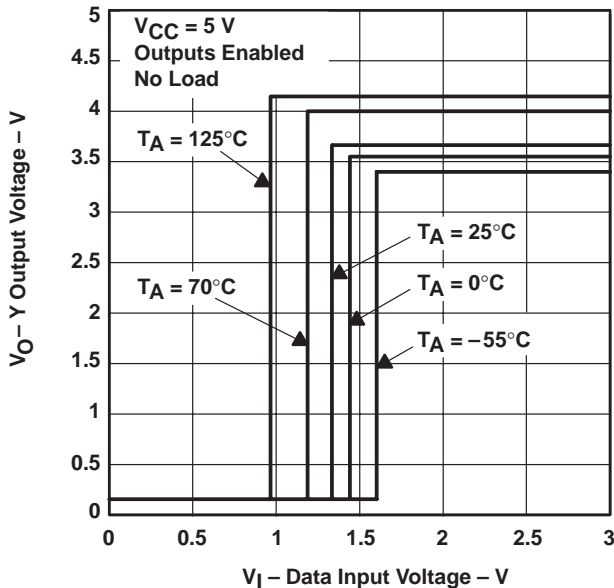


Figure 6

Y OUTPUT VOLTAGE  
 vs  
 ENABLE G INPUT VOLTAGE

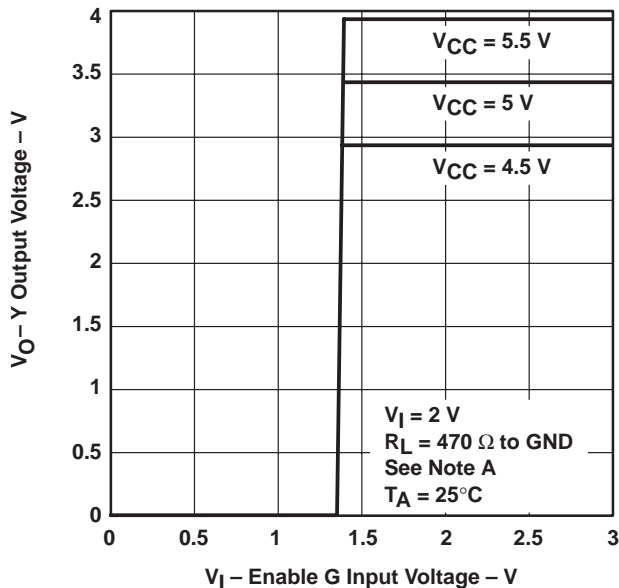


Figure 7

Y OUTPUT VOLTAGE  
 vs  
 ENABLE G INPUT VOLTAGE

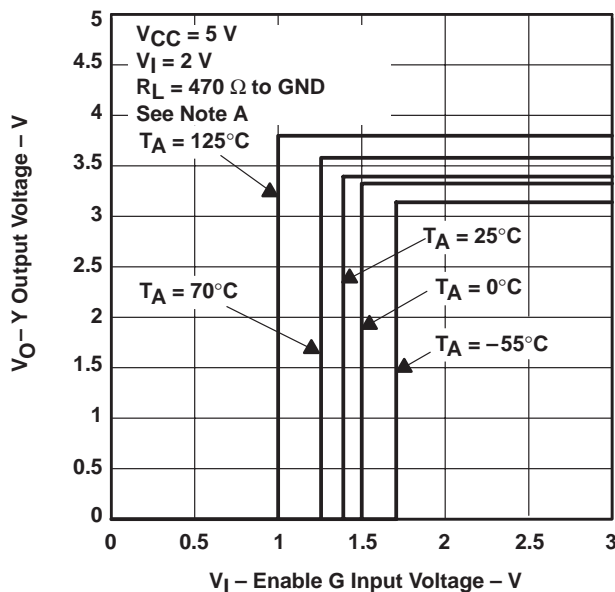


Figure 8

† Data for temperatures below 0°C and above 70°C are applicable to the SN55ALS194 circuits only.

NOTE A: The A input is connected to V<sub>CC</sub> during the testing of the Y outputs and to GND during the testing of the Z outputs.

# SN55ALS194, SN75ALS194 QUADRUPLE DIFFERENTIAL LINE DRIVERS

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## TYPICAL CHARACTERISTICS†

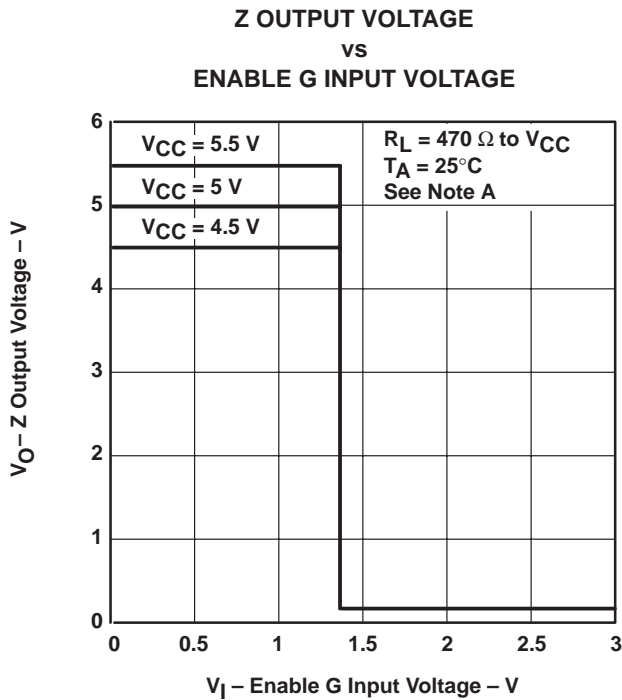


Figure 9

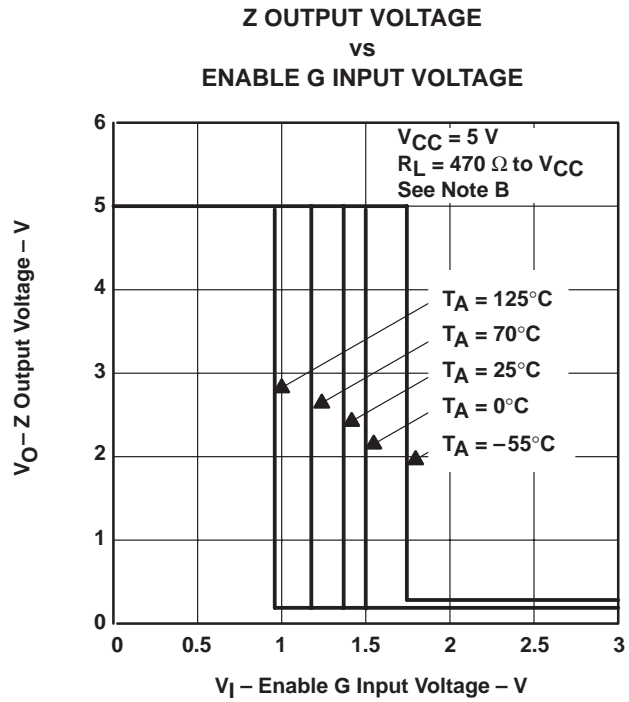


Figure 10

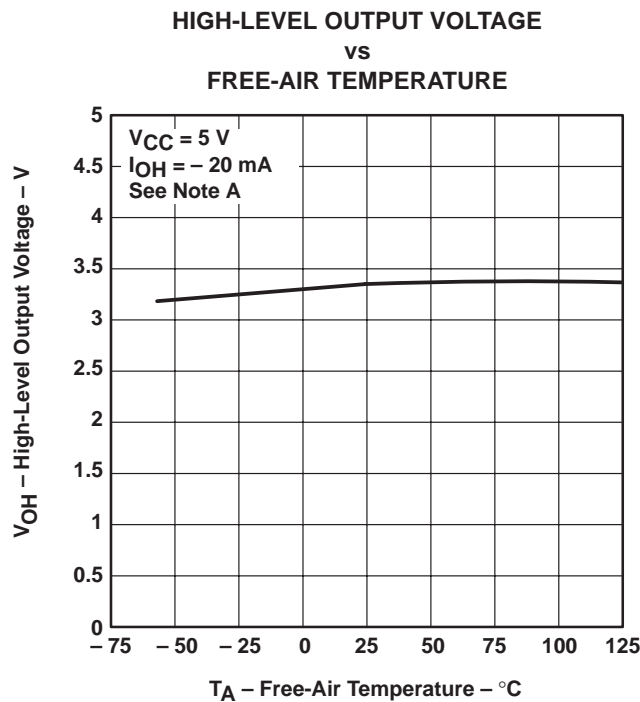


Figure 11

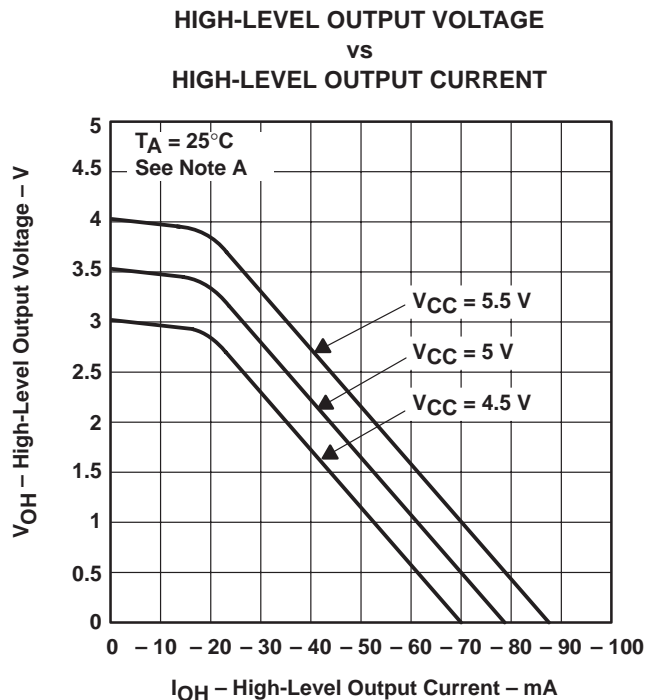


Figure 12

† Data for temperatures below  $0^\circ\text{C}$  and above  $70^\circ\text{C}$  are applicable to the SN55ALS194 circuits only.

NOTES: A. The A input is connected to  $V_{CC}$  during the testing of the Y outputs and to GND during the testing of the Z outputs.

B. The A input is connected to ground during the testing of the Y outputs and to  $V_{CC}$  during the testing of the Z outputs.



TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE  
 vs  
 FREE-AIR TEMPERATURE

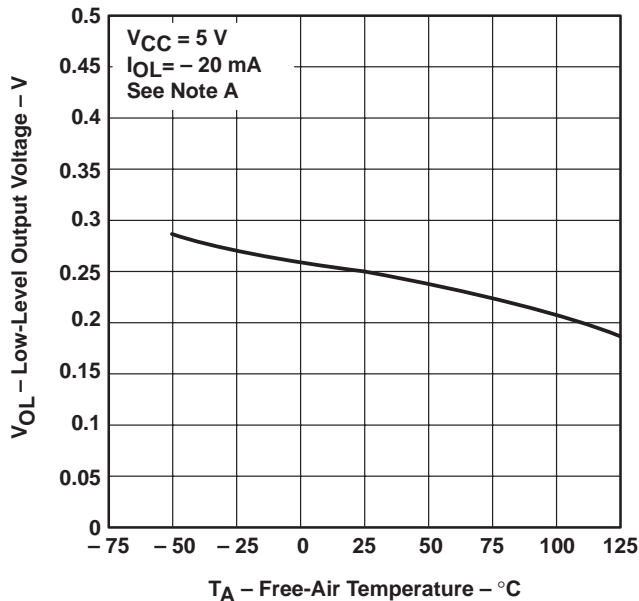


Figure 13

LOW-LEVEL OUTPUT VOLTAGE  
 vs  
 LOW-LEVEL OUTPUT CURRENT

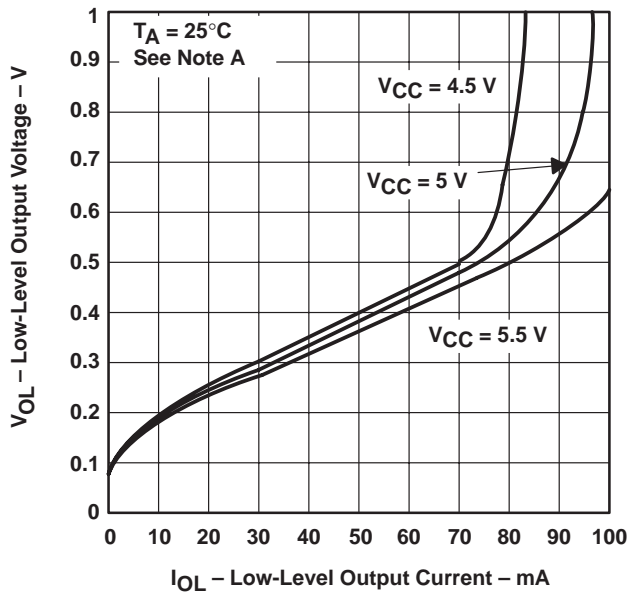


Figure 14

NOTE A: The A input is connected to GND during the testing of the Y outputs and to V<sub>CC</sub> during the testing of the Z outputs.

SUPPLY CURRENT  
 vs  
 SUPPLY VOLTAGE

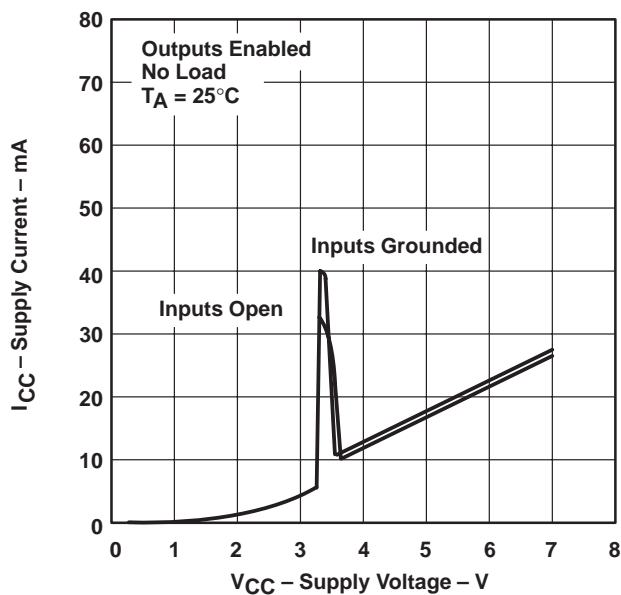


Figure 15

SUPPLY CURRENT  
 vs  
 SUPPLY VOLTAGE

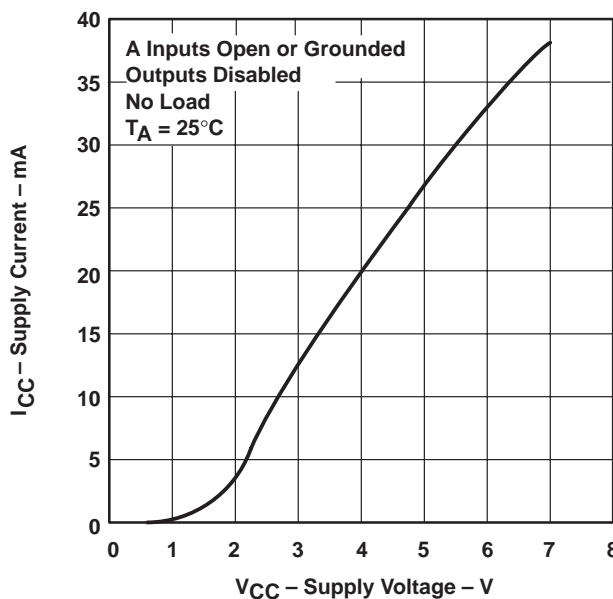


Figure 16

† Data for temperatures below 0°C and above 70°C are applicable to the SN55ALS194 circuits only.

# SN55ALS194, SN75ALS194 QUADRUPLE DIFFERENTIAL LINE DRIVERS

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## TYPICAL CHARACTERISTICS

### SUPPLY CURRENT vs FREQUENCY

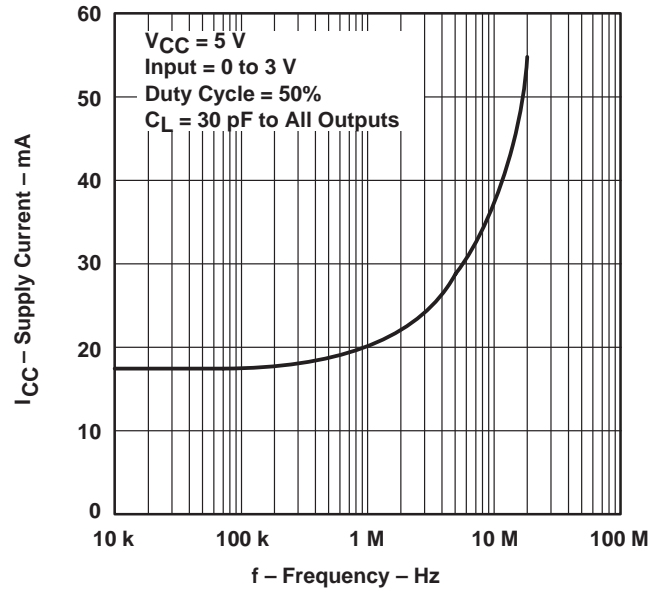


Figure 17

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75ALS194D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS194	<a href="#">Samples</a>
SN75ALS194DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS194	<a href="#">Samples</a>
SN75ALS194N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75ALS194N	<a href="#">Samples</a>
SN75ALS194NE4	ACTIVE	PDIP	N	16	25	TBD	Call TI	Call TI	0 to 70		<a href="#">Samples</a>
SN75ALS194NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS194	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75ALS194DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN75ALS194NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75ALS194DR	SOIC	D	16	2500	340.5	336.1	32.0
SN75ALS194NSR	SO	NS	16	2000	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN75ALS194D	D	SOIC	16	40	507	8	3940	4.32
SN75ALS194N	N	PDIP	16	25	506	13.97	11230	4.32



# PACKAGE OUTLINE

## NS0016A

### SOP - 2.00 mm max height

SOP



4220735/A 12/2021

#### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

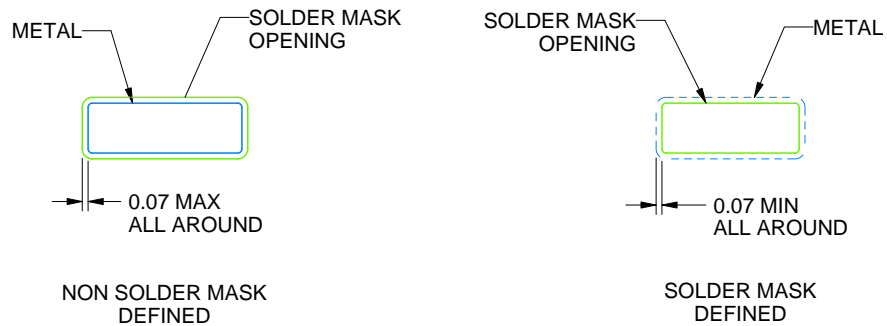


# EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220735/A 12/2021

NOTES: (continued)



7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - (C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

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