description

The SN75C188 is a monolithic, low-power, quadruple line driver that interfaces data terminal equipment with data communications equipment. This device is designed to conform to ANSI Standard EIA/TIA-232-E.

An external diode in series with each supply-voltage terminal is needed to protect the SN75C188 under certain fault conditions to comply with EIA/TIA-232-E.

The SN75C188 is characterized for operation from 0°C to 70°C.

Function Tables

**DRIVER 1**

<table>
<thead>
<tr>
<th>B</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>H</td>
<td>L</td>
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<tr>
<td>L</td>
<td>H</td>
</tr>
</tbody>
</table>

**DRIVERS 2 – 4**

<table>
<thead>
<tr>
<th>A</th>
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<th>Y</th>
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<tbody>
<tr>
<td>H</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>L</td>
<td>X</td>
<td>H</td>
</tr>
<tr>
<td>X</td>
<td>L</td>
<td>H</td>
</tr>
</tbody>
</table>

H = high level, L = low level, X = don’t care

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
logic symbol†

<table>
<thead>
<tr>
<th></th>
<th>1A</th>
<th>2A</th>
<th>3A</th>
<th>4A</th>
<th>13</th>
<th>12</th>
<th>10</th>
<th>9</th>
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<tr>
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<td></td>
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</tr>
<tr>
<td></td>
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<td>5</td>
<td>10</td>
<td>10</td>
<td></td>
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<td></td>
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<td></td>
</tr>
<tr>
<td></td>
<td>1Y</td>
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<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

schematics of inputs and outputs

†† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

positive logic

\[ Y = \overline{A} \text{ (driver 1) } \]
\[ Y = AB \text{ or } \overline{A} + B \text{ (drivers 2 through 4) } \]
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

- Supply voltage, $V_{CC+}$ (see Note 1) .................................................. $15\, \text{V}$
- Supply voltage, $V_{CC-}$ (see Note 1) .................................................. $-15\, \text{V}$
- Input voltage range, $V_I$ ................................................................. $V_{CC-}$ to $V_{CC+}$
- Output voltage range, $V_O$ ................................................................. $V_{CC-} - 6\, \text{V}$ to $V_{CC+} + 6\, \text{V}$
- Continuous total power dissipation ........................................ See Dissipation Rating Table
- Operating free-air temperature range, $T_A$ ........................................ 0°C to 70°C
- Storage temperature range, $T_{stg}$ .................................................. $-65°C$ to 150°C
- Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds ........ $260°C$

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

<table>
<thead>
<tr>
<th>PACKAGE</th>
<th>$T_{A \leq 25°C}$</th>
<th>DERATING FACTOR ABOVE $T_{A = 25°C}$</th>
<th>$T_{A = 70°C}$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>POWER RATING</td>
<td></td>
<td>POWER RATING</td>
</tr>
<tr>
<td>D</td>
<td>950 mW</td>
<td>7.6 mW/°C</td>
<td>608 mW</td>
</tr>
<tr>
<td>DB</td>
<td>525 mW</td>
<td>4.2 mW/°C</td>
<td>336 mW</td>
</tr>
<tr>
<td>N</td>
<td>1150 mW</td>
<td>9.2 mW/°C</td>
<td>736 mW</td>
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</table>

recommended operating conditions

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage, $V_{CC+}$</td>
<td>4.5</td>
<td>12</td>
<td>15</td>
<td>V</td>
</tr>
<tr>
<td>Supply voltage, $V_{CC-}$</td>
<td>-4.5</td>
<td>-12</td>
<td>-15</td>
<td>V</td>
</tr>
<tr>
<td>Input voltage, $V_I$</td>
<td>$V_{CC-}+2$</td>
<td>$V_{CC+}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>High-level Input voltage, $V_{IH}$</td>
<td>2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Low-level Input voltage, $V_{IL}$</td>
<td>0.8</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Operating free-air temperature, $T_A$</td>
<td>0</td>
<td>70</td>
<td></td>
<td>°C</td>
</tr>
</tbody>
</table>
electrical characteristics over operating free-air temperature range, \( V_{CC+} = 12 \, V \), \( V_{CC-} = -12 \, V \) (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP †</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{OH} )</td>
<td>( V_{IL} = 0.8 , V, , R_L = 3 , k\Omega ) ( V_{CC+} = 5 , V, , V_{CC-} = -5 , V ) ( V_{CC+} = 12 , V, , V_{CC-} = -12 , V )</td>
<td>4</td>
<td>10</td>
<td>10</td>
<td>V</td>
</tr>
<tr>
<td>( V_{OL} )</td>
<td>( V_{IH} = 2 , V, , R_L = 3 , k\Omega ) ( V_{CC+} = 5 , V, , V_{CC-} = -5 , V ) ( V_{CC+} = 12 , V, , V_{CC-} = -12 , V )</td>
<td>-4</td>
<td>10</td>
<td>10</td>
<td>V</td>
</tr>
<tr>
<td>( I_{IH} )</td>
<td>( V_I = 5 , V )</td>
<td>10</td>
<td>10</td>
<td>10</td>
<td>µA</td>
</tr>
<tr>
<td>( I_{IL} )</td>
<td>( V_I = 0 )</td>
<td>-10</td>
<td>-10</td>
<td>-10</td>
<td>µA</td>
</tr>
<tr>
<td>( I_{OS(H)} )</td>
<td>( V_I = 0.8 , V, , V_O = 0 , V ) ( V_{CC+} = 5 , V, , V_{CC-} = -5 , V ) ( V_{CC+} = 12 , V, , V_{CC-} = -12 , V )</td>
<td>-5.5</td>
<td>-10</td>
<td>-19.5</td>
<td>mA</td>
</tr>
<tr>
<td>( I_{OS(L)} )</td>
<td>( V_I = 2 , V, , V_O = 0 , V ) ( V_{CC+} = 5 , V, , V_{CC-} = -5 , V ) ( V_{CC+} = 12 , V, , V_{CC-} = -12 , V )</td>
<td>5.5</td>
<td>10</td>
<td>19.5</td>
<td>mA</td>
</tr>
<tr>
<td>( r_O )</td>
<td>( V_{CC+} = 0 , V, , V_{CC-} = 0 , V ) ( V_I = -2 , V ) to ( 2 , V )</td>
<td>300</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>( I_{CC+} )</td>
<td>( V_{CC+} = 5 , V, , V_{CC-} = -5 , V ) ( V_{CC+} = 12 , V, , V_{CC-} = -12 , V ) All inputs at ( 2 , V ) or ( 0.8 , V )</td>
<td>90</td>
<td>95</td>
<td>160</td>
<td>µA</td>
</tr>
<tr>
<td>( I_{CC-} )</td>
<td>( V_{CC+} = 5 , V, , V_{CC-} = -5 , V ) ( V_{CC+} = 12 , V, , V_{CC-} = -12 , V ) All inputs at ( 2 , V ) or ( 0.8 , V )</td>
<td>-90</td>
<td>-95</td>
<td>-160</td>
<td>µA</td>
</tr>
</tbody>
</table>

† All typical values are at \( T_A = 25^\circ C \).

‡ Not more than one output should be shorted at a time.

NOTE 2: The algebraic convention, in which the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only; e.g., if \(-4 \, V\) is a maximum, the typical value is a more negative voltage.

switching characteristics, \( V_{CC+} = 12 \, V \), \( V_{CC-} = -12 \, V \), \( T_A = 25^\circ C \)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP †</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{PLH} )</td>
<td>( RL = 3 , k\Omega ), ( C_L = 15 , pF ) See Figure 1</td>
<td>3</td>
<td>3.5</td>
<td>3.5</td>
<td>µs</td>
</tr>
<tr>
<td>( t_{PHL} )</td>
<td>( RL = 3 , k\Omega ), ( C_L = 15 , pF ) See Figure 1</td>
<td>0.53</td>
<td>3.2</td>
<td>3.2</td>
<td>µs</td>
</tr>
<tr>
<td>( t_{TLH} )</td>
<td>( RL = 3 , k\Omega ) to ( 7 , k\Omega ), ( C_L = 2500 , pF ) See Figure 1</td>
<td>1.5</td>
<td>6</td>
<td>15</td>
<td>µs</td>
</tr>
</tbody>
</table>

§ Measured at the 50% level

¶ Measured between the 10% and 90% points on the output waveform

# Measured between the 3-V and –3-V points on the output waveform (EIA/TIA-232-E conditions), all unused inputs tied either high or low
PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT

NOTES:  
A. The pulse generator has the following characteristics: \( t_w = 25 \, \mu s \), \( PRR = 20 \, kHz \), \( Z_O = 50 \, \Omega \), \( t_r = t_f \leq 50 \, ns \).
B. \( C_L \) includes probe and jig capacitance.

VOLTAGE WAVEFORMS

Figure 1. Test Circuit and Voltage Waveforms
TYPICAL CHARACTERISTICS

VOLTAGE TRANSFER CHARACTERISTICS

Figure 2

SHORT-CIRCUIT OUTPUT CURRENT

VS

FREE-AIR TEMPERATURE

Figure 4

OUTPUT VOLTAGE

VS

FREE-AIR TEMPERATURE

Figure 5
TYPICAL CHARACTERISTICS

INPUT CURRENT

VCC± = ±12 V

IIH, Vl = 5 V

IIIL, Vl = 0

T A – Free-Air Temperature – °C

Figure 6

POWER-OFF OUTPUT RESISTANCE

VCC+ = VCC− = 0

VO = –2 V

VO = 2 V

T A – Free-Air Temperature – °C

Figure 7

SUPPLY CURRENT

VCC± = ±12 V

VCC± = ±5 V

RL = ∞

VI = 0.8 V or 2 V

ICC +

ICC −

T A – Free-Air Temperature – °C

Figure 8

OUTPUT SLEW RATE

VCC± = ±12 V

SR = Output Slew Rate – V/s

CL = 15 pF

Slew Rate

Positive Transition

RL = 3 kΩ

RL = 7 kΩ

Slew Rate

Negative Transition

RL = 3 kΩ

RL = 7 kΩ

T A – Free-Air Temperature – °C

Figure 9
TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME

vs

FREE-AIR TEMPERATURE

Figure 10

OUTPUT TRANSITION TIME

vs

FREE-AIR TEMPERATURE

Figure 11

APPLICATION INFORMATION

Figure 12. Logic Translator Applications
NOTE A: External diodes placed in series with the $V_{CC+}$ and $V_{CC-}$ leads protect the SN75C188 in the fault condition where the device outputs are shorted to $\pm 15$ V and the power supplies are at low voltage and provide low-impedance paths to GND.

Figure 13. Power Supply Protection to Meet Power-Off Fault Conditions of Standard EIA/TIA-232-E
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>PIns</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN75C188D</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>14</td>
<td>50</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>SN75C188</td>
<td>Samples</td>
</tr>
<tr>
<td>SN75C188DBR</td>
<td>ACTIVE</td>
<td>SSOP</td>
<td>DB</td>
<td>14</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>CA188</td>
<td>Samples</td>
</tr>
<tr>
<td>SN75C188DR</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>14</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>SN75C188</td>
<td>Samples</td>
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<tr>
<td>SN75C188DRE4</td>
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<td>SOIC</td>
<td>D</td>
<td>14</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>SN75C188</td>
<td>Samples</td>
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<tr>
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<td>PDIP</td>
<td>N</td>
<td>14</td>
<td>25</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>N / A for Pkg Type</td>
<td>0 to 70</td>
<td>SN75C188</td>
<td>Samples</td>
</tr>
<tr>
<td>SN75C188NSR</td>
<td>ACTIVE</td>
<td>SO</td>
<td>NS</td>
<td>14</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>75C188</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
- **RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
- **Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
**TAPE AND REEL INFORMATION**

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width (W1 mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin 1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN75C188DR</td>
<td>SOIC</td>
<td>D</td>
<td>14</td>
<td>2500</td>
<td>330.0</td>
<td>16.4</td>
<td>6.5</td>
<td>9.0</td>
<td>2.1</td>
<td>8.0</td>
<td>16.0</td>
<td>Q1</td>
</tr>
<tr>
<td>SN75C188DR</td>
<td>SOIC</td>
<td>D</td>
<td>14</td>
<td>2500</td>
<td>330.0</td>
<td>16.4</td>
<td>6.5</td>
<td>9.0</td>
<td>2.1</td>
<td>8.0</td>
<td>16.0</td>
<td>Q1</td>
</tr>
<tr>
<td>SN75C188NSR</td>
<td>SO</td>
<td>NS</td>
<td>14</td>
<td>2000</td>
<td>330.0</td>
<td>16.4</td>
<td>8.2</td>
<td>10.5</td>
<td>2.5</td>
<td>12.0</td>
<td>16.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>

**TAPE DIMENSIONS**

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers
**TAPE AND REEL BOX DIMENSIONS**

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN75C188DR</td>
<td>SOIC</td>
<td>D</td>
<td>14</td>
<td>2500</td>
<td>333.2</td>
<td>345.9</td>
<td>28.6</td>
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<tr>
<td>SN75C188DR</td>
<td>SOIC</td>
<td>D</td>
<td>14</td>
<td>2500</td>
<td>367.0</td>
<td>367.0</td>
<td>38.0</td>
</tr>
<tr>
<td>SN75C188NSR</td>
<td>SO</td>
<td>NS</td>
<td>14</td>
<td>2000</td>
<td>367.0</td>
<td>367.0</td>
<td>38.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
N (R-PDIP-T**)

16 PINS SHOWN

<table>
<thead>
<tr>
<th>PINS **</th>
<th>14</th>
<th>16</th>
<th>18</th>
<th>20</th>
</tr>
</thead>
<tbody>
<tr>
<td>A MAX</td>
<td>0.775 (19.69)</td>
<td>0.775 (19.69)</td>
<td>0.920 (23.37)</td>
<td>1.060 (26.92)</td>
</tr>
<tr>
<td>A MIN</td>
<td>0.745 (18.92)</td>
<td>0.745 (18.92)</td>
<td>0.850 (21.59)</td>
<td>0.940 (23.88)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>VARIATION</th>
<th>AA</th>
<th>BB</th>
<th>AC</th>
<th>AD</th>
</tr>
</thead>
</table>

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
   
   Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
   
   The 20 pin end lead shoulder width is a vendor option, either half or full width.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.15.
D. Falls within JEDEC MO-150
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.15.
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