TCA39416 Ultra-Low-Voltage I3C Translator with Rise Time Accelerators

1 Features

- 2-bit dual supply bidirectional translator for I3C, I^2C, SMBus, SPI applications
- Provides bidirectional voltage translation with no direction pin
- High-impedance output Ax and Bx pins when OE = 0 V or V_{CC} = 0 V
- Internal 10-kΩ pull-up resistor on Ax and Bx pins
- 0.72 V to 1.98 V on both A and B ports; $V_{CCA} \leq V_{CCB}$
- Compatible with MIPI I3C supporting speeds up to 12.5 MHz
- Compatible with JEDEC I3C module sideband bus specification (JESD403)
- V_{CC} Isolation feature: If either V_{CC} input is at GND, both A and B ports are in the high-impedance state
- No power-supply sequencing required: either V_{CCA} or V_{CCB} can be ramped first
- Low I_{off} of 2.5 µA when either V_{CCA} or V_{CCB} = 0 V
- OE input can be tied directly to V_{CCA} or controlled by GPIO
- Latch-up performance exceeds 100 mA per JESD 78, class II
- ESD Protection exceeds JESD 22
  - 4000-V Human-body model (A114-B)
  - 1500-V Charged-device model (C101)

2 Applications

- Servers
- Wearables
- Personal electronics

3 Description

The TCA39416 is a 2-bit bidirectional MIPI I3C v1.1.1, I^2C, SMBus and SPI voltage-level translator with an output enable (OE) input and rising and falling edge accelerators. It is operational from 0.72 V to 1.98 V on both the A-side and B-side with V_{CCA} must be less than V_{CCB} for proper operation. This limitation allows the device to interface between lower and higher logic signal levels at any of the typical 1-V, 1.2-V and 1.8-V supply rails.

The OE input pin is referenced to V_{CCA}, can be tied directly to V_{CCA}, but it is also 1.98-V tolerant. The OE pin can also be controlled and set to a logic low to place all the Ax (A1, A2) and Bx (B1, B2) pins in a high-impedance state, which significantly reduces the quiescent current consumption.

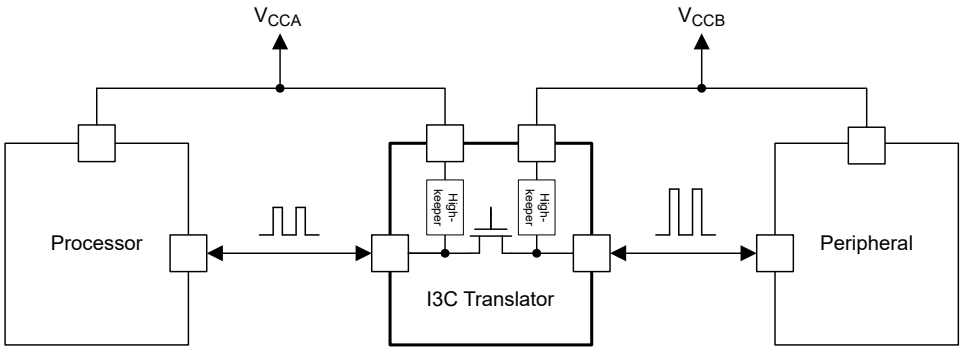
The TCA39416 is compatible with 12.5 MHz I3C speeds and also supports higher speed SPI applications with two devices. It also enables bidirectional voltage level translation for traditional I2C-bus/SMBus applications under normal I^2C and SMBus configurations.

The TCA39416 features internal 10-kΩ pull-up resistors on Ax and Bx that act as high-keeper and are enabled based on respective V_{CC} voltage when bus is high.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TCA39416	X2SON (8)	1 mm × 1.35 mm
	SOT-23-T (8)	2.9 mm × 2.8 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Application

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4 Pin Configuration and Functions

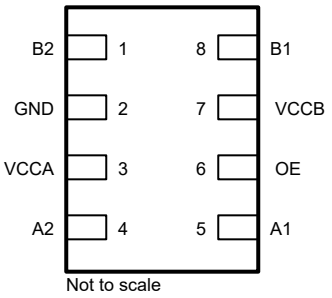


Figure 4-1. 8-PIN DTW (Top View)

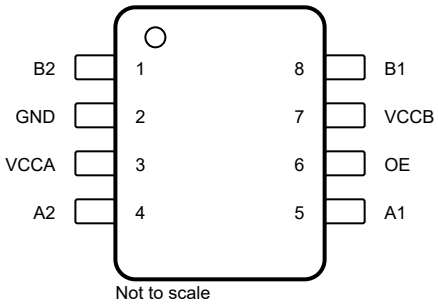


Figure 4-2. 8-PIN DDF (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
	DTW, DDF		
B2	1	I/O	Input and output B. Referenced to V_{CCB}.
B1	8	I/O	Input and output B. Referenced to V_{CCB}.
GND	2	GND	Ground.
VCCA	3	Power	A-port supply voltage. 0.72 V ≤ V_{CCA} ≤ 1.98 V.
A1	5	I/O	Input and output A. Referenced to V_{CCA}.
A2	4	I/O	Input and output A. Referenced to V_{CCA}.
OE	6	I	Output enable (active High). Pull OE low to place all outputs in 3-state mode. Referenced to V_{CCA}.
VCCB	7	Power	B-port supply voltage. 0.72 V ≤ V_{CCB} ≤ 1.98 V.

5 Specifications

5.1 Absolute Maximum Ratings

over recommended operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage range		–0.5	2.5	V
V_{CCB}	Supply voltage range		–0.5	2.5	V
V_I	Input voltage range(2)	A port	–0.5	2.5	V
		B port	–0.5	2.5	
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)	A port	–0.5	2.5	V
		B port	–0.5	2.5	
V_O	Voltage range applied to any output in the high or low state(2) (3)	A port	–0.5	2.5	V
		B port	–0.5	2.5	
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA}, V_{CCB}, or GND			±100	mA
T_{stg}	Storage temperature		–65	150	°C
P_{tot}	Total power dissipation			100	mW

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CCA} and V_{CCB} are provided in the recommended operating conditions table.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)

			V_{CCA}	V_{CCB}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				0.72	1.98	V
V_{CCB}	Supply voltage				0.72	1.98	V
V_I	Input voltage	A-port I/Os, B-port I/Os, OE	0 V to 1.98 V	0 V to 1.98 V	0	1.98	V
V_{IH}	High-level input voltage	OE input	0.72 V to 1.98 V	0.72 V to 1.98 V	V_{CCA} × 0.65	1.98	V
V_{IL}	Low-level input voltage	OE input	0.72 V to 1.98 V	0.72 V to 1.98 V	0	V_{CCA} × 0.35	V
Δt/ΔV	Input transition rise and fall rate		0.72 V to 1.98 V	0.72 V to 1.98 V		5	ns/V
T_A	Operating free-air temperature				–40	125	°C

5.4 Thermal Information

THERMAL METRIC(1)		TCA39416 DDF (SOT-23) 8 PINS	TCA39416 DTW (X2SON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	220.8	261.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	132.4	128.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	138.3	146.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	24.2	8.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	137.2	146.1	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)[1] [2] [3]

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	TYP	MAX	UNIT
V_{UVLO_RISE}	UVLO Rising Threshold	V_{UVLO} for V_{CCA} and V_{CCB} are independent	0 V to 1.98 V	0 V to 1.98 V	0.3	0.55	0.65	V
V_{UVLO_FALL}	UVLO Falling Threshold	V_{UVLO} for V_{CCA} and V_{CCB} are independent	0 V to 1.98 V	0 V to 1.98 V	0.25	0.5	0.6	V
V_{RTA} [4]	RTA Activation Threshold		0.72 V to 1.98 V	0.72 V to 1.98 V	V_{CCI} × 0.30	V_{CCI} × 0.45		V
V_{FTA} [4]	FTA Activation Threshold		0.72 V to 1.98 V	0.72 V to 1.98 V		V_{CCI} × 0.40	V_{CCI} × 0.70	V
R_{PU}		V_I = V_{CC} – 0.15 V	0.72 V to 1.98 V	0.72 V to 1.98 V	7.5	10	15	kΩ
I_I	OE	V_I = V_{CCA} or GND	0.72 V to 1.98 V	0.72 V to 1.98 V		±0.1	±1	µA
I_{OZ}	A or B port	OE less than V_{IL}	0.72 V to 1.98 V	0.72 V to 1.98 V		0	±2.5	µA
I_{off}	A port	V_I = 1.98 V, V_O = 0 V (T_A ≤ 85°C)	0 V	0 V to 1.98 V		±0.1	±0.5	µA
	B port	V_I = 1.98 V, V_O = 0 V (T_A ≤ 85°C)	0 V to 1.98 V	0 V		±0.1	±0.5	
	A port	V_I = 1.98 V, V_O = 0 V (T_A ≤ 125°C)	0 V	0 V to 1.98 V		±0.1	±2.5	
	B port	V_I = 1.98 V, V_O = 0 V (T_A ≤ 125°C)	0 V to 1.98 V	0 V		±0.1	±2.5	
I_{CC_OFF}	VCCA	V_I = V_O = 0 V to 1.98 V, I_O = 0, OE = 0 V	0.72 V to 1.98 V	0.72 V to 1.98 V		2.5	20	µA
	VCCB	V_I = V_O = 0 V to 1.98 V, I_O = 0, OE = 0 V				2.5	20	
I_{CCA}		V_I = V_O = 0 V or V_{CCI}, I_O = 0, OE = V_{CCA}	0.72 V	0.72 V to 1.98 V		1.5	40	µA
			1.1 V	1.1 V to 1.98 V		2	25	
			1.32 V	1.32 V to 1.98 V		3	25	
			1.98 V	1.98 V		4	28	
I_{CCB}		V_I = V_O = 0 V or V_{CCI}, I_O = 0, OE = V_{CCA}	0.72 V	0.72 V to 1.98 V		1	24	µA
			1.1 V	1.1 V to 1.98 V		1.5	26	
			1.32 V	1.32 V to 1.98 V		2	26	
			1.98 V	1.98 V		2.5	28	
I_{CCA} + I_{CCB}		V_I = V_O = 0 V or V_{CCI}, I_O = 0, OE = V_{CCA}	0.72 V	0.72 V to 1.98 V		1	46	µA
			1.1 V	1.1 V to 1.98 V		2	48	
			1.32 V	1.32 V to 1.98 V		4	48	
			1.98 V	1.98 V		6	54	

5.5 Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)[1] [2] [3]

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	TYP	MAX	UNIT
R_{on}		V_I = 0.1 V, I_O = 2 mA	1.8 V	1.8 V		8	20	Ω
		V_I = 0.1 V, I_O = 2 mA	0.8 V, 1.8 V	1.8 V, 0.8 V		10	28	
		V_I = 0.1 V, I_O = 2 mA	1.2 V, 1.8 V	1.8 V, 1.2 V		8	18	
C_I	OE		1.98 V	1.98 V		2	3	pF
C_{io}	A or B port		0 V, 1 V, 1.98 V	0 V, 1 V, 1.98 V		4	8	pF

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) V_{CCA} must be less than or equal to V_{CCB}, and V_{CCA} must not exceed 1.98 V.
(4) RTA is "rise time accelerator" and FTA is "fall time accelerator".

5.6 Timing Requirements

over operating free-air temperature range (unless otherwise noted). Typical specifications are at T_A = 25 °C unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{RTA}	Time from V_{RTA} to RTA disabling	Ax, Bx = Hi-Z EN = V_{CC}		80	210	ns
t_W	Pulse width	data inputs	35			ns

5.7 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	A	B	V_{CCA} = 0.72 V		8	20	ns
			V_{CCA} = 0.8 V		7	18	
			V_{CCA} = 1.0 V		4	13	
			V_{CCA} = 1.2 V		2	9	
			V_{CCA} = 1.8 V		1	5	
t_{PLH}	A	B	V_{CCA} = 0.72 V		8	30	ns
			V_{CCA} = 0.8 V		6	16	
			V_{CCA} = 1.0 V		3	10	
			V_{CCA} = 1.2 V		2	8	
			V_{CCA} = 1.8 V		0.5	4	
t_{PHL}	B	A	V_{CCB} = 0.72 V		9	18	ns
			V_{CCB} = 0.8 V		8	15	
			V_{CCB} = 1.0 V		8	16	
			V_{CCB} = 1.2 V		2	17	
			V_{CCB} = 1.8 V		2	18	
t_{PLH}	B	A	V_{CCB} = 0.72 V		9	35	ns
			V_{CCB} = 0.8 V		2	18	
			V_{CCB} = 1.0 V		1	16	
			V_{CCB} = 1.2 V		0.5	15	
			V_{CCB} = 1.8 V		0.5	14	
$t_{SK(O)-RISE}$	Rising Channel-to-channel skew (Propagation)					3	ns
$t_{SK(O)-FALL}$	Falling Channel-to-channel skew (Propagation)					3	ns
t_{en}	OE	A or B				250	ns
t_{dis}	OE	A or B				350	ns
t_{rA}	B-port	A-port	V_{CCA} = 0.72 V		18	42	ns
			V_{CCA} = 0.8 V		5	22	
			V_{CCA} = 1.0 V		4	15	
			V_{CCA} = 1.2 V		2	12	
			V_{CCA} = 1.8 V		1.5	9	
t_{rB}	A-port	B-port	V_{CCB} = 0.72 V		6	34	ns
			V_{CCB} = 0.8 V		4	21	
			V_{CCB} = 1.0 V		3	15	
			V_{CCB} = 1.2 V		2	13	
			V_{CCB} = 1.8 V		1.5	8	
t_{fA}	B-port	A-port	V_{CCA} = 0.72 V		4	12	ns
			V_{CCA} = 0.8 V		4	11	
			V_{CCA} = 1.0 V		3	11	
			V_{CCA} = 1.2 V		3	11	
			V_{CCA} = 1.8 V		4	12	
t_{fB}	A-port	B-port	V_{CCB} = 0.72 V		4	9	ns
			V_{CCB} = 0.8 V		4	9	
			V_{CCB} = 1.0 V		3	10	
			V_{CCB} = 1.2 V		3	11	
			V_{CCB} = 1.8 V		2	11	
f_{data}	Data rate			0.06		26	Mbps

5.8 Typical Characteristics

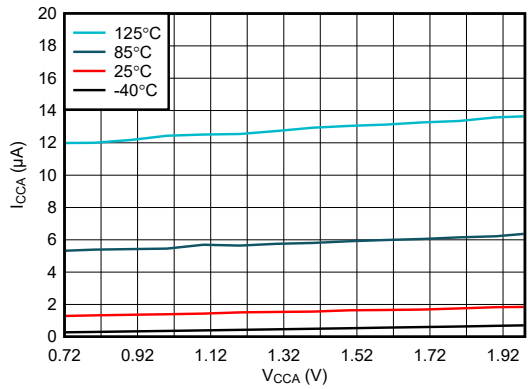


Figure 5-1. I_{CCA} (µA) vs V_{CCA} (V)

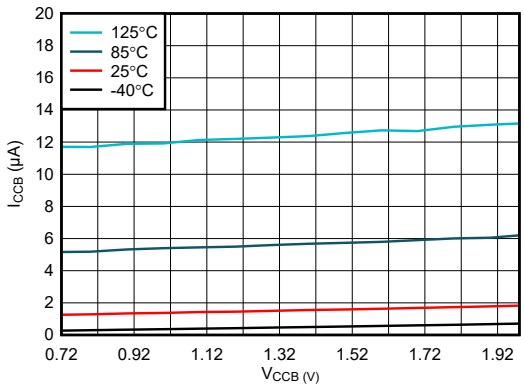
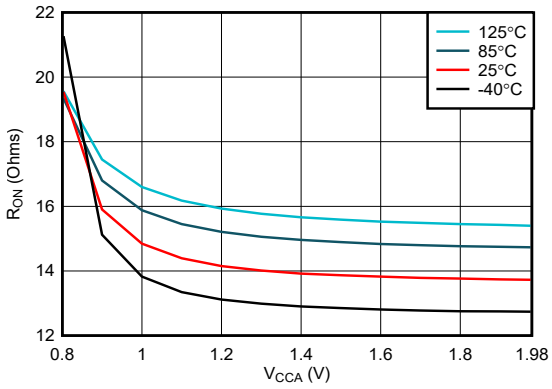


Figure 5-2. I_{CCB} (µA) vs V_{CCB} (V)



$V_{CCA} \leq V_{CCB}$

Figure 5-3. R_{ON} (Ω) vs Min(V_{CCA}, V_{CCB}) (V)

6 Parameter Measurement Information

Following load circuit is used to measure pulse duration, propagation delay, output rise-time and fall-time measurement.

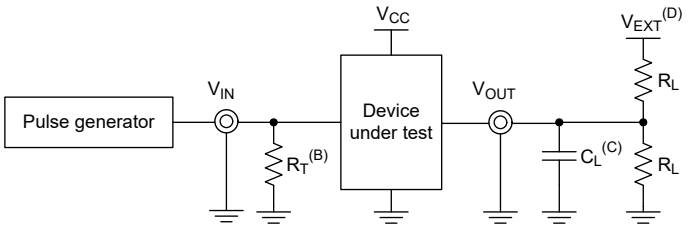


Figure 6-1. Load Circuit

A. Load resistance R_L = 1 MΩ for measuring data rate, pulse width, propagation delay and output rise and fall measurements. R_L = 50 kΩ for measuring enable and disable times.
B. R_T termination resistance should be equal to Z_{OUT} of pulse generators.
C. C_L Load capacitance includes probe and jig capacitance. C_L = 15 pF when on the B-side.
D. V_{EXT} External voltage for measuring switching times.
E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 26 MHz, Z_O = 50 Ω, slew rate ≥ 1 V/ns.
F. V_{CCI} is the V_{CC} associated with the input port.
G. V_{CCO} is the V_{CC} associated with the output port.

6.1 Voltage Waveforms

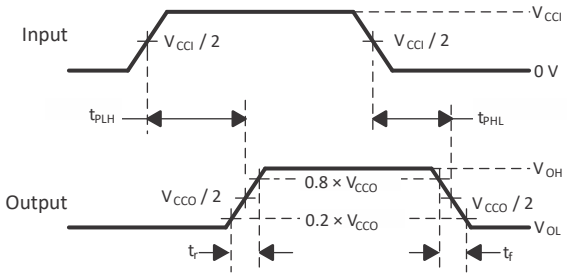
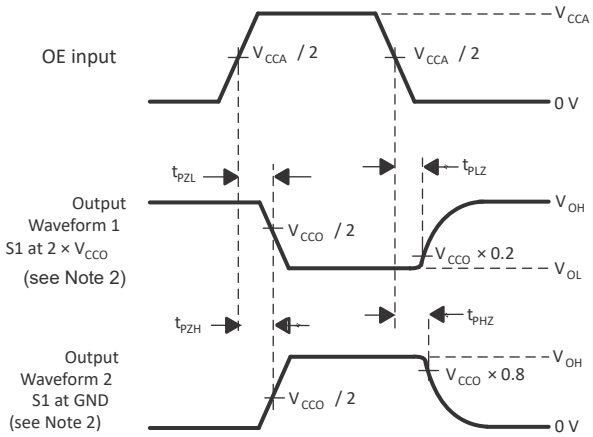


Figure 6-2. Propagation Delay Times



1. C_L includes probe and jig capacitance.
2. Waveform 1 in Figure 6-3 is for an output with internal such that the output is high, except when OE is high (see Figure 6-1). Waveform 2 in Figure 6-3 is for an output with conditions such that the output is low, except when OE is high.
3. All input pulses are supplied by generators having the following characteristics: PRR ≤ 26 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
4. The outputs are measured one at a time, with one transition per measurement.
5. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
6. t_{PZL} and t_{PZH} are the same as t_{en}.
7. t_{PLH} and t_{PHL} are the same as t_{pd}.
8. V_{CCI} is the V_{CC} associated with the input port.
9. V_{CCO} is the V_{CC} associated with the output port.

Figure 6-3. Enable and Disable Times

7 Detailed Description

7.1 Overview

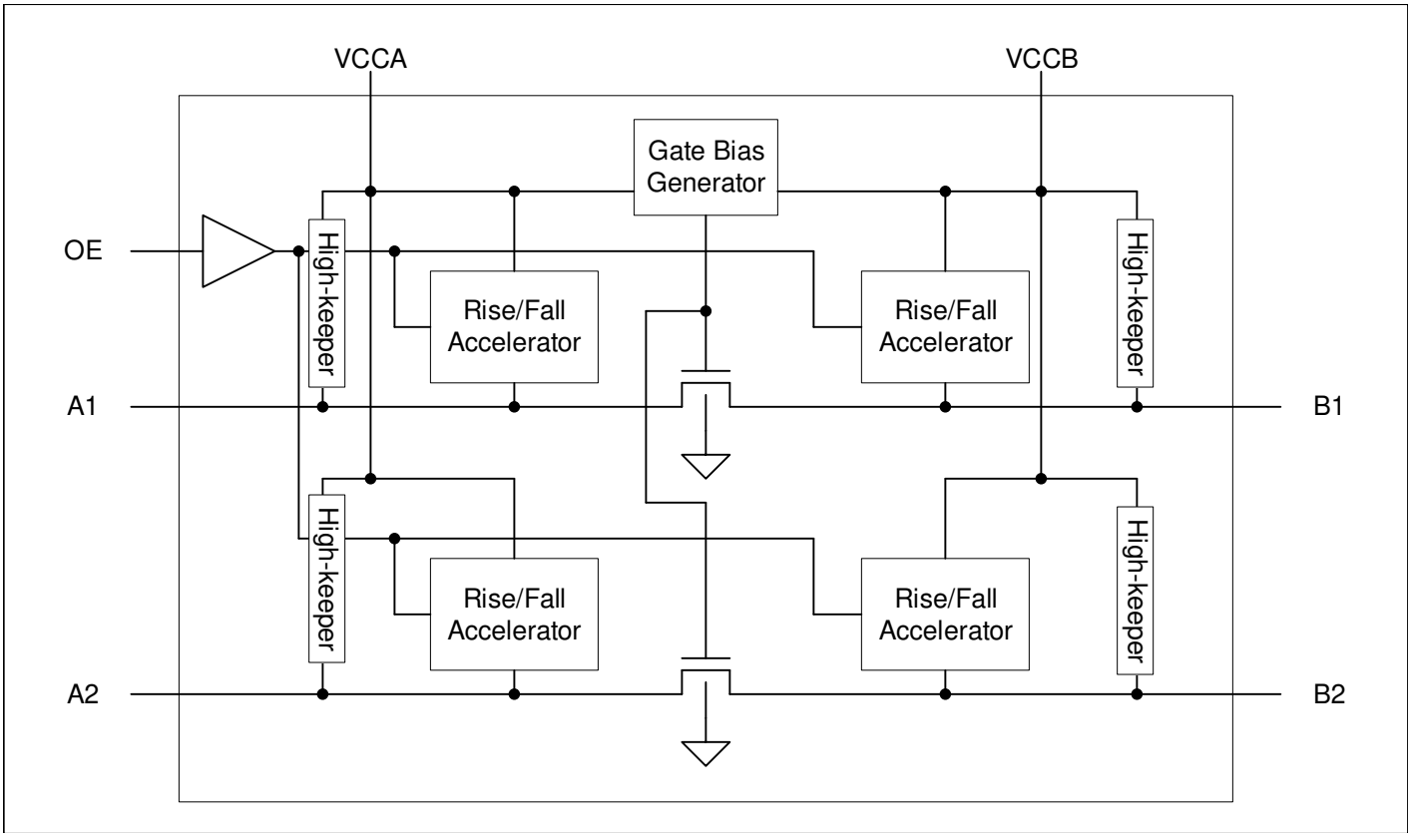
The TCA39416 device is a directionless voltage-level translator specifically designed for translating logic voltage levels. The device is MIPI I3C v1.1.1 compatible supporting data rates up to 12.5 Mbps in I3C Single Data Rate (SDR) mode and 25 Mbps in I3C High Data Rate (HDR-DDR) mode. Like SDR Mode, HDR-DDR Mode uses SCL as a clock; however unlike SDR, data is sampled on both edges of clock SCL effectively doubling the data rate achieving 25 Mbps.

The A and B ports are able to accept I/O voltages ranging from 0.72 V to 1.98 V. V_{CCA} must be ≤ V_{CCB} to ensure proper operation. The device is a pass-gate architecture with edge-rate accelerators (one-shots) to improve the overall data rate and supports both high speed push-pull and low speed open-drain operation.

MIPI I3C specification requires dynamic pull-up control to switch between “strong pull-up” and “weak pull-up” to optimize open-drain and push-pull timing requirements. In TCA39416, the internal 10-kΩ pull-up resistors on Ax and Bx pins are enabled based on respective VCC voltage and OE input and act as High-Keeper when the bus is high.

When OE is low, the TCA39416 is disabled, the one shots and internal pull ups are also disabled.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Architecture

The TCA39416 architecture (see Figure 7-1) is an auto-direction-sensing based translator that does not require a direction-control signal to control the direction of data flow from A to B or from B to A.

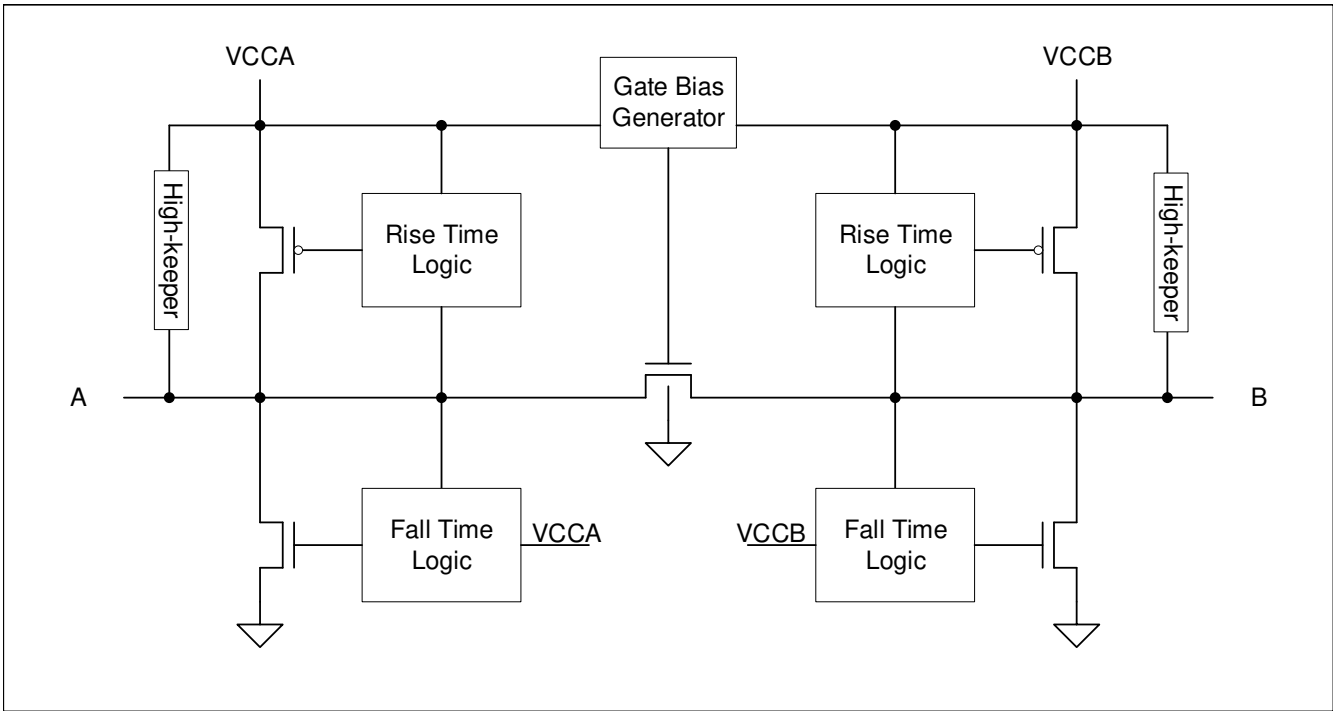


Figure 7-1. Architecture of a TCA39416 Cell

These two bidirectional channels support both directions of data flow without a direction-control signal. By properly biasing the gate of the pass-FET, the FET can turn on (low R_{DSON}), when either side input voltage drops to ~ 1 voltage threshold below the lowest of the two supplies.

The TCA39416 is part of the TI "Switch" type voltage translator family and employs key circuits to enable this voltage translation:

1. An N-channel pass-gate transistor topology that ties the A-port to the B-port.
2. Output rise time accelerator circuitry to detect and accelerate rising edges on the A or B ports
3. Output fall time accelerator circuitry to detect and accelerate falling edges on the A or B ports

For bidirectional voltage translation, pull up resistors are included on the device for dc current sourcing capability. The V_{GATE} gate bias of the N-channel pass transistor is set to the lower supply voltage and can be represented with V_{CCA}.

The rise and fall time accelerator (RTA and FTA, respectively) circuitry speeds up the output slew rate by monitoring the input edge for transitions, helping maintain the data rate through the device. During a low-to-high signal rising edge, the rise time accelerator (RTA) circuit turns on to increase the current drive capability of the driver. This edge-rate acceleration provides high ac drive by bypassing the internal 10-kΩ pull up resistors during the low-to-high transition to speed up the signal. The output resistance of the driver is decreased to approximately 150 Ω during this acceleration phase. During a high-to-low signal falling edge, the fall time accelerator (FTA) turns on to increase the current drive capability of the driver, similar to the rise time accelerator. This helps reduce the fall time for large capacitive loads. For light capacitive loads, the fall time accelerator will not enable.

7.3.2 Enable and Disable

The TCA39416 has an OE input that is used to disable the device by setting OE low, which prevents any signals from propagating across the device. This pin is referenced to the V_{CCA} supply. The rise and fall time accelerators and the internal pull-up resistors are also disabled. The disable time (t_{dis}) indicates the delay between the time when OE goes low and when the outputs are disabled (Hi-Z). The enable time (t_{en}) indicates the amount of time the user must allow for the one-shot circuitry to become operational after OE is taken high.

7.3.3 Pull up resistors on I/O Lines

I3C Controllers manage an active (such as, dynamic) pull-up resistance on SDA, which they can enable and disable as the bus transitions between open drain and push-pull mode. The continuous DC current sourcing or sinking capability is determined by the external system-level open-drain or push-pull drivers that are interfaced to the TCA39416 I/O pins.

In TCA39416, each A-port I/O has an internal 10-kΩ pull up resistor to V_{CCA}, and each B-port I/O has an internal 10-kΩ pull up resistor to V_{CCB}. The internal pull ups of the TCA39416 are controlled by their respective supplies. The resistors have back-biasing protection, so that if a supply is off, the current cannot flow through the resistors back into the supply. When both A and B side supply is above V_{UVLO_RISE} and OE is high, the pull up resistors are enabled when the bus is high.

7.3.4 Input Driver Requirements

The continuous dc-current "sinking" capability is determined by the external system-level open-drain (or push-pull) drivers that are interfaced to the TCA39416 I/O pins. Since the high bandwidth of these bidirectional I/O circuits is used to facilitate this fast change from an input to an output and an output to an input, they have a modest dc-current "sourcing" capability of hundreds of micro-Amps, as determined by the internal 10-kΩ pullup resistors.

The fall time (t_{fA}, t_{fB}) of a signal depends on the edge-rate and output impedance of the external device driving TCA39416 data I/Os, as well as the capacitive loading on the data lines.

Similarly, the t_{PHL} and max data rates also depend on the output impedance of the external driver. The values for t_{fA}, t_{fB}, t_{PHL}, and maximum data rates in the data sheet assume that the output impedance of the external driver is below V_{OL} on both sides.

7.4 Device Functional Modes

The TCA39416 device has two functional modes, enabled and disabled. To disable the device, set the OE input low, which disables the rise time and fall time accelerators, and prevents signals from propagating across the channels. The internal pull up resistors are also affected by the OE input and are disabled when OE input is low. Setting the OE input high enables the device. The internal pull-up resistors act has High-Keeper and are enabled based on respective VCC voltage when bus is high. Table 7-1 provides functional description for TCA39416.

Table 7-1. Functional table

Supply voltage(4)		Input(1)	I/O
V_{CCA}	V_{CCB}	OE(2)	
0.72 V to 1.98 V	0.72 V to 1.98 V	L	disconnected
0.72 V to 1.98 V	0.72 V to 1.98 V	H	A1 = B1; A2 = B2
GND(3)	GND(3)	X	disconnected

(1) H = HIGH voltage level; L = LOW voltage level; X = don't care
(2) OE is referenced to V_{CCA}. Pull OE low to place all outputs in 3-state mode.
(3) When either V_{CCA} or V_{CCB} is at GND level, the device goes into power-down mode.
(4) $V_{CCA} \leq V_{CCB}$.

8 Application and Implementation

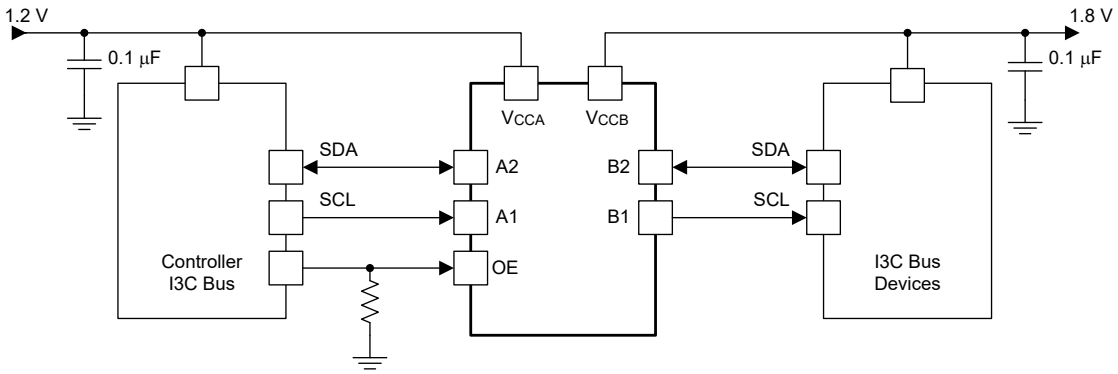
Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TCA39416 can be used to bridge the digital-switching compatibility gap between two voltage nodes to successfully interface logic threshold levels found in electronic systems. It should be used in a point-to-point topology for interfacing devices or systems operating at different interface voltages with one another. The primary target application use is for interfacing with I3C push-pull drivers or open-drain drivers on the data I/Os such as I^2C or SMBus, where the data is bidirectional and no control signal is available.

8.2 Typical Application



OE is referenced to V_{CCA}

Figure 8-1. Typical Application

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-1.

Table 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	0.72 V to 1.98 V
Output voltage range	0.72 V to 1.98 V

8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the TCA39416 device to determine the input voltage range. For a valid logic high, the value must exceed the V_{IH} of the input port. For a valid logic low, the value must be less than the V_{IL} of the input port.

- Output voltage range
  - Use the supply voltage of the device that the TCA39416 device is driving to determine the output voltage range
  - The TCA39416 device has 10-kΩ internal pull up resistors that act as high-keepers when the I/O lines are high.

8.2.3 Application Curve

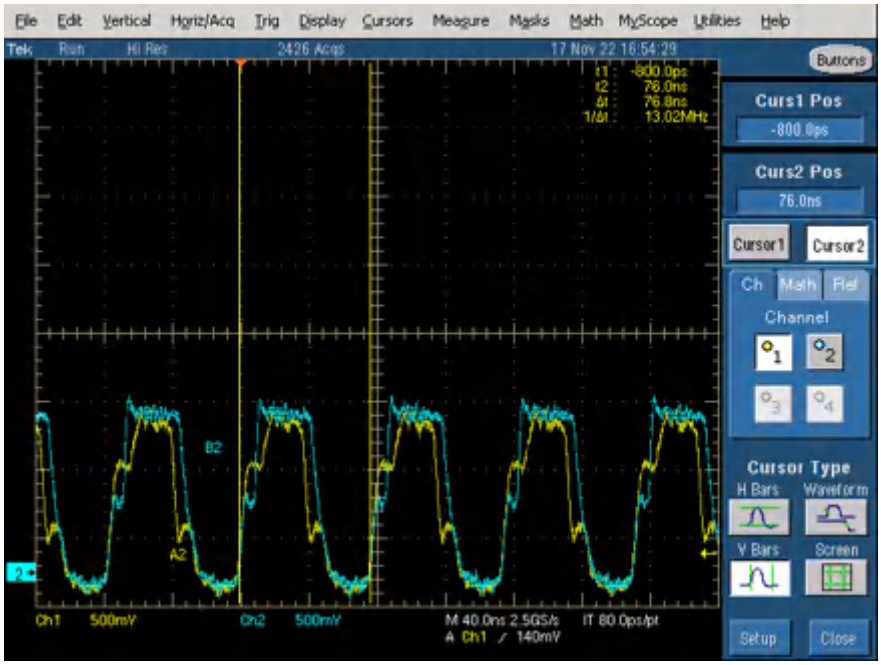


Figure 8-2. Level-Translation of a 12.5-MHz Signal

8.3 Power Supply Recommendations

The TCA39416 has no supply restrictions outside of the 0.72 V to 1.98 V range. V_{CCA} must be ≤ V_{CCB} for proper operation.

The sequencing of each power supply does not damage the device during the power up operation, so either power supply can be ramped up first. The output-enable (OE) input circuit is designed so that when the (OE) input is low, the outputs are disabled. No signals may propagate the rise time and fall time accelerators, and the internal pull up resistors are disabled. To make sure the signals do not pass through during power up or power down, the OE input pin must be tied to GND through a pull down resistor. The OE input pin should not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. If OE is tied to V_{CCA}, this is OK, but might result in a glitch on the bus during power up depending on the capacitive load and ramp rates. The minimum value of the pull down resistor to ground is determined by the current-sourcing capability of the driver.

8.4 Layout

8.4.1 Layout Guidelines

For reliability of the device, the following common printed-circuit board layout guidelines are recommended:

1. Bypass capacitors should be used on power supplies and should be placed as close as possible to the V_{CCA}, V_{CCB} pin, and G_{ND} pin.
2. Short trace lengths should be used to avoid excessive loading.
3. Keep Ax and Bx lengths close to prevent skewing the signals.
4. PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than the one-shot duration, approximately < 20 ns. Making sure that any reflection encounters low impedance at the source driver.

8.4.2 Layout Example

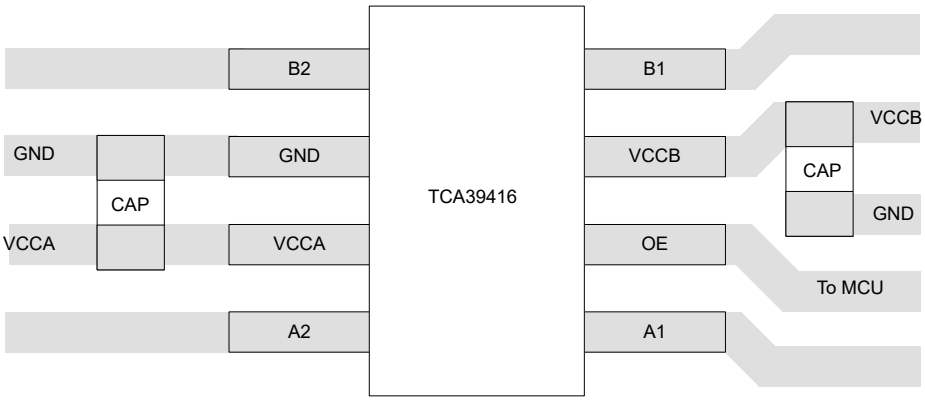


Figure 8-3. Layout Example (DDF)

9 Device and Documentation Support

9.1 Documentation Support

For related documentation see the following:

- Texas Instruments, *I3C - Next Generation Serial Communication Interface*

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (July 2023) to Revision B (November 2023)	Page
• Added *Feature* Compatibility with JEDEC I3C JESD403	1
• Changed t_{en} by deleting the typical value and changing the max value from 124 ns to 250 ns	7
• Changed t_{dis} by deleting the typical value and changing the max value from 68 ns to 350 ns	7
• Changed from 13C to I3C	14
• Changed round-trip delay from < 30 ns to < 20 ns	16

Changes from Revision * (December 2022) to Revision A (July 2023)	Page
• Deleted the Product Preview note from X2SON in the *Package Information* table	1
• Added thermal information for DTW	5
• Deleted sentence "When V_{CCA} is same as V_{CCB},…" from the *Power Supply Recommendations*	15

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTCA39416DTWR	ACTIVE	X2SON	DTW	8	3000	TBD	Call TI	Call TI	-40 to 125		Samples
TCA39416DDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2VIF	Samples
TCA39416DTWR	ACTIVE	X2SON	DTW	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1OC	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

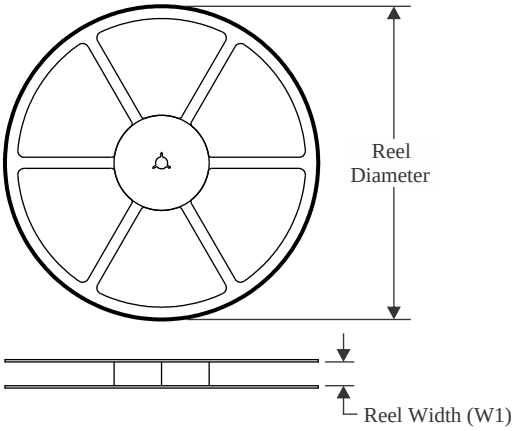
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

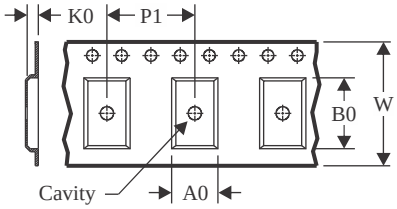
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

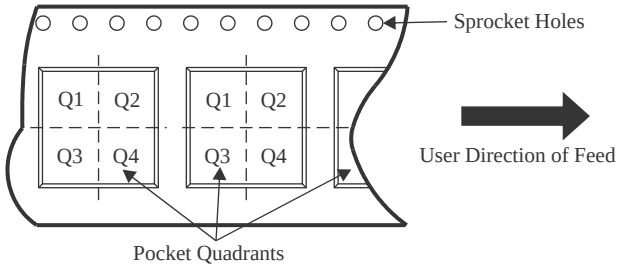


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

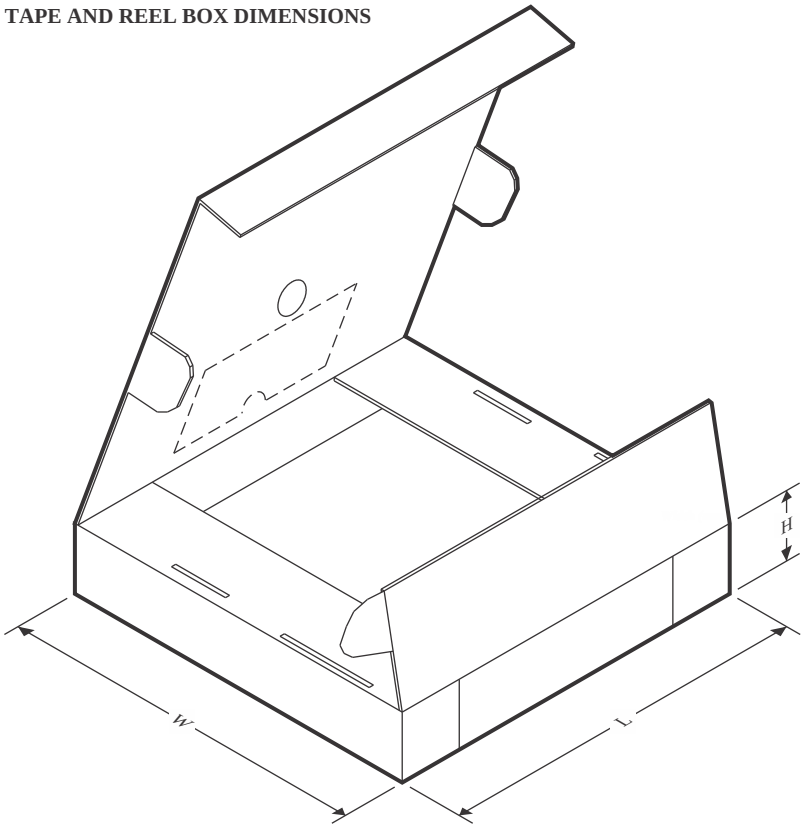
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA39416DDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TCA39416DTWR	X2SON	DTW	8	3000	180.0	8.4	1.15	1.5	0.55	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

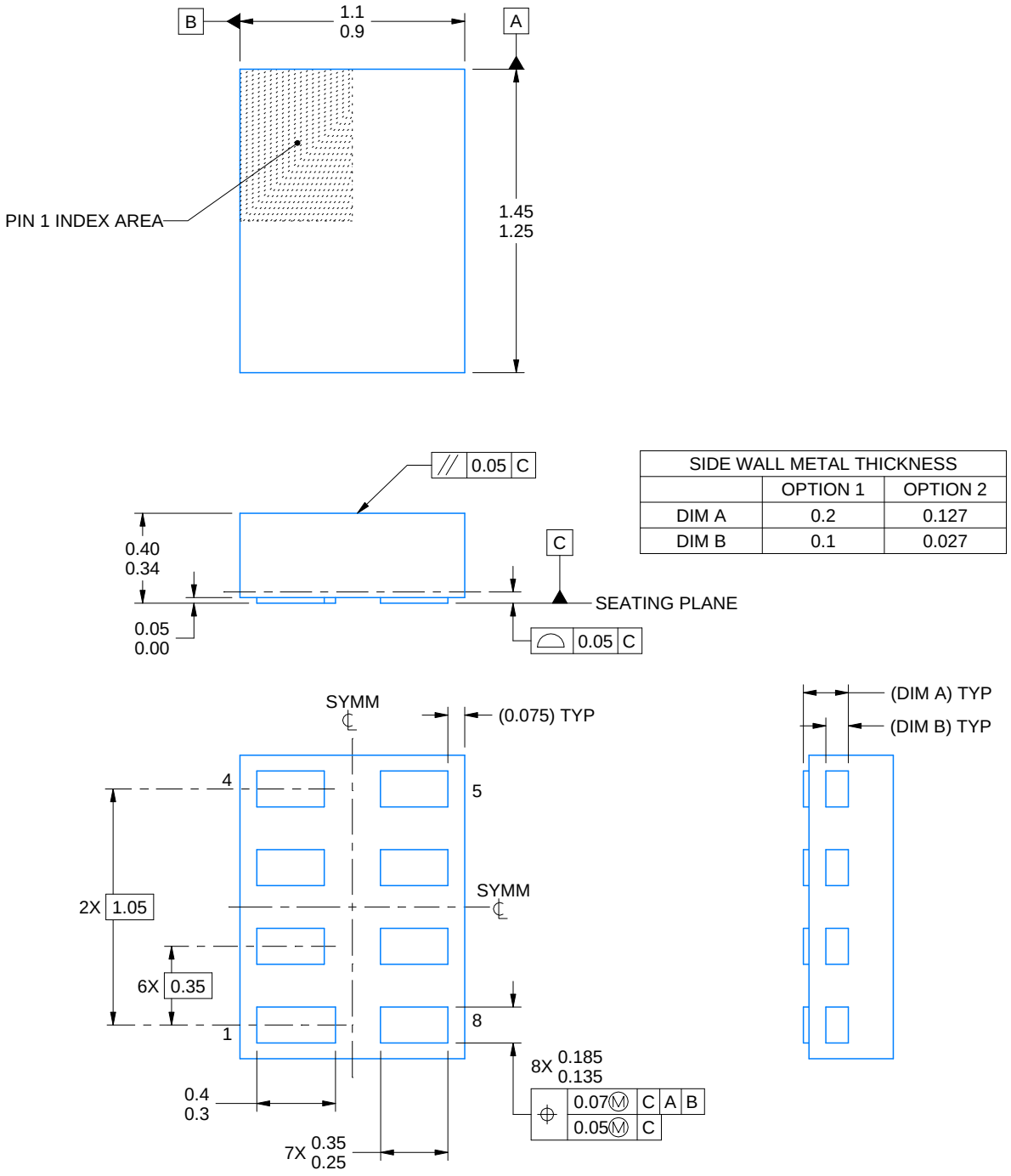
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA39416DDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TCA39416DTWR	X2SON	DTW	8	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DTW0008A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

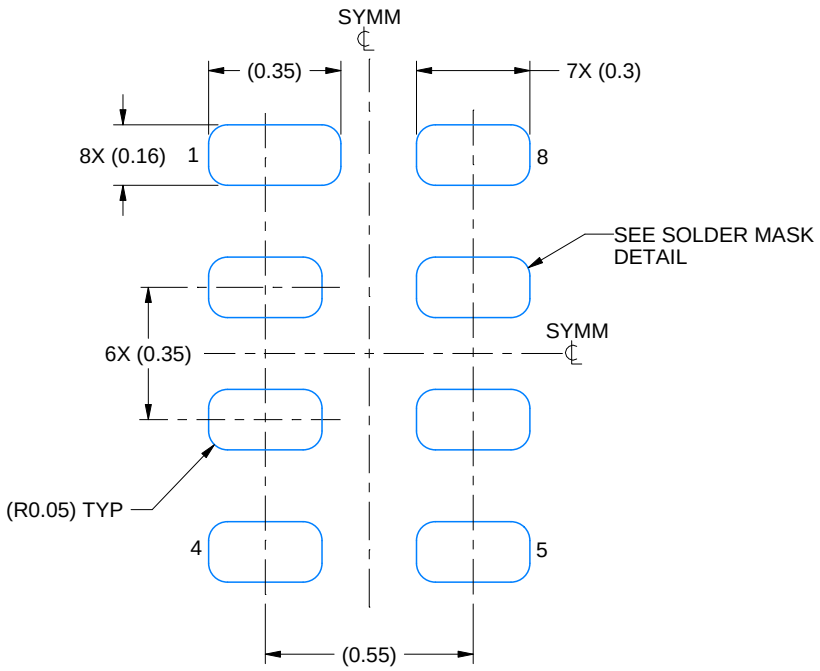


SIDE WALL METAL THICKNESS		
	OPTION 1	OPTION 2
DIM A	0.2	0.127
DIM B	0.1	0.027

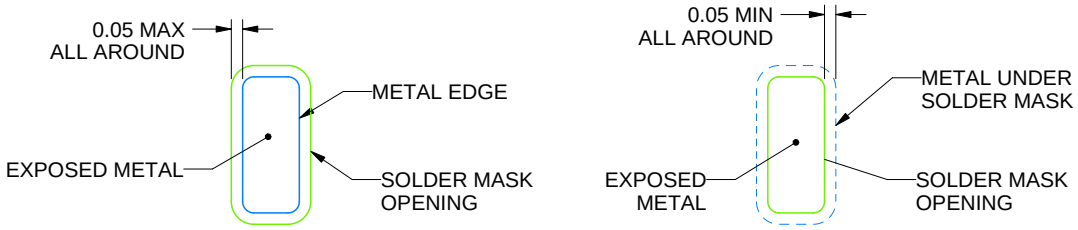
4228862/B 07/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package complies to JEDEC MO-287 variation X2EAF.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X



SOLDER MASK DETAILS

4228862/B 07/2023

NOTES: (continued)

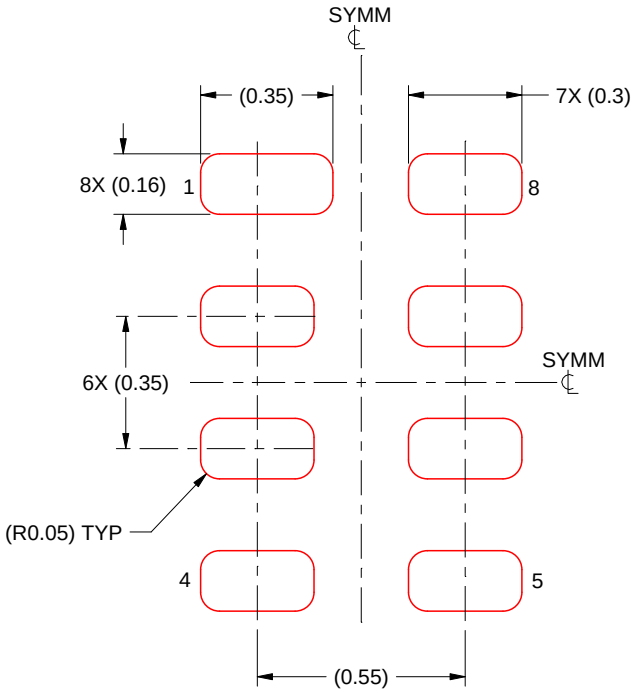
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DTW0008A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 MM THICK STENCIL
SCALE: 50X

4228862/B 07/2023

NOTES: (continued)

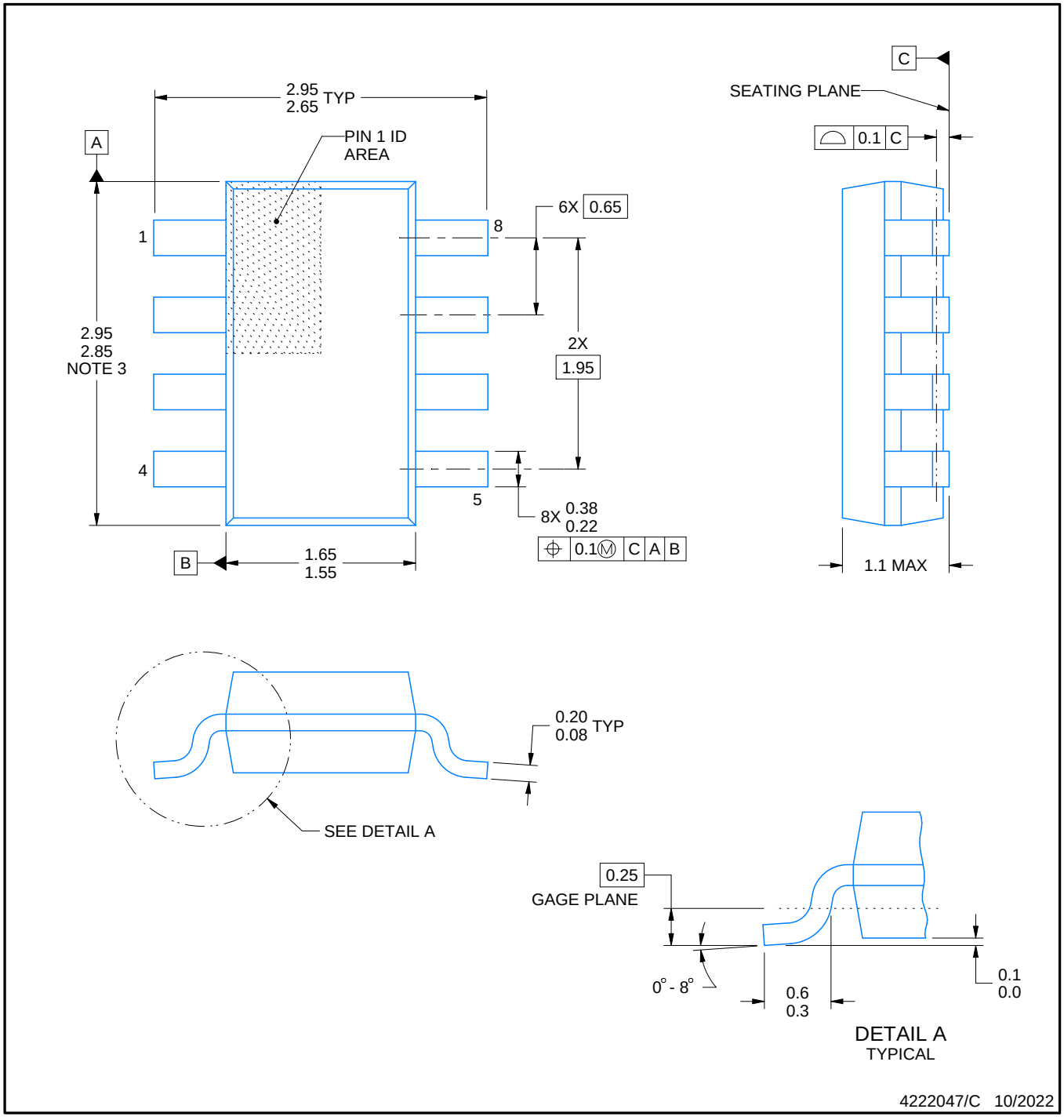
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DDF0008A

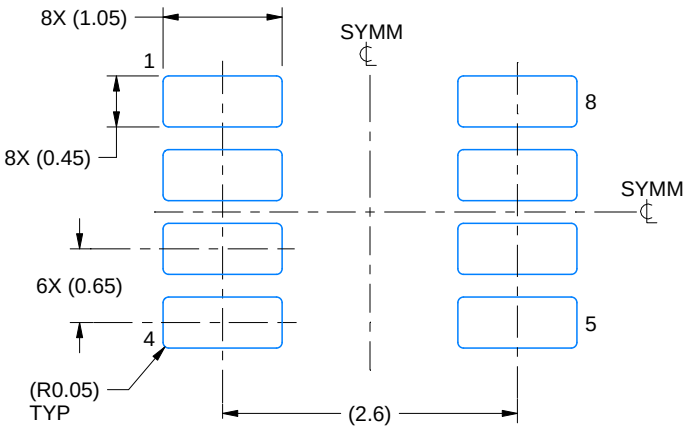
SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
SCALE:15X

NON SOLDER MASK
DEFINED

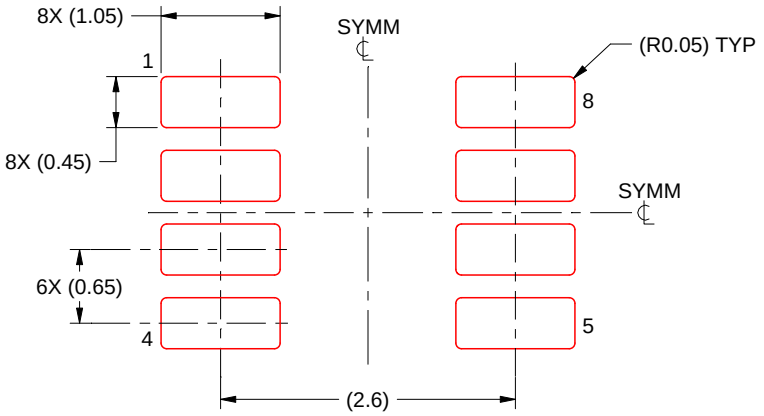
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222047/C 10/2022

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/C 10/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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