1 Features
- Two-Channel Bidirectional Buffer
- \(^{2}\text{C}\) Bus and SMBus Compatible
- Operating Supply Voltage Range of 0.9 V to 5.5 V on A-side
- Operating Supply Voltage Range of 2.7 V to 5.5 V on B-side
- Voltage-Level Translation From 0.9 V - 5.5 V to 2.7 V - 5.5 V
- Footprint and Functional Replacement for PCA9515B
- Active-High Repeater-Enable Input
- Open-Drain \(^{2}\text{C}\) I/O
- 5.5-V Tolerant \(^{2}\text{C}\) and Enable Input Support Mixed-Mode Signal Operation
- Accommodates Standard Mode and Fast Mode \(^{2}\text{C}\) Devices and Multiple Masters
- High-Impedance \(^{2}\text{C}\) Pins When Powered-Off
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 5500 V Human-Body Model (A114-A)
  - 200 V Machine Model (A115-A)
  - 1000 V Charged-Device Model (C101)

2 Applications
- Servers
- Routers (Telecom Switching Equipment)
- Industrial Equipment
- Products with Many \(^{2}\text{C}\) Slaves and/or Long PCB Traces

3 Description
The TCA9517 is a bidirectional buffer with level shifting capabilities for \(^{2}\text{C}\) and SMBus systems. It provides bidirectional voltage-level translation (up-transformation/down-transformation) between low voltages (down to 0.9 V) and higher voltages (2.7 V to 5.5 V) in mixed-mode applications. This device enables \(^{2}\text{C}\) and SMBus systems to be extended without degradation of performance, even during level shifting.

The TCA9517 buffers both the serial data (SDA) and the serial clock (SCL) signals on the \(^{2}\text{C}\) bus, thus allowing two buses of up to 400-pF bus capacitance to be connected in an \(^{2}\text{C}\) application.

The TCA9517 has two types of drivers: A-side drivers and B-side drivers. All inputs and I/Os are over-voltage tolerant to 5.5 V, even when the device is unpowered (V\text{CCB} and/or V\text{CCA} = 0 V).

Device Information(1)

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TCA9517</td>
<td>VSSOP (8)</td>
<td>3.00 mm × 3.00 mm</td>
</tr>
<tr>
<td></td>
<td>SOIC (8)</td>
<td>4.90 mm x 3.91 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic

---

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.
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4 Revision History
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (June 2015) to Revision D ...
Page

• Deleted VCCA < VCCB from the Design Requirements list ................................................................. 12

Changes from Revision B (May 2013) to Revision C ...
Page

• Added Pin Configuration and Functions section, ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section ........................................... 1
• Removed Ordering Information table. ..................................................................................................... 3

Changes from Revision A (April 2013) to Revision B ...
Page

• Updated the TOP-SIDE MARKING column of the ORDERING INFORMATION TABLE. ................................. 1

Changes from Original (December 2012) to Revision A ...
Page

• Added D package to document. .......................................................................................................... 1
• Updated the TOP-SIDE MARKING column of the ORDERING INFORMATION TABLE. ................................. 1
5 Description (continued)

The type of buffer design on the B-side prevents it from being used in series with devices which use static voltage offset. This is because these devices do not recognize buffered low signals as a valid low and do not propagate it as a buffered low again.

The B-side drivers operate from 2.7 V to 5.5 V. The output low level for this internal buffer is approximately 0.5 V, but the input voltage must be 70 mV or more below the output low level when the output internally is driven low. The higher-voltage low signal is called a buffered low. When the B-side I/O is driven low internally, the low is not recognized as a low by the input. This feature prevents a lockup condition from occurring when the input low condition is released.

The A-side drivers operate from 0.9 V to 5.5 V and drive more current. They do not require the buffered low feature (or the static offset voltage). This means that a low signal on the B-side translates to a nearly 0 V low on the A-side, which accommodates smaller voltage swings of lower-voltage logic. The output pulldown on the A-side drives a hard low, and the input level is set at 0.3 × V_{CCA} to accommodate the need for a lower low level in systems where the low-voltage-side supply voltage is as low as 0.9 V.

The A-side of two or more TCA9517s can be connected together, allowing many topographies (See Figure 8 and Figure 9), with the A-side as the common bus. Also, the A-side can be connected directly to any other buffer with static- or dynamic-offset voltage. Multiple TCA9517s can be connected in series, A-side to B-side, with no buildup in offset voltage and with only time-of-flight delays to consider. The TCA9517 cannot be connected B-side to B-side, because of the buffered low voltage from the B-side. The B-side cannot be connected to a device with rise time accelerators.

VCCA is only used to provide the 0.3 × V_{CCA} reference to the A-side input comparators and for the power-good-detect circuit. The TCA9517 logic and all I/Os are powered by the VCCB pin.

As with the standard I²C system, pullup resistors are required to provide the logic-high levels on the buffered bus. The TCA9517 has standard open-drain configuration of the I²C bus. The size of these pullup resistors depends on the system, but each side of the repeater must have a pullup resistor. The device is designed to work with Standard mode and Fast mode I²C devices in addition to SMBus devices. Standard mode I²C devices only specify 3 mA in a generic I²C system, where Standard mode devices and multiple masters are possible. Under certain conditions, higher termination currents can be used.
6 Pin Configuration and Functions

D Packages
8-Pin SOIC
Top View

<table>
<thead>
<tr>
<th>PIN</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VCCA</td>
<td>Supply A-side supply voltage (0.9 V to 5.5 V)</td>
</tr>
<tr>
<td>2</td>
<td>SCLA</td>
<td>Input/Output Serial clock bus, A-side. Connect to VCCA through a pull-up resistor. If unused, connect directly to ground.</td>
</tr>
<tr>
<td>3</td>
<td>SDAA</td>
<td>Input/Output Serial data bus, A-side. Connect to VCCA through a pull-up resistor. If unused, connect directly to ground.</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td>Ground Ground</td>
</tr>
<tr>
<td>5</td>
<td>EN</td>
<td>Input Active-high repeater enable input</td>
</tr>
<tr>
<td>6</td>
<td>SDAB</td>
<td>Input/Output Serial data bus, B-side. Connect to VCCB through a pull-up resistor. If unused, connect directly to ground.</td>
</tr>
<tr>
<td>7</td>
<td>SCLB</td>
<td>Input/Output Serial clock bus, B-side. Connect to VCCB through a pull-up resistor. If unused, connect directly to ground.</td>
</tr>
<tr>
<td>8</td>
<td>VCCB</td>
<td>Supply B-side and device supply voltage (2.7 V to 5.5 V)</td>
</tr>
</tbody>
</table>

DGK Package
8-Pin VSSOP
Top View

7 Specifications

7.1 Absolute Maximum Ratings
over operating free-air temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>PIN</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCCB</td>
<td>Supply voltage range</td>
<td>–0.5 (\text{V}) 7 (\text{V})</td>
</tr>
<tr>
<td>VCCA</td>
<td>Supply voltage range</td>
<td>–0.5 (\text{V}) 7 (\text{V})</td>
</tr>
<tr>
<td>(V_i)</td>
<td>Enable input voltage range(^{(2)})</td>
<td>–0.5 (\text{V}) 7 (\text{V})</td>
</tr>
<tr>
<td>(V_{IO})</td>
<td>I(^2)C bus voltage range(^{(2)})</td>
<td>–0.5 (\text{V}) 7 (\text{V})</td>
</tr>
<tr>
<td>(I_{IK})</td>
<td>Input clamp current</td>
<td>(V_i &lt; 0) (-50) (\text{mA})</td>
</tr>
<tr>
<td>(I_{OK})</td>
<td>Output clamp current</td>
<td>(V_O &lt; 0) (-50) (\text{mA})</td>
</tr>
<tr>
<td>(I_O)</td>
<td>Continuous output current</td>
<td>(\pm50) (\text{mA})</td>
</tr>
<tr>
<td>Continuous current through (V_{CC}) or GND</td>
<td>(\pm100) (\text{mA})</td>
<td></td>
</tr>
<tr>
<td>(T_{stg})</td>
<td>Storage temperature range</td>
<td>–65 (\text{°C}) 150 (\text{°C})</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

\(^{(2)}\) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
7.2 ESD Ratings

<table>
<thead>
<tr>
<th>Electrostatic discharge</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;ESD&lt;/sub&gt; (HBM)</td>
<td>±5500</td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub&gt;ESD&lt;/sub&gt; (CDM)</td>
<td>±1000</td>
<td>V</td>
</tr>
<tr>
<td>Machine model (A115-A)</td>
<td>±200</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;CC&lt;/sub&gt;A</td>
<td>0.9&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td>5.5</td>
</tr>
<tr>
<td>V&lt;sub&gt;CC&lt;/sub&gt;B</td>
<td>2.7</td>
<td>5.5</td>
</tr>
<tr>
<td>V&lt;sub&gt;IL&lt;/sub&gt;</td>
<td>0.3 × V&lt;sub&gt;CC&lt;/sub&gt;A</td>
<td>0.3 × V&lt;sub&gt;CC&lt;/sub&gt;B</td>
</tr>
<tr>
<td>I&lt;sub&gt;OL&lt;/sub&gt;</td>
<td>6</td>
<td>mA</td>
</tr>
<tr>
<td>T&lt;sub&gt;A&lt;/sub&gt;</td>
<td>−40</td>
<td>85</td>
</tr>
</tbody>
</table>

(1) Low-level supply voltage
(2) V<sub>IL</sub> specification is for the first low level seen by the SDAB and SCLB lines. V<sub>IL</sub> is for the second and subsequent low levels seen by the SDAB and SCLB lines. See V<sub>IL</sub> and Pullup Resistor Sizing for V<sub>IL</sub> application information.

7.4 Thermal Information

<table>
<thead>
<tr>
<th>Thermal Metric&lt;sup&gt;(1)&lt;/sup&gt;</th>
<th>TCA9517</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>DGK (VSSOP)</td>
<td>D (SOIC)</td>
</tr>
<tr>
<td>R&lt;sub&gt;JA&lt;/sub&gt;</td>
<td>187.6</td>
<td>133.6</td>
</tr>
<tr>
<td>R&lt;sub&gt;JCC(top)&lt;/sub&gt;</td>
<td>59.3</td>
<td>87.6</td>
</tr>
<tr>
<td>R&lt;sub&gt;JB&lt;/sub&gt;</td>
<td>108.6</td>
<td>74.2</td>
</tr>
<tr>
<td>ψ&lt;sub&gt;JT&lt;/sub&gt;</td>
<td>3.4</td>
<td>36.9</td>
</tr>
<tr>
<td>ψ&lt;sub&gt;JB&lt;/sub&gt;</td>
<td>106.9</td>
<td>73.7</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.
### 7.5 Electrical Characteristics

$V_{CCB} = 2.7 \, \text{V} \; \text{to} \; 5.5 \, \text{V}$, $GND = 0 \, \text{V}$, $T_A = -40^\circ \text{C} \; \text{to} \; 85^\circ \text{C}$ (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>$V_{CCB}$</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IK}$</td>
<td>Input clamp voltage</td>
<td>$I_I = -18 , \text{mA}$</td>
<td>$2.7 , \text{V} ; \text{to} ; 5.5 , \text{V}$</td>
<td>$-1.2$</td>
<td></td>
<td>$\text{V}$</td>
</tr>
<tr>
<td>$V_{DL}$</td>
<td>Low-level output voltage</td>
<td>SDAB, SCLB $I_{OL} = 100 , \mu\text{A}$ or $6 , \text{mA}$, $V_{ILA} = V_{ILB} = 0 , \text{V}$</td>
<td>$2.7 , \text{V} ; \text{to} ; 5.5 , \text{V}$</td>
<td>$0.45$</td>
<td>$0.52$</td>
<td>$0.6$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SDA, SCL $I_{OL} = 6 , \text{mA}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{DL} - V_{ILC}$</td>
<td>Low-level input voltage below low-level output voltage</td>
<td>SDAB, SCLB</td>
<td>$2.7 , \text{V} ; \text{to} ; 5.5 , \text{V}$</td>
<td>$70$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{ILC}$</td>
<td>SDA and SCL low-level input voltage contention</td>
<td>SDAB, SCLB</td>
<td>$2.7 , \text{V} ; \text{to} ; 5.5 , \text{V}$</td>
<td>$0.4$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{CC}$</td>
<td>Quiescent supply current for $V_{CCA}$</td>
<td>Both channels low, SDAA = SCLA = GND and SDAB = SCLB = open, or SDAA = SCLA = open and SDAB = SCLB = GND</td>
<td>$5.5 , \text{V}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Quiescent supply current</td>
<td>Both channels high, SDAA = SCLA = $V_{CCA}$ and SDAB = SCLB = $V_{CCB}$ and EN = $V_{CCB}$</td>
<td></td>
<td>$1.5$</td>
<td>$5$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Both channels low, SDAA = SCLA = GND and SDAB = SCLB = open</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>In contention, SDAA = SCLA = GND and SDAB = SCLB = GND</td>
<td></td>
<td>$3$</td>
<td>$5$</td>
<td></td>
</tr>
</tbody>
</table>

#### 7.6 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>$V_{CCB}$</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{II}$</td>
<td>Input leakage current</td>
<td>SDAB, SCLB $V_I = V_{CCB}$</td>
<td>$2.7 , \text{V} ; \text{to} ; 5.5 , \text{V}$</td>
<td>$10$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>SDAA, SCLB $V_I = 0.2 , \text{V}$</td>
<td></td>
<td>$10$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>En $V_I = V_{CCB}$</td>
<td></td>
<td>$10$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_I = V_{CCB}$</td>
<td></td>
<td>$10$</td>
<td></td>
</tr>
<tr>
<td>$I_{OH}$</td>
<td>High-level output leakage current</td>
<td>SDAB, SCLB $V_O = 3.6 , \text{V}$</td>
<td>$2.7 , \text{V} ; \text{to} ; 5.5 , \text{V}$</td>
<td>$10$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>SDA, SCL $V_I = 0.2 , \text{V}$</td>
<td></td>
<td>$10$</td>
<td></td>
</tr>
<tr>
<td>$C_I$</td>
<td>Input capacitance</td>
<td>EN $V_I = 3 , \text{V}$ or $0 , \text{V}$</td>
<td>$3.3 , \text{V}$</td>
<td>$6$</td>
<td>$10$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SCLB, SCL $V_I = 3 , \text{V}$ or $0 , \text{V}$</td>
<td>$3.3 , \text{V}$</td>
<td>$8$</td>
<td>$13$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$0 , \text{V}$</td>
<td>$7$</td>
<td>$11$</td>
<td>$\text{pF}$</td>
</tr>
<tr>
<td>$C_{IO}$</td>
<td>Input/output capacitance</td>
<td>SDAA, SCLB $V_I = 3 , \text{V}$ or $0 , \text{V}$</td>
<td>$3.3 , \text{V}$</td>
<td>$8$</td>
<td>$13$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$0 , \text{V}$</td>
<td>$7$</td>
<td>$11$</td>
<td>$\text{pF}$</td>
</tr>
</tbody>
</table>

(1) EN should change state only when the global bus and the repeater port are in an idle state.
### 7.7 I²C Interface Switching Characteristics

$V_{CCB} = 2.7$ V to 5.5 V, GND = 0 V, $T_A = -40°C$ to 85°C (unless otherwise noted)\(^{(1)}\)\(^{(2)}\)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP(^{(3)})</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{PLZ}$</td>
<td>SDAB, SCLB(^{(4)}) (see Figure 6)</td>
<td>SDAA, SCLA(^{(4)}) (see Figure 6)</td>
<td>$V_{CCA} \leq 2.7$ V (see Figure 6)</td>
<td>80</td>
<td>141</td>
<td>250</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>SDAA, SCLA(^{(5)}) (see Figure 5)</td>
<td>SDAB, SCLB(^{(5)}) (see Figure 5)</td>
<td>$V_{CCA} \geq 3$ V (see Figure 4)</td>
<td>25</td>
<td>74</td>
<td>110</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PLZ}$</td>
<td>SDAB, SCLB</td>
<td>SDAA, SCLA</td>
<td>$V_{CCA} \leq 2.7$ V (see Figure 4)</td>
<td>30</td>
<td>76(^{(6)})</td>
<td>110</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>SDAA, SCLA(^{(5)}) (see Figure 5)</td>
<td>SDAB, SCLB(^{(5)}) (see Figure 5)</td>
<td>$V_{CCA} \geq 3$ V (see Figure 4)</td>
<td>10</td>
<td>86</td>
<td>230</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{TLH}$</td>
<td>B-side to A side</td>
<td>80%</td>
<td>$V_{CCA} \leq 2.7$ V (see Figure 5)</td>
<td>10</td>
<td>12</td>
<td>15</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>A side to B-side (see Figure 4)</td>
<td>20%</td>
<td>$V_{CCA} \geq 3$ V (see Figure 5)</td>
<td>40</td>
<td>42</td>
<td>45</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>80%</td>
<td>20%</td>
<td></td>
<td>110</td>
<td>125</td>
<td>140</td>
<td></td>
</tr>
<tr>
<td>$t_{THL}$</td>
<td>B-side to A side</td>
<td>80%</td>
<td>$V_{CCA} \leq 2.7$ V (see Figure 5)</td>
<td>1</td>
<td>52(^{(6)})</td>
<td>105</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>A side to B-side (see Figure 4)</td>
<td>20%</td>
<td>$V_{CCA} \geq 3$ V (see Figure 5)</td>
<td>20</td>
<td>67</td>
<td>175</td>
<td></td>
</tr>
<tr>
<td></td>
<td>80%</td>
<td>20%</td>
<td></td>
<td>30</td>
<td>48</td>
<td>90</td>
<td></td>
</tr>
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</table>

(1) Times are specified with loads of 1.35-kΩ pull-up resistance and 50-pF load capacitance on the B-side and 167-Ω pull-up and 57-pF load capacitance on the A side. Different load resistance and capacitance alter the RC time constant, thereby changing the propagation delay and transition times.

(2) Pull-up voltages are $V_{CCA}$ on the A side and $V_{CCB}$ on the B-side.

(3) Typical values were measured with $V_{CCA} = V_{CCB} = 3.3$ V at $T_A = 25°C$, unless otherwise noted.

(4) The $t_{PLH}$ delay data from B to A side is measured at 0.4 V on the B-side to 0.5 $V_{CCA}$ on the A side when $V_{CCA}$ is less than 2 V, and 1.5 V on the A side if $V_{CCA}$ is greater than 2 V.

(5) The proportional delay data from A to B-side is measured at 0.3 $V_{CCA}$ on the A side to 1.5 V on the B-side.

(6) Typical value measured with $V_{CCA} = 2.7$ V at $T_A = 25°C$
7.8 Typical Characteristics

\[ V_{\text{CCA}} = 0.9 \, \text{V}, \quad V_{\text{CCB}} = 2.7 \, \text{V} \]

<table>
<thead>
<tr>
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<th>( V_{\text{OL}} ) (V)</th>
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<tr>
<td>0</td>
<td>0.025</td>
</tr>
<tr>
<td>1</td>
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<tr>
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<tr>
<td>4</td>
<td>0.125</td>
</tr>
<tr>
<td>5</td>
<td>0.15</td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>Port B</th>
<th>( V_{\text{OL}} ) (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0.49</td>
</tr>
<tr>
<td>1</td>
<td>0.5</td>
</tr>
<tr>
<td>2</td>
<td>0.51</td>
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<tr>
<td>3</td>
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<tr>
<td>4</td>
<td>0.53</td>
</tr>
<tr>
<td>5</td>
<td>0.54</td>
</tr>
</tbody>
</table>

![Figure 1. Port A \( V_{\text{OL}} \) vs \( I_{\text{OL}} \)](image1)

![Figure 2. Port B \( V_{\text{OL}} \) vs \( I_{\text{OL}} \)](image2)
8 Parameter Measurement Information

A. $R_L = 167 \, \Omega$ (0.9 V to 2.7 V) and $R_L = 450 \, \Omega$ (3.0 V to 5.5 V) on the A side and 1.35 k\Omega on the B-side
B. $R_T$ termination resistance should be equal to $Z_{OUT}$ of pulse generators.
C. $C_L$ includes probe and jig capacitance.
D. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10$ MHz, $Z_O = 50$ \Omega, slew rate $\geq 1$ V/ns.
E. The outputs are measured one at a time, with one transition per measurement.
F. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
G. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{ds}$.
H. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.

**Figure 3. Test Circuit**

**Figure 4. Waveform 1 – Propagation Delay and Transition Times for B-side to A-side**

**Figure 5. Waveform 2 – Propagation Delay and Transition Times for A-side to B-side**

**Figure 6. Waveform 3 – Propagation Delay for B-side to A-side**
9 Detailed Description

9.1 Overview

The TCA9517 is a bidirectional buffer with level shifting capabilities for \( \text{I}^2\text{C} \) and SMBus systems. It provides bidirectional voltage-level translation (up-translation/down-translation) between low voltages (down to 0.9 V) and higher voltages (2.7 V to 5.5 V) in mixed-mode applications. This device enables \( \text{I}^2\text{C} \) and SMBus systems to be extended without degradation of performance, even during level shifting.

The TCA9517 buffers both the serial data (SDA) and the serial clock (SCL) signals on the \( \text{I}^2\text{C} \) bus, thus allowing two buses of up to 400-pF bus capacitance to be connected in an \( \text{I}^2\text{C} \) application.

The TCA9517 has two types of drivers: A-side drivers and B-side drivers. All inputs and I/Os are over-voltage tolerant to 5.5 V, even when the device is unpowered (\( V_{\text{CCB}} \) and/or \( V_{\text{CCA}} = 0 \) V).

9.2 Functional Block Diagram
9.3 Feature Description

9.3.1 Two-Channel Bidirectional Buffer

The TCA9517 is a two-channel bidirectional buffer with level-shifting capabilities.

9.3.2 Active-High Repeater-Enable Input

The TCA9517 has an active-high enable (EN) input with an internal pull-up to $V_{CCB}$, which allows the user to select when the repeater is active. This can be used to isolate a badly behaved slave on power-up reset. The EN input should change state only when the global bus and repeater port are in an idle state, to prevent system failures.

9.3.3 $V_{OL}$ B-Side Offset Voltage

The B-side drivers operate from 2.7 V to 5.5 V. The output low level for this internal buffer is approximately 0.5 V, but the input voltage must be 70 mV or more below the output low level when the output internally is driven low. The higher-voltage low signal is called a buffered low. When the B-side I/O is driven low internally, the low is not recognized as a low by the input. This feature prevents a lockup condition from occurring when the input low condition is released. This type of design prevents 2 B-side ports from being connected to each other.

9.3.4 Standard Mode and Fast Mode Support

The TCA9517 supports standard mode as well as fast mode I2C. The maximum system operating frequency will depend on system design and the delays added by the repeater.

9.3.5 Clock Stretching Support

The TCA9517 can support clock stretching, but care needs to be taken to minimize the overshoot voltage presented during the hand-off between the slave and master. This is best done by increasing the pull-up resistor value.

9.4 Device Functional Modes

<table>
<thead>
<tr>
<th>INPUT</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>Outputs disabled</td>
</tr>
</tbody>
</table>
| H     | SDAA = SDAB  
SCLA = SCLB             |
10 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

A typical application is shown in Figure 7. In this example, the system master is running on a 3.3 V I²C bus, and the slave is connected to a 1.2 V I²C bus. Both buses run at 400 kHz. Master devices can be placed on either bus.

The TCA9517 is 5-V tolerant, so it does not require any additional circuitry to translate between 0.9 V to 5.5 V bus voltages and 2.7 V to 5.5 V bus voltages.

When the A side of the TCA9517 is pulled low by a driver on the I²C bus, a comparator detects the falling edge when it goes below 0.3 × V_{CCA} and causes the internal driver on the B-side to turn on, causing the B-side to pull down to about 0.5 V. When the B-side of the TCA9517 falls, first a CMOS hysteresis-type input detects the falling edge and causes the internal driver on the A side to turn on and pull the A-side pin down to ground. In order to illustrate what would be seen in a typical application, refer to Figure 9 and Figure 10. If the bus master in Figure 7 were to write to the slave through the TCA9517, waveforms shown in Figure 9 would be observed on the A bus. This looks like a normal I²C transmission, except that the high level may be as low as 0.9 V, and the turn on and turn off of the acknowledge signals are slightly delayed.

On the B-side bus of the TCA9517, the clock and data lines would have a positive offset from ground equal to the V_{OL} of the TCA9517. After the eighth clock pulse, the data line is pulled to the V_{OL} of the slave device, which is very close to ground in this example. At the end of the acknowledge, the level rises only to the low level set by the driver in the TCA9517 for a short delay, while the A-bus side rises above 0.3 × V_{CCA} and then continues high.

10.2 Typical Application

![Figure 7. Typical Application Schematic](image)

10.2.1 Design Requirements

For the level translating application, the following should be true:

- V_{CCA} = 0.9 V to 5.5 V
- V_{CCB} = 2.7 to 5.5 V
- B-side ports must not be connected together
Typical Application (continued)

10.2.2 Detailed Design Procedure

10.2.2.1 Clock Stretching Support
The TCA9517 can support clock stretching, but care needs to be taken to minimize the overshoot voltage presented during the hand-off between the slave and master. This is best done by increasing the pull-up resistor value.

10.2.2.2 $V_{ILC}$ and Pullup Resistor Sizing
For the TCA9517 to function correctly, all devices on the B-side must be able to pull the B-side below the voltage input low contention level ($V_{ILC}$). This means that the $V_{OL}$ of any device on the B-side must be below 0.4 V.

$V_{OL}$ of a device can be adjusted by changing the $I_{OL}$ through the device which is set by the pull-up resistance value. The pull-up resistance on the B-side must be carefully selected to ensure that logic levels will be transferred correctly to the A-side.

![Typical Star Application](image)

Figure 8. Typical Star Application

Multiple A sides of TCA9517s can be connected in a star configuration, allowing all nodes to communicate with each other.
Typical Application (continued)

To further extend the I²C bus for long traces/cables, multiple TCA9517s can be connected in series as long as the A-side is connected to the B-side. I²C bus slave devices can be connected to any of the bus segments. The number of devices that can be connected in series is limited by repeater delay/time-of-flight considerations on the maximum bus speed requirements.

Figure 9. Typical Series Application

Figure 10. Bus A (0.9 V to 5.5 V Bus) Waveform

Figure 11. Bus B (2.7 V to 5.5 V Bus) Waveform
11 Power Supply Recommendations

$V_{CCB}$ and $V_{CCA}$ can be applied in any sequence at power up. The TCA9517 includes a power-up circuit that keeps the output drivers turned off until $V_{CCB}$ is above 2.5 V and the $V_{CCA}$ is above 0.8 V. After power up and with the EN high, a low level on the A-side (below $0.3 \times V_{CCA}$) turns the corresponding B-side driver (either SDA or SCL) on and drives the B-side down to approximately 0.5 V. When the A-side rises above $0.3 \times V_{CCA}$, the B-side pull-down driver is turned off and the external pull-up resistor pulls the pin high. When the B-side falls first and goes below $0.3 \times V_{CCB}$, the A-side driver is turned on and the A-side pulls down to 0 V. The B-side pull-down is not enabled unless the B-side voltage goes below 0.4 V. If the B-side low voltage does not go below 0.5 V, the A-side driver turns off when the B-side voltage is above $0.7 \times V_{CCB}$. If the B-side low voltage goes below 0.4 V, the B-side pull-down driver is enabled, and the B-side is able to rise to only 0.5 V until the A-side rises above $0.3 \times V_{CCA}$.

TI recommends using a decoupling capacitor and placing it close to the VCCA and VCCB pins of a value of about 100 nF.
12 Layout

12.1 Layout Guidelines
There are no special layout procedures required for the TCA9517.
It is recommended that the decoupling capacitors be placed as close to the VCC pins as possible.

12.2 Layout Example
Figure 13 shows an example layout of the DGK package.

Figure 13. TCA9517A Layout Example

= Via to GND Plane
13 Device and Documentation Support

13.1 Community Resource
The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support TI's Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.2 Trademarks
E2E is a trademark of Texas Instruments. All other trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary
SLYZ022 — TI Glossary.
This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

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<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead finish/Ball material</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
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<td>DGK</td>
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<td>2500</td>
<td>RoHS &amp; Green</td>
<td>NIPDAUAG</td>
<td>SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>AYK</td>
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<tr>
<td>TCA9517DR</td>
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<td>D</td>
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<td>PW517</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
- **RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
- **Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead finish/Ball material** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
OTHER QUALIFIED VERSIONS OF TCA9517:

- Automotive: TCA9517-Q1

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
TAPE DIMENSIONS

- A0: Dimension designed to accommodate the component width
- B0: Dimension designed to accommodate the component length
- K0: Dimension designed to accommodate the component thickness
- W: Overall width of the carrier tape
- P1: Pitch between successive cavity centers

REEL DIMENSIONS

- A0: Overall width of the carrier tape
- B0: Pitch between successive cavity centers
- K0: Dimension designed to accommodate the component width
- W: Reel Diameter

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

- Q1, Q2, Q3, Q4: Pocket Quadrants

User Direction of Feed

Pocket Quadrants

Sprocket Holes

*All dimensions are nominal

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<th>Device</th>
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TAPE AND REEL BOX DIMENSIONS

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*All dimensions are nominal*
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.
DGK (S-PDSO-G8)  PLASTIC SMALL-OUTLINE PACKAGE

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
  □ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
  □ Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO-187 variation AA, except interlead flash.

4073329/E 05/06
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
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