1 Features

- AEC Q100 (Grade 1): Qualified for automotive applications
- Meets the requirements of ISO 11898-2:2016 and CiA 601-4 standards
- Classical CAN and CAN FD up to 8 Mbps
  - Actively improves the bus signal by reducing ringing effects in complex topologies
  - Backward compatible for use in classic CAN networks
- \( V_{IO} \) level shifting supports: 1.7 V to 5.5 V
- Operating Modes
  - Normal mode
  - Low-power standby mode supporting remote wake-up request
- Ideal passive behavior when unpowered
  - Bus and logic terminals are high impedance (no load to operating bus or application)
  - Hot plug capable: power up/down glitch free operation on bus and RXD output
  - Defined device behavior with floating logic pins and in undervoltage supply conditions
- Protection features
  - IEC ESD protection on bus pins
  - \( \pm 58 \) V CAN bus fault tolerant
  - Undervoltage protection on \( V_{CC} \) and \( V_{IO} \) (\( V \) variants only) supply terminals
  - TXD dominant state timeout (TXD DTO)
  - Thermal shutdown protection (TSD)
- Available in SOIC (8), small footprint SOT-23 (8) and leadless 3mm x 3mm VSON (8) package with wettable flanks for improved automated optical inspection (AOI) capability

2 Applications

- Automotive gateway
- Advanced driver assistance system (ADAS)
- Body electronics and lighting
- Hybrid, electric & powertrain systems
- Automotive infotainment & cluster

3 Description

The TCAN1462-Q1 and TCAN1462V-Q1 are high speed Controller Area Network (CAN) transceivers that meet the physical layer requirements of the ISO 11898-2:2016 high speed CAN specification and the CiA 601-4 Signal Improvement (SIC) specification. The devices reduce signal ringing at dominant-to-recessive edge and enable higher throughput in complex network topologies. Signal improvement capability allows the applications to extract real benefit of CAN FD (flexible data rate) by being able to operate at 2 Mbps, 5 Mbps or even beyond in large networks with multiple unterminated stubs.

The devices meet the timing specifications mandated by CiA 601-4, thus have much tighter bit timing symmetry compared to a regular CAN FD transceivers. This provides larger timing window to sample the correct bit and enables error-free communication in large complex star networks where ringing and bit distortion are inherent.

These devices are pin-compatible to 8-pin CAN FD transceivers, such as TCAN1044A-Q1 or TCAN1042-Q1.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE(1)</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TCAN1462(V)-Q1</td>
<td>SOT-23 (DDF)</td>
<td>2.90 mm x 1.60 mm</td>
</tr>
<tr>
<td></td>
<td>VSON (DRB)</td>
<td>3.00 mm x 3.00 mm</td>
</tr>
<tr>
<td></td>
<td>SOIC (D)</td>
<td>4.90 mm x 3.91 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Block Diagram
Table of Contents

1 Features ............................................................................ 1
2 Applications ....................................................................... 1
3 Description ......................................................................... 1
4 Revision History ................................................................... 2
5 Description Continued ................................................................. 2
6 Device Comparison Table ............................................................... 2
7 Pin Configurations and Functions .................................................. 3
8 Device and Documentation Support .................................................. 4

4 Revision History

<table>
<thead>
<tr>
<th>DATE</th>
<th>REVISION</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>February 2022</td>
<td>*</td>
<td>Initial Revision</td>
</tr>
</tbody>
</table>

5 Description Continued

The TCAN1462-Q1 devices with suffix 'V' include internal logic level translation via the $V_{IO}$ logic supply terminal to allow for interfacing directly to 1.8 V, 2.5 V, or 3.3 V controllers. The transceivers support low power standby mode which allows remote wake-up via CAN bus compliant with ISO 11898-2:2016 defined wake-up pattern (WUP). The device family also includes many protection features such as undervoltage detection, thermal shutdown (TSD), driver dominant timeout (TXD DTO), and ±58 V bus fault protection.

6 Device Comparison Table

<table>
<thead>
<tr>
<th>Device Number</th>
<th>Bus Fault Protection</th>
<th>Low voltage I/O Logic Support on Pin 5</th>
<th>Pin 8 Mode Selection</th>
</tr>
</thead>
<tbody>
<tr>
<td>TCAN1462-Q1</td>
<td>± 58 V</td>
<td>No</td>
<td>Low Power Standby Mode with Remote Wake</td>
</tr>
<tr>
<td>TCAN1462V-Q1</td>
<td>± 58 V</td>
<td>Yes</td>
<td></td>
</tr>
</tbody>
</table>
7 Pin Configurations and Functions

![Pin Configurations and Functions Diagram]

Table 7-1. Pin Functions

<table>
<thead>
<tr>
<th>PINS</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>TXD</td>
<td>1</td>
<td>Digital Input</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CAN transmit data input, integrated pull-up</td>
</tr>
<tr>
<td>GND</td>
<td>2</td>
<td>GND</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Ground connection</td>
</tr>
<tr>
<td>VCC</td>
<td>3</td>
<td>Supply</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5 V supply voltage</td>
</tr>
<tr>
<td>RXD</td>
<td>4</td>
<td>Digital Output</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CAN receive data output, tristate when powered off</td>
</tr>
<tr>
<td>VIO</td>
<td>5</td>
<td>Supply</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Logic supply voltage</td>
</tr>
<tr>
<td>NC</td>
<td>6</td>
<td>No Connect (not internally connected); Devices without VIO</td>
</tr>
<tr>
<td>CANL</td>
<td>6</td>
<td>Bus IO</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Low-level CAN bus input/output line</td>
</tr>
<tr>
<td>CANH</td>
<td>7</td>
<td>Bus IO</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High-level CAN bus input/output line</td>
</tr>
<tr>
<td>STB</td>
<td>8</td>
<td>Digital Input</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Standby mode control input, integrated pull-up</td>
</tr>
<tr>
<td>Thermal Pad</td>
<td>—</td>
<td>Electrically connected to GND, connect the thermal pad to the</td>
</tr>
<tr>
<td>(VSON only)</td>
<td></td>
<td>printed circuit board (PCB) ground plane for thermal relief</td>
</tr>
</tbody>
</table>

Figure 7-1. SOIC (D) and SOT-23 (DDF) Package, 8 Pin (Top View)

Figure 7-2. VSON (DRB) Package, 8 Pin (Top View)
8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.3 Trademarks

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8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
9.1 Tape and Reel Information

REEL DIMENSIONS

TAPE DIMENSIONS

A0: Dimension designed to accommodate the component width
B0: Dimension designed to accommodate the component length
K0: Dimension designed to accommodate the component thickness
W: Overall width of the carrier tape
P1: Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Pocket Quadrants

Sprocket Holes

User Direction of Feed

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>TCAN1462DRQ1</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>330.0</td>
<td>12.5</td>
<td>6.4</td>
<td>5.2</td>
<td>2.1</td>
<td>8.0</td>
<td>12.0</td>
<td>Q2</td>
</tr>
<tr>
<td>TCAN1462VDRQ1</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>330.0</td>
<td>12.5</td>
<td>6.4</td>
<td>5.2</td>
<td>2.1</td>
<td>8.0</td>
<td>12.0</td>
<td>Q2</td>
</tr>
<tr>
<td>TCAN1462DDFRQ1</td>
<td>SOT-23</td>
<td>DDF</td>
<td>8</td>
<td>3000</td>
<td>330.0</td>
<td>12.4</td>
<td>3.3</td>
<td>3.3</td>
<td>1.1</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
<tr>
<td>TCAN1462DDFRQ1</td>
<td>SOT-23</td>
<td>DDF</td>
<td>8</td>
<td>3000</td>
<td>330.0</td>
<td>12.4</td>
<td>3.3</td>
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<td>1.1</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
<tr>
<td>TCAN1462DRBRQ1</td>
<td>SON</td>
<td>DRB</td>
<td>8</td>
<td>3000</td>
<td>330.0</td>
<td>12.4</td>
<td>3.3</td>
<td>3.3</td>
<td>1.0</td>
<td>8.0</td>
<td>12.0</td>
<td>Q2</td>
</tr>
<tr>
<td>TCAN1462VDRBRQ1</td>
<td>SON</td>
<td>DRB</td>
<td>8</td>
<td>3000</td>
<td>330.0</td>
<td>12.4</td>
<td>3.3</td>
<td>3.3</td>
<td>1.0</td>
<td>8.0</td>
<td>12.0</td>
<td>Q2</td>
</tr>
</tbody>
</table>
## TAPE AND REEL BOX DIMENSIONS

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TCAN1462DRQ1</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>340.5</td>
<td>336.1</td>
<td>25.0</td>
</tr>
<tr>
<td>TCAN1462VDRQ1</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>340.5</td>
<td>336.1</td>
<td>25.0</td>
</tr>
<tr>
<td>TCAN1462DDFRQ1</td>
<td>SOT-23</td>
<td>DDF</td>
<td>8</td>
<td>3000</td>
<td>210.0</td>
<td>185.0</td>
<td>210.0</td>
</tr>
<tr>
<td>TCAN1462VDDFRQ1</td>
<td>SOT-23</td>
<td>DDF</td>
<td>8</td>
<td>3000</td>
<td>210.0</td>
<td>185.0</td>
<td>210.0</td>
</tr>
<tr>
<td>TCAN1462DRBRQ1</td>
<td>SON</td>
<td>DRB</td>
<td>8</td>
<td>3000</td>
<td>346.0</td>
<td>346.0</td>
<td>35.0</td>
</tr>
<tr>
<td>TCAN1462VDRBRQ1</td>
<td>SON</td>
<td>DRB</td>
<td>8</td>
<td>3000</td>
<td>346.0</td>
<td>346.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15], per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.
**PACKAGING INFORMATION**

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead finish/ Ball material</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>PTCAN1462DRBRQ1</td>
<td>ACTIVE</td>
<td>SON</td>
<td>DRB</td>
<td>8</td>
<td>3000</td>
<td>TBD</td>
<td>Call TI</td>
<td>Call TI</td>
<td>-40 to 125</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PTCAN1462DRQ1</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>3000</td>
<td>TBD</td>
<td>Call TI</td>
<td>Call TI</td>
<td>-40 to 125</td>
<td></td>
<td>Samples</td>
</tr>
<tr>
<td>PTCAN1462VDRBRQ1</td>
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<td>DRB</td>
<td>8</td>
<td>3000</td>
<td>TBD</td>
<td>Call TI</td>
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<td>-40 to 125</td>
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</tr>
<tr>
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<td>3000</td>
<td>TBD</td>
<td>Call TI</td>
<td>Call TI</td>
<td>-40 to 125</td>
<td></td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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