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THVD1424 3-V to 5.5-V RS-485 Transceiver With Slew Rate Control, Integrated 120-Ohm Switchable Termination Resistor and Duplex Switching

1 Features

- Meets or exceeds the requirements of the TIA/EIA-485A standard
- 3-V to 5.5-V bus supply voltage
- 1.65 V to 5.5 V supply for logic signals
- Differential output exceeds 2.1 V for PROFIBUS compatibility with 5-V supply
- Pin configurable Half-duplex and full-duplex
- Pin controlled on-chip 120 Ω termination resistor on bus pins
- Maximum Data rate configurable
  - SLR = High: 500 kbps
  - SLR = Low or floating: 20 Mbps
- Bus I/O protection
  - ±16-kV HBM ESD
  - ±8-kV IEC 61000-4-2 Contact discharge
  - ±15-kV IEC 61000-4-2 Air gap discharge
  - ±4-kV IEC 61000-4-4 Fast transient burst
  - ±16-V bus fault protection (absolute max voltage on bus pins)
- Extended industrial temperature range: -40°C to 125°C
- Low power consumption
  - Shutdown supply current < 5 µA
  - Quiescent current during operation < 3 mA
- Glitch-free power-up/power-down for hot plug-in capability
- Open, short, and idle bus failsafe
- Small, space-saving 16-VQFN (3 mm x 3 mm) package

2 Applications

- Factory automation & control
- Building automation
- Industrial transport
- HVAC systems
- Smart meters
- Lighting
- Grid Infrastructure

3 Description

The THVD1424 is a flexible RS-485 transceiver for industrial applications. The device has features such as on-chip 120-Ω termination resistor, slew rate control and interchangeability between half and full duplex mode. All the features are pin-controlled. This enables the device to be used at any node location (end nodes or middle nodes) in any network, two-wire (half duplex) or 4-wire (full duplex), slow or fast. End-equipment designers can now design a common printed circuit board (PCB) and configure it via software for various application needs. This can save considerable design and qualification time for the customers.

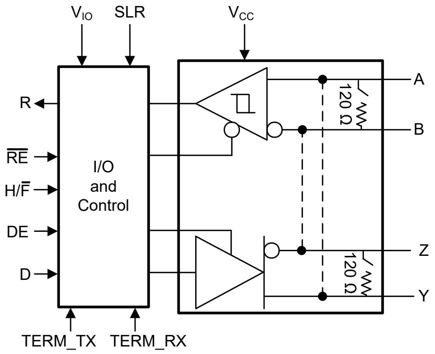
The bus pins are immune to high levels of IEC Contact Discharge ESD events, eliminating the need for additional system level protection components. The device operates from 3 to 5.5-V bus supply, while the logic supply voltage range is 1.65 V to 5.5 V. The wide common-mode voltage range and low input leakage on bus pins makes the devices suitable for multi-point applications over long cable runs.

The device is available in a space-saving, thermally efficient 16-pin VQFN package. The device is characterized for ambient temperatures from –40°C to 125°C.

Package Information

PART NUMBER	PACKAGE[1]	BODY SIZE (NOM)
THVD1424	VQFN (16)	3 mm x 3 mm

(1) For the complete part number, see the orderable addendum at the end of the data sheet.



Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 2022) to Revision A (March 2023)	Page
• Changed Figure 9-2	19

5 Pin Configuration and Functions

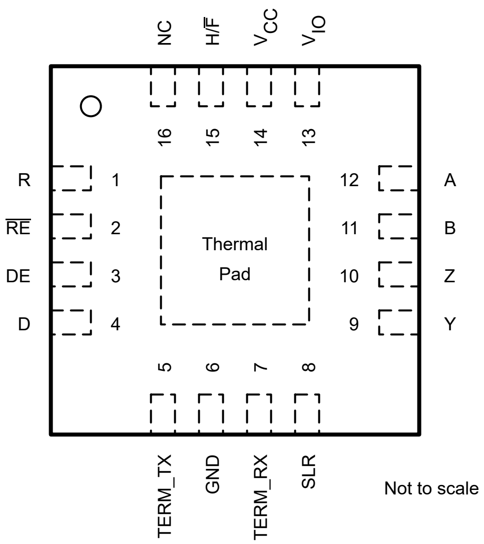


Figure 5-1. VQFN (RGT) Package, 16-Pins (Top View)

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
R	1	Digital output	Logic output RS485 data
RE̅	2	Digital input	Receiver enable/disable. Internal pull-up. Receiver disabled by default
DE	3	Digital input	Driver enable/disable. Internal pull-down. Driver disabled by default
D	4	Digital input	Logic input RS485 data. Internal pull-up. Drives the bus high by default if driver is enabled
TERM_TX	5	Digital input	120 Ω on-chip termination control for Y/Z pins. Internal pull-down. Termination across Y/Z is disabled by default
GND	6	GND	Ground
TERM_RX	7	Digital input	120 Ω on-chip termination control for A/B pins. Internal pull-down. Termination across A/B is disabled by default
SLR	8	Digital input	Slew rate control. Internal pull-down, default 20 Mbps operation. Logic high SLR enables slow speed (500 kbps)
Y	9	Bus input/output	RS485 bus pins. In full duplex, this pin is non-inverting driver output. In half duplex, this is non-inverting driver output and non-inverting receiver input
Z	10	Bus input/output	RS485 bus pins. In full duplex, this pin is inverting driver output. In half duplex, this is inverting driver output and inverting receiver input
B	11	Bus input	RS485 receiver inverting input pin in full duplex mode
A	12	Bus input	RS485 receiver non-inverting input pin in full duplex mode
V_{IO}	13	Supply	1.65 to 5.5 V logic supply voltage
V_{CC}	14	Supply	3 to 5.5V supply voltage
H/F̅	15	Digital input	Half to full duplex control. Internal pull-down, so full duplex by default- Y/Z are driver output, A/B are receiver input pins
NC	16	No connect	Not connected internally
Thermal pad		--	Connect to GND for optimal thermal and electrical performance

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

		MIN	MAX	UNIT
Bus supply voltage	V_{CC}	–0.5	7	V
Logic supply voltage	V_{IO}	–0.5	V_{CC} + 0.2	V
Bus voltage	Voltage at any bus pin (Y, Z, A or B) with respect to GND	–16	16	V
Differential bus voltage	(Y-Z) or (Z-Y), (A-B) or (B-A) with termination enabled	-6	6	V
Input voltage	Range at any logic pin (D, DE, SLR, TERM_TX, TERM_RX, H/$\overline{F}$ or $\overline{RE}$)	–0.3	V_{IO} + 0.2	V
Receiver output current	I_O	–24	24	mA
Storage temperature	T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values, except differential I/O bus voltages, are with respect to ground terminal.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Bus terminals (Y, Z, A, B) and GND	±16,000	V
			All pins except bus terminals and GND	±4,000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1,500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings [IEC]

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge, Device configured as either half duplex or Full duplex, on chip termination ON or OFF	Contact discharge, per IEC 61000-4-2	Bus terminals and GND	±8,000	V
		Air-gap discharge, per IEC 61000-4-2	Bus terminals and GND	±15,000	
$V_{(EFT)}$	Electrical fast transient	Per IEC 61000-4-4	Bus terminals	±4,000	V

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3		5.5	V
V_{IO}	I/O supply voltage		1.65		V_{CC}	V
V_I	Input voltage at any bus terminal (separately or common mode)(1)		–7		12	V
V_{IH}	High-level input voltage (D, DE, $\overline{RE}$, TERM_TX, TERM_RX, SLR, H/$\overline{F}$ inputs)		$0.7{*}V_{IO}$		V_{IO}	V
V_{IL}	Low-level input voltage (D, DE, $\overline{RE}$, TERM_TX, TERM_RX, SLR, H/$\overline{F}$ inputs)		0		$0.3{*}V_{IO}$	V
I_O	Output current, driver		–60		60	mA
I_{OR}	Output current, receiver	V_{IO} = 1.8 V or 2.5 V	–4		4	mA
I_{OR}	Output current, receiver	V_{IO} = 3.3 V or 5 V	–8		8	mA
R_L	Differential load resistance		54	60		Ω
$1/t_{UI}$	Signaling rate	SLR = V_{IO}			500	kbps
		SLR = GND or floating			20	Mbps
T_A ((2))	Operating ambient temperature		-40		125	°C
T_J (2)	Junction temperature		-40		150	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.
(2) Operation is specified for internal (junction) temperatures up to 150°C. Self-heating due to internal power dissipation should be considered for each application. Maximum junction temperature is internally limited by the thermal shut-down (TSD) circuit which disables the driver and receiver when the junction temperature reaches typical 170°C.

6.5 Thermal Information

THERMAL METRIC(1)		THVD1424	UNIT
		RGT (QFN)	
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	46.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	20.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.9	°C/W

(1) For more information about traditional and new thermal metrics, see the yes application report.

6.6 Power Dissipation

PARAMETER		TEST CONDITIONS			Typical	Max	UNIT
P_D	Driver and receiver enabled, external loopback by A connected to Y, B connected to Z V_{IO} = V_{CC} = 5.5 V, T_A = 125 °C, D = square wave 50% duty	Unterminated, TERM_TX = L, TERM_RX = L	SLR = H	500 kbps	185	210	mW
			SLR = L	20Mbps	310	340	
		TERM_RX = H, With 120 Ω load between A/B inputs	SLR = H	500 kbps	316	360	mW
			SLR = L	20Mbps	396	430	
		TERM_TX = TERM_RX = H; With 120 Ω between Y/Z outputs and A/B inputs, C_L = 50 pF (driver)	SLR = H	500 kbps	407	470	mW
			SLR = L	20Mbps	476	510	

6.7 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of V_{CC} = 5 V, V_{IO} = 3.3 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
$\vert V_{OD}\vert$	Driver differential output voltage magnitude	R_L = 60 Ω, –7 V ≤ V_{test} ≤ 12 V (See Figure 7-1)		1.5	3.3		V
		R_L = 60 Ω, –7 V ≤ V_{test} ≤ 12 V, 4.5 V ≤ V_{CC} ≤ 5.5 V (See Figure 7-1)		2.1	3.3		V
		R_L = 100 Ω (See Figure 7-2)		2	4		V
		R_L = 54 Ω, 4.5 V ≤ V_{CC} ≤ 5.5 V (See Figure 7-2)		2.1	3.3		V
		R_L = 54 Ω (See Figure 7-2)		1.5	3.3		V
$\Delta\vert V_{OD}\vert$	Change in magnitude of differential output voltage	R_L = 54 Ω or 100 Ω (See Figure 7-2)		–50		50	mV
V_{OC}	Common-mode output voltage	R_L = 54 Ω or 100 Ω (See Figure 7-2)			$V_{CC}/2$	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage	R_L = 54 Ω or 100 Ω (See Figure 7-2)		–50		50	mV
I_{OS}	Short-circuit output current	DE = V_{IO}, -7 V ≤ (V_Y or V_Z) ≤ 12 V, or Y shorted to Z		–250		250	mA
I_{OZD}	Driver High impedance output leakage current on Y an Z in Full duplex mode	H/$\overline{F}$ = GND, TERM_TX = GND, DE = GND, V_{CC} = GND or 5.5V, V_O = -7V, +12V		-100		110	μA
		H/$\overline{F}$ = GND, TERM_TX = V_{IO}, DE = GND, V_{CC} = 5.5V, V_O = -7V, +12V		- 300		300	μA
Receiver							
I_I	Bus input current (termination disabled)	DE = 0 V, V_{CC} and V_{IO} = 0 V or 5.5 V	V_I = 12 V		85	110	μA
			V_I = –7 V	–100	–70		μA
I_{RXT}	Receiver bus input leakage current with termination enabled	DE = 0 V, V_{CC} and V_{IO} = 5.5 V, TERM_RX = V_{IO}	VI = - 7 to 12 V	-300		300	μA
V_{TH+}	Positive-going input threshold voltage(1)	Over common-mode range of - 7 V to 12 V			- 85	- 45	mV
V_{TH-}	Negative-going input threshold voltage(1)			–200	–135		mV
V_{HYS}	Input hysteresis			30	50		mV
$C_{A,B}$	Input differential capacitance	Measured between A and B, f = 1 MHz			20		pF
V_{OH}	Output high voltage	I_{OH} = –8 mA, V_{IO} = 3 to 3.6 V or 4.5 V to 5.5 V		V_{IO} – 0.4	V_{IO} – 0.2		V
V_{OL}	Output low voltage	I_{OL} = 8 mA, V_{IO} = 3 to 3.6 V or 4.5 V to 5.5 V			0.2	0.4	V
V_{OH}	Output high voltage	I_{OH} = –4 mA, V_{IO} = 1.65 to 1.95 V or 2.25 V to 2.75 V		V_{IO} – 0.4	V_{IO} – 0.2		V
V_{OL}	Output low voltage	I_{OL} = 4 mA, V_{IO} = 1.65 to 1.95 V or 2.25 V to 2.75 V			0.2	0.4	V
I_{OZ}	Output high-impedance current, R pin	V_O = 0 V or V_{IO}, $\overline{RE}$ = V_{IO}		–2		2	μA
Logic							
I_{IN}	Input current (D, $\overline{RE}$, DE , SLR, TERM_TX, TERM_RX, H/$\overline{F}$)	1.65 V ≤ V_{IO} ≤ 5.5 V, 0 V ≤ V_{IN} ≤ V_{IO}		-5		5	μA
Thermal Protection							
T_{SHDN}	Thermal shutdown threshold	Temperature rising		150	170		°C
T_{HYS}	Thermal shutdown hysteresis				15		°C
Supply							
UV_{VCC} (rising)	Rising under-voltage threshold on V_{CC}				2.5	2.7	V
UV_{VCC} (falling)	Falling under-voltage threshold on V_{CC}			2	2.1		V
$UV_{VCC(hys)}$	Hysteresis on under-voltage of V_{CC}				400		mV
UV_{VIO} (rising)	Rising under-voltage threshold on V_{IO}				1.5	1.6	V

6.7 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of V_{CC} = 5 V, V_{IO} = 3.3 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
UV_{VIO} (falling)	Falling under-voltage threshold on V_{IO}			1.3	1.4		V
$UV_{VIO(hys)}$	Hysteresis on under-voltage of V_{IO}				100		mV
I_{CC}	Supply current (quiescent), V_{CC} = 4.5 V to 5.5 V TERM_RX, TERM_TX= Floating or low, SLR = X	Driver and receiver enabled, H/$\overline{\text{F}}$ = GND	$\overline{\text{RE}}$ = 0 V, DE = V_{IO}, No load		1.5	3	mA
		Driver enabled, receiver disabled, H/$\overline{\text{F}}$ = GND	$\overline{\text{RE}}$ = V_{IO}, DE = V_{IO}, No load		1.3	2.5	mA
		Driver disabled, receiver enabled, H/$\overline{\text{F}}$ = GND	$\overline{\text{RE}}$ = 0 V, DE = 0 V, No load		0.8	1.2	mA
		Driver and receiver disabled, H/$\overline{\text{F}}$ = GND	$\overline{\text{RE}}$ = V_{IO}, DE = 0 V, D = open, No load		0.1	2	µA
I_{CC}	Supply current (quiescent), V_{CC} = 3 V to 3.6 V TERM_RX, TERM_TX= Floating or low, SLR = X	Driver and receiver enabled, H/$\overline{\text{F}}$ = GND	$\overline{\text{RE}}$ = 0 V, DE = V_{IO}, No load		1.4	2	mA
		Driver enabled, receiver disabled, H/$\overline{\text{F}}$ = GND	$\overline{\text{RE}}$ = V_{IO}, DE = V_{IO}, No load		1	1.5	mA
		Driver disabled, receiver enabled, H/$\overline{\text{F}}$ = GND	$\overline{\text{RE}}$ = 0 V, DE = 0 V, No load		0.7	1	mA
		Driver and receiver disabled, H/$\overline{\text{F}}$ = GND	$\overline{\text{RE}}$ = V_{IO}, DE = 0 V, D = open, No load		0.1	2	µA
I_{IO}	Logic supply current (quiescent), V_{IO} = 3 to 3.6 V TERM_RX, TERM_TX= Floating or low	Driver disabled, Receiver enabled, SLR = GND	DE = 0 V, $\overline{\text{RE}}$ = 0 V, No load		6	11	µA
		Driver disabled, Receiver enabled, SLR = V_{IO}	DE = 0 V, $\overline{\text{RE}}$ = 0 V, No load		8	11	µA
		Driver disabled, Receiver disabled, SLR = GND	DE = 0 V, $\overline{\text{RE}}$ = V_{IO}, No load		2	4	µA
		Driver disabled, Receiver disabled, SLR = V_{IO}	DE = 0 V, $\overline{\text{RE}}$ = V_{IO}, No load		4	7	µA
I_{CCDT}	Supply current in driver termination mode	Driver enabled with termination ON, H/$\overline{\text{F}}$ = GND	DE= V_{IO}, TERM_TX = V_{IO}		39	48	mA
I_{CCRT}	Supply current in receiver termination mode	Receiver enabled with termination ON, H/$\overline{\text{F}}$ = GND	$\overline{\text{RE}}$ = GND, TERM_RX = V_{IO}		1	1.3	mA
I_{CCT}	Supply current in device disabled, termination ON mode	Driver and receiver disabled, H/$\overline{\text{F}}$ = GND	DE= GND, $\overline{\text{RE}}$ = V_{IO}, TERM_RX = V_{IO}		200	310	µA
On-Chip termination resistor							
R_{TERM_TX}	120 Ω termination across Driver output Y/Z terminals	DE = GND, TERM_TX = V_{IO}, V_{YZ} = 2 V, V_Z = -7 V, 0 V, 10 V See Figure 7-9		102	120	138	Ω
R_{TERM_RX}	120 Ω termination across receiver output A/B terminals	TERM_RX = V_{IO}, V_{AB} = 2 V, V_B = -7 V, 0 V, 10 V See Figure 7-10		102	120	138	Ω

(1) Under any specific conditions, V_{TH+} is assured to be at least V_{HYS} higher than V_{TH-}.

6.8 Switching Characteristics_500 kbps

500-kbps (with SLR = V_{IO}) over recommended operating conditions. All typical values are at 25°C and supply voltage of V_{CC} = 5 V, V_{IO} = 3.3 V, unless otherwise noted. ((1))

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
t_r, t_f	Differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF See Figure 7-3	V_{CC} = 3 to 3.6 V, Typical at 3.3V	200	250	600	ns
			V_{CC} = 4.5 to 5.5 V, Typical at 5 V	220	270	600	ns
t_{PHL}, t_{PLH}	Propagation delay		V_{CC} = 3 to 3.6 V, Typical at 3.3V		260	500	ns
			V_{CC} = 4.5 to 5.5 V, Typical at 5 V		260	450	ns
$t_{SK(P)}$	Pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$		V_{CC} = 3 to 3.6 V, Typical at 3.3V		2	15	ns
			V_{CC} = 4.5 to 5.5 V, Typical at 5 V		2	15	ns
t_{PHZ}, t_{PLZ}	Disable time	$\overline{RE}$ = X	See Figure 7-4 and Figure 7-5		80	200	ns
t_{PZH}, t_{PZL}	Enable time	$\overline{RE}$ = 0 V			200	650	ns
		$\overline{RE}$ = V_{IO}			6	11	μs
Receiver							
t_r, t_f	Output rise/fall time	C_L = 15 pF	See Figure 7-6		5	20	ns
t_{PHL}, t_{PLH}	Propagation delay				620	1200	ns
$t_{SK(P)}$	Pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$				10	40	ns
t_{PHZ}, t_{PLZ}	Disable time	DE = X	See Figure 7-7		20	60	ns
$t_{PZH(1)}$	Enable time	DE = V_{IO}			80	155	ns
$t_{PZL(1)}$	Enable time	DE = V_{IO}			650	1250	ns
$t_{PZH(2)}$, $t_{PZL(2)}$	Enable time	V_{IO} = 1.65 V to 1.95 V; DE = 0 V	See Figure 7-8		7	12	μs
		V_{IO} = 3 V to 3.6 V; DE = 0 V			7	12	

(1) A, B are RX input, Y/Z are driver output terminals in Full duplex mode

6.9 Switching Characteristics_20 Mbps

20-Mbps (SLR = GND) over recommended operating conditions. All typical values are at 25°C and supply voltage of V_{CC} = 5 V, V_{IO} = 3.3 V. ((1))

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
t_r, t_f	Differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF See Figure 7-3	V_{CC} = 3 to 3.6 V, Typical at 3.3 V	5	9	15	ns
			V_{CC} = 4.5 to 5.5 V, Typical at 5 V	4.5	8	15	ns
t_{PHL}, t_{PLH}	Propagation delay		V_{IO} = 1.65 V to 1.95V	14	25	50	ns
			V_{IO} = 3 V to 3.6 V	9	20	40	ns
$t_{SK(P)}$	Pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$		V_{CC} = 3 to 3.6 V, Typical at 3.3 V		1	3.5	ns
			V_{CC} = 4.5 to 5.5 V, Typical at 5 V		1	3.5	ns
t_{PHZ}, t_{PLZ}	Disable time	$\overline{RE}$ = X	See Figure 7-4 and Figure 7-5		25	50	ns
t_{PZH}, t_{PZL}	Enable time	$\overline{RE}$ = 0 V	See Figure 7-4 and Figure 7-5		30	70	ns
t_{PZH}, t_{PZL}	Enable time	$\overline{RE}$ = V_{IO} , V_{IO} = 1.65 V to 1.95 V	See Figure 7-4 and Figure 7-5		6	11	μs
		$\overline{RE}$ = V_{IO} , V_{IO} = 3 V to 3.6 V			6	11	
Receiver							

6.9 Switching Characteristics_20 Mbps (continued)

20-Mbps (SLR = GND) over recommended operating conditions. All typical values are at 25°C and supply voltage of V_{CC} = 5 V, V_{IO} = 3.3 V. ((1))

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_r, t_f	Output rise/fall time	C_L = 15 pF	See Figure 7-6		5	10	ns
t_{PHL}, t_{PLH}	Propagation delay				30	55	ns
$t_{SK(P)}$	Pulse skew, $\|t_{PHL} – t_{PLH}\|$					4	ns
t_{PHZ}, t_{PLZ}	Disable time	DE = X	See Figure 7-7		20	58	ns
$t_{PZH(1)}$, $t_{PZL(1)}$	Enable time	DE = V_{IO}			80	155	ns
$t_{PZH(2)}$, $t_{PZL(2)}$	Enable time	V_{IO} = 1.65 V to 1.95 V; DE = 0 V	See Figure 7-8		6	11	µs
		V_{IO} = 3 V to 3.6 V; DE = 0 V			6	11	µs

(1) A, B are RX input, Y/Z are driver output terminals in Full duplex mode.

6.10 Switching Characteristics_Termination resistor

Parameters over recommended operating conditions. All typical values are at 25°C and supply voltage of V_{CC} = 5 V, V_{IO} = 3.3 V, unless otherwise noted.

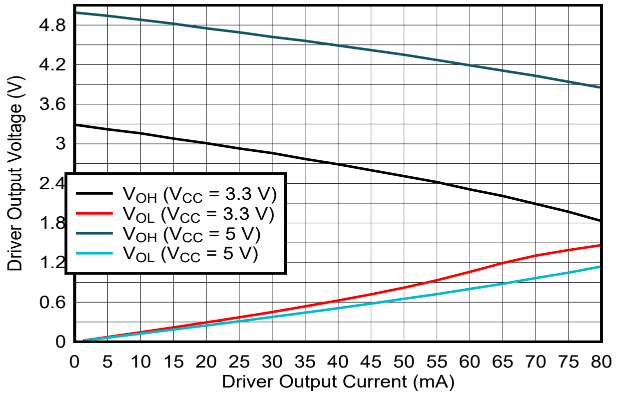
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DTEN}	Driver terminal Termination resistor turn-on time	$H/\overline{F}$ = GND, V_{IO} = 3 to 3.6 V, DE = GND, V_{YZ} = 2 V, V_Z = 0 V See Figure 7-9		1500	4000	ns
t_{DTZ}	Driver terminal Termination resistor turn-off time	$H/\overline{F}$ = GND, V_{IO} = 3 to 3.6 V, DE = GND, V_{YZ} = 2 V, V_Z = 0 V See Figure 7-9		4600	7200	ns
t_{RTEN}	Receiver terminal Termination resistor turn-on time	$H/\overline{F}$ = GND, V_{IO} = 3 to 3.6 V, $\overline{RE}$ = X, V_{AB} = 2 V, V_B = 0 V See Figure 7-10		1500	4000	ns
t_{RTZ}	Receiver terminal Termination resistor turn-off time	$H/\overline{F}$ = GND, V_{IO} = 3 to 3.6 V, $\overline{RE}$ = X, V_{AB} = 2 V, V_B = 0 V See Figure 7-10		4600	7200	ns

6.11 Switching Characteristics_Duplex switching

Parameters over recommended operating conditions. All typical values are at 25°C and supply voltage of V_{CC} = 5 V, V_{IO} = 3.3 V, unless otherwise noted.

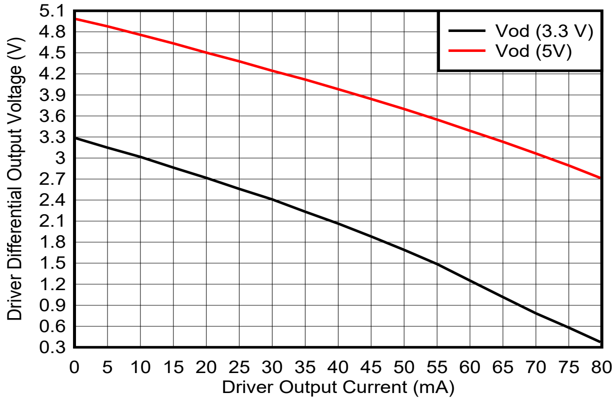
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{HFD}	Time to switch from half to full duplex mode	V_{IO} = 3 to 3.6 V, Driver and receiver enabled, TERM_TX = V_{IO} See Figure 7-11		0.1	1.2	µs
t_{FHD}	Time to switch from full to half duplex mode	V_{IO} = 3 to 3.6 V, Driver and receiver enabled, TERM_TX = V_{IO} See Figure 7-11		0.1	1.2	µs

6.12 Typical Characteristics



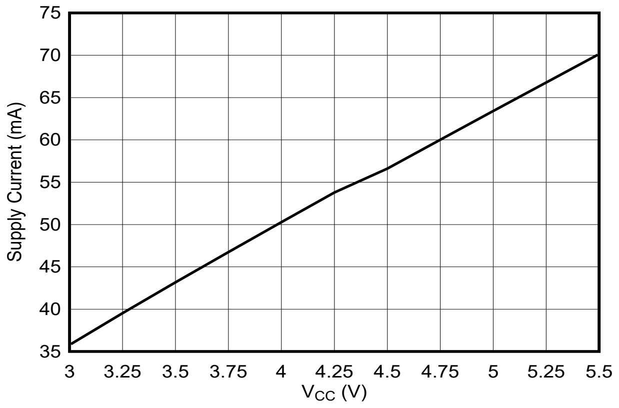
DE = V_{IO} T_A = 25°C

Figure 6-1. Driver Output voltage vs Driver Output Current



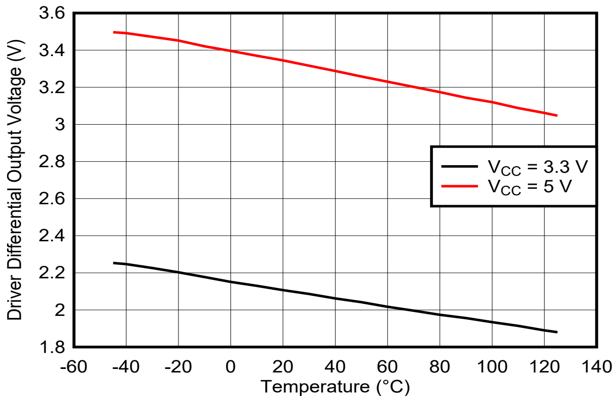
DE = V_{IO} T_A = 25°C

Figure 6-2. Driver Differential Output voltage vs Driver Output Current



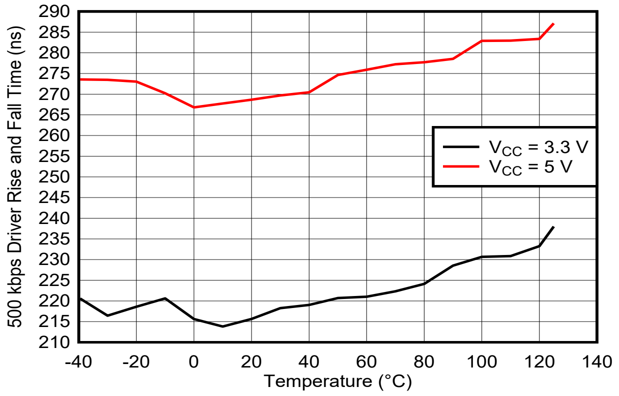
R_L = 54 Ω DE = V_{IO} D = V_{IO}
T_A = 25°C

Figure 6-3. Supply Current vs Supply Voltage



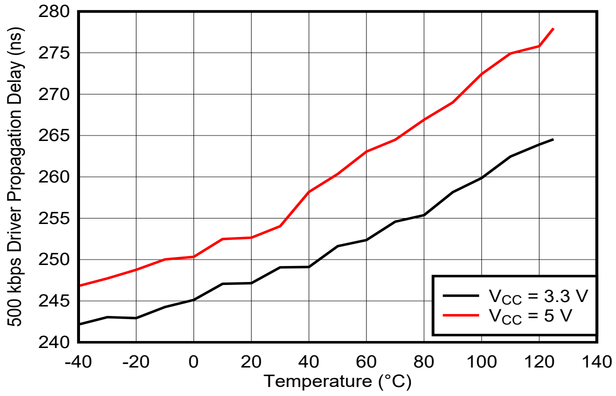
R_L = 54 Ω DE = V_{IO} D = V_{IO}

Figure 6-4. Driver Output Voltage vs Temperature



R_L = 54 Ω C_L = 50 pF DE = V_{IO}

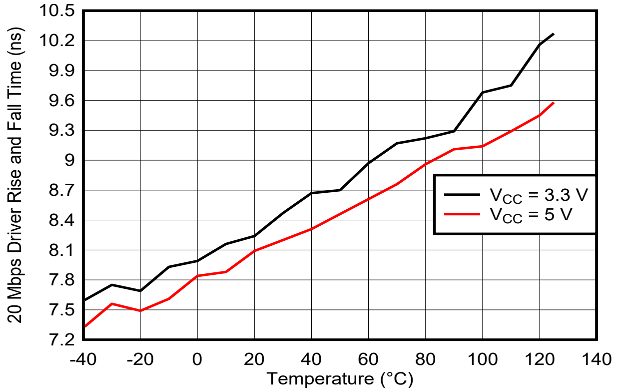
Figure 6-5. Driver Rise or Fall Time vs Temperature (500 kbps)



R_L = 54 Ω C_L = 50 pF DE = V_{IO}

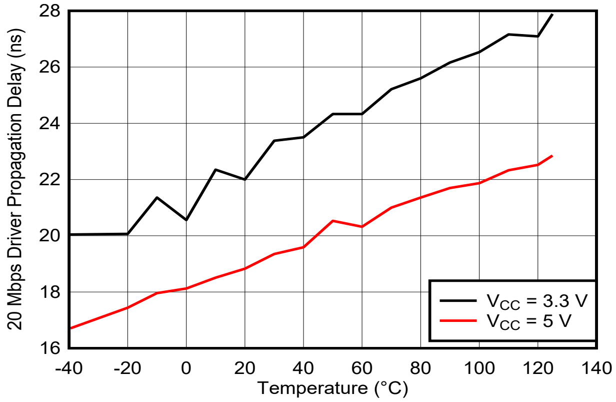
Figure 6-6. Driver Propagation Delay vs Temperature (500 kbps)

6.12 Typical Characteristics (continued)



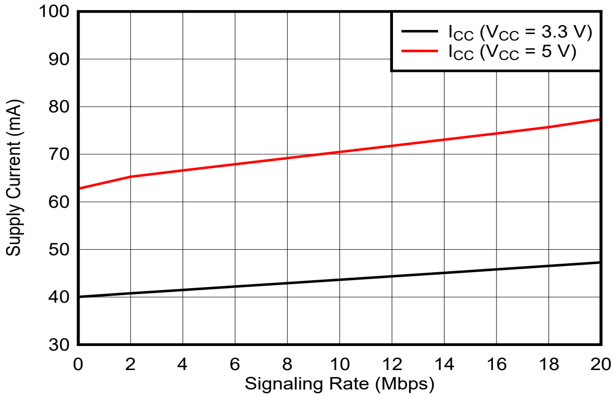
R_L = 54 Ω C_L = 50 pF DE = V_{IO}

Figure 6-7. Driver Rise or Fall Time vs Temperature (20 Mbps)



R_L = 54 Ω C_L = 50 pF DE = V_{IO}

Figure 6-8. Driver Propagation Delay vs Temperature (20 Mbps)



R_L = 54 Ω T_A = 25 °C

DE = V_{IO}

Figure 6-9. Supply Current vs Signal Rate (20 Mbps)

7 Parameter Measurement Information

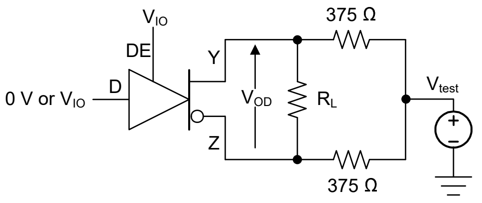


Figure 7-1. Measurement of Driver Differential Output Voltage With Common-Mode Load

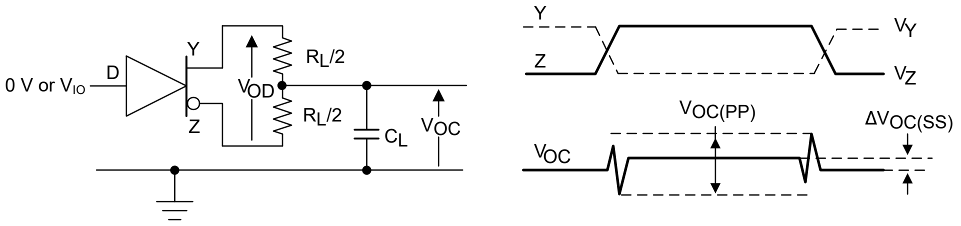


Figure 7-2. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

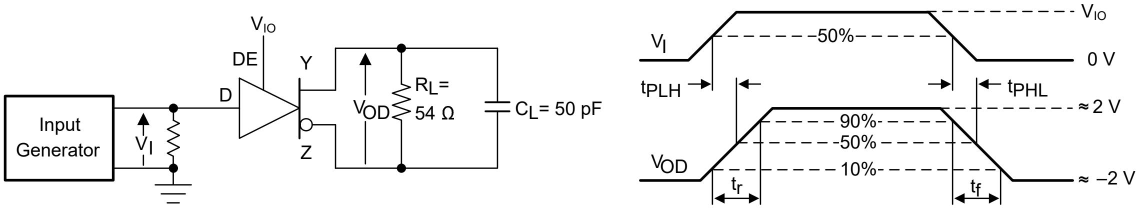


Figure 7-3. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays

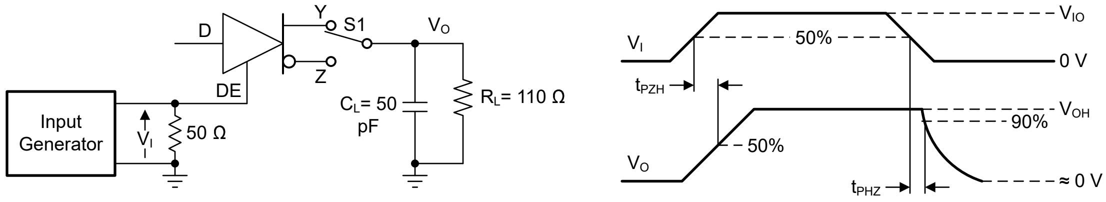


Figure 7-4. Measurement of Driver Enable and Disable Times With Active High Output and Pull-Down Load

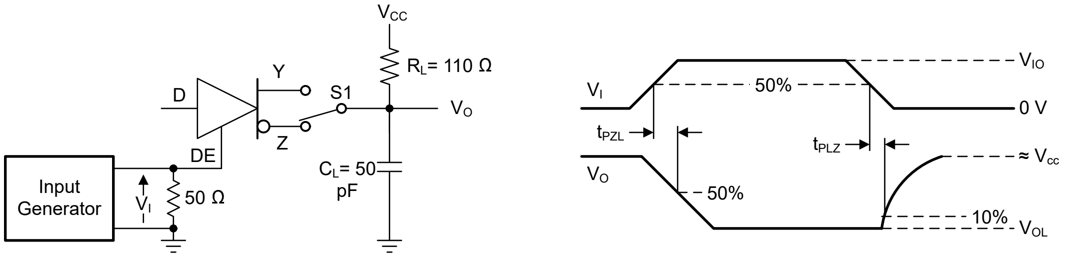


Figure 7-5. Measurement of Driver Enable and Disable Times With Active Low Output and Pull-up Load

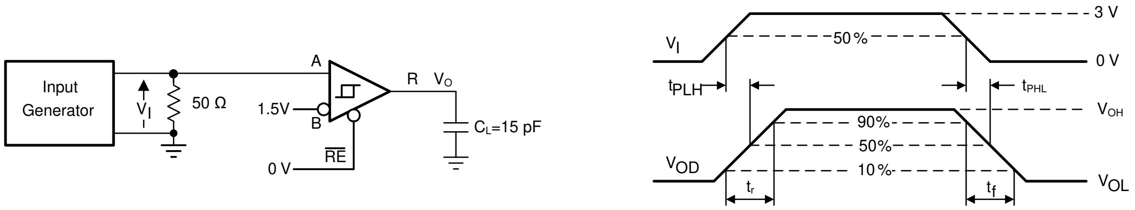


Figure 7-6. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

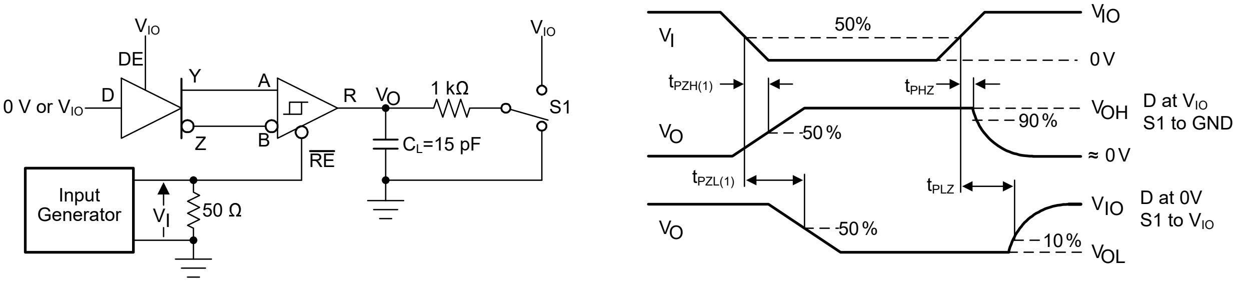


Figure 7-7. Measurement of Receiver Enable/Disable Times With Driver Enabled

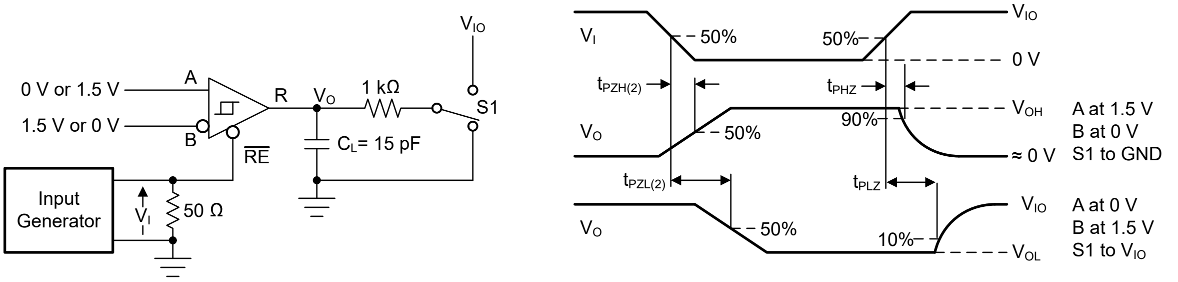


Figure 7-8. Measurement of Receiver Enable Times With Driver Disabled

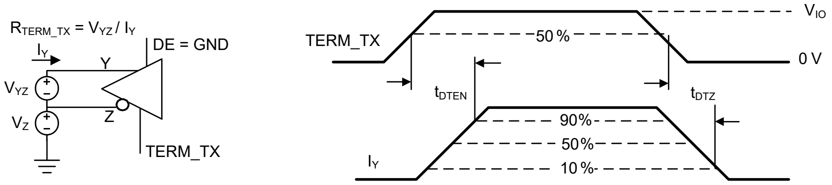


Figure 7-9. Measurement of Enable and Disable times of Driver Terminal Termination Resistor

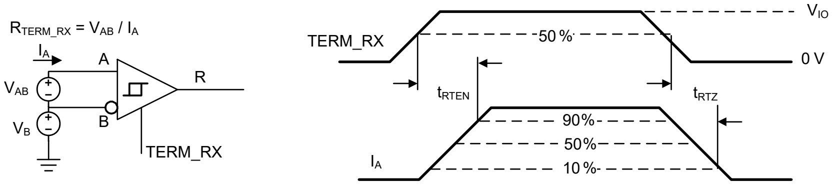


Figure 7-10. Measurement of Enable and Disable times of Receiver Terminal Termination Resistor

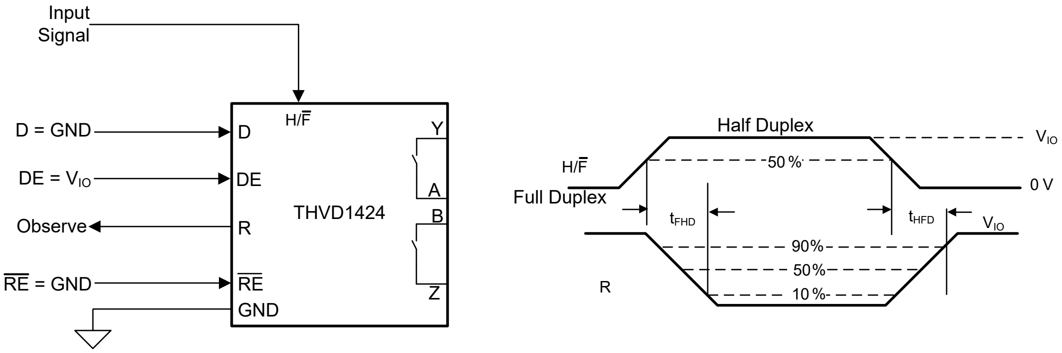


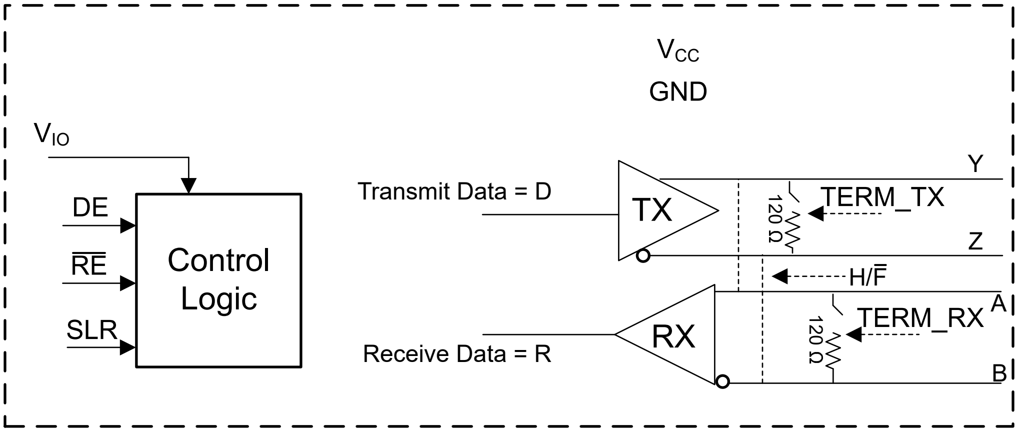
Figure 7-11. Measurement of Time to Switch from Half duplex mode to Full duplex mode and vice versa

8 Detailed Description

8.1 Overview

The THVD1424 is a flexible RS-485 transceiver which can be used in half-duplex or full-duplex RS-485 networks by configuring the pin H/$\overline{F}$. The device has slew rate control pin SLR which can be used to set the device in maximum 20 Mbps mode or slew rate limited 500 kbps mode. THVD1424 also has on-chip 120 Ω termination resistor across Y/Z terminals and also across A/B terminals. Termination resistors are controlled using two pins TERM_TX and TERM_RX.

8.2 Functional Block Diagrams



8.3 Feature Description

The THVD1424 operates from 3 to 5.5V bus supply. The device has a V_{IO} pin which allows it to interface to 1.8 V, 2.5 V, 3.3 V or 5 V logic interface. Internal ESD protection circuits protect the transceiver against Electrostatic Discharges (ESD) according to IEC 61000-4-2 of up to ±8 kV (Contact Discharge), ±15 kV (Air Gap Discharge) and against electrical fast transients (EFT) according to IEC 61000-4-4 of up to ±4 kV.

8.4 Device Functional Modes

THVD1424 has H/$\overline{F}$ pin which allows it to be used in half-duplex or full duplex networks. Functional operation of H/$\overline{F}$ pin is described in table.

Table 8-1. Duplex switching function table

Signal state	Driver	Receiver	Comment
H/$\overline{F}$ = V_{IO}	Driver output pins are Y and Z	Receiver input pins are Y and Z	Half duplex mode: Driver and receiver share same bus pins, and device state is controlled by DE and $\overline{RE}$ pins
H/$\overline{F}$ = GND	Driver output pins are Y and Z	Receiver input pins are A and B	Full duplex mode: This is the default state of the device in case H/$\overline{F}$ is floating.

When the driver enable pin, DE, is logic high, the differential outputs Y and Z follow the logic states at data input D. A logic high at D causes Y to turn high and Z to turn low. In this case, the differential output voltage defined as $V_{OD} = V_Y – V_Z$ is positive. When D is low, the output states reverse, Z turns high, Y becomes low, and V_{OD} is negative.

When DE is low, both outputs turn high-impedance. In this condition, the logic state at D is irrelevant. The DE pin has an internal pull-down resistor to ground; thus, when left open, the driver is disabled (high-impedance) by default. The D pin has an internal pull-up resistor to V_{IO}, thus, when left open while the driver is enabled, output Y turns high and Z turns low.

Table 8-2. Driver Function Table

INPUT	ENABLE	OUTPUTS		FUNCTION
D	DE	Y	Z	
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus high by default

When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A – V_B$ in case of full duplex mode (or V_Y - V_Z in case of half duplex mode) is positive and higher than the positive input threshold, V_{TH+}, the receiver output, R, turns high. When V_{ID} is negative and lower than the negative input threshold, V_{TH-}, the receiver output, R, turns low. If V_{ID} is between V_{TH+} and V_{TH-}, the output is indeterminate.

When $\overline{RE}$ is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output R to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

Table 8-3. Receiver Function Table

DIFFERENTIAL INPUT	ENABLE	OUTPUT	FUNCTION
$V_{ID} = V_A – V_B$ (full duplex mode) or $V_Y – V_Z$ (half duplex mode)	$\overline{RE}$	R	
$V_{TH+} < V_{ID}$	L	H	Receive valid bus high
$V_{TH-} < V_{ID} < V_{TH+}$	L	?	Indeterminate bus state
$V_{ID} < V_{TH-}$	L	L	Receive valid bus low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

8.4.1 On-Chip Switchable Termination

THVD1424 has 2 termination resistors of nominal 120 Ω, one across Y/Z and another across A/B. Both termination resistors are enabled or disabled using pins as described in On-chip termination function table. Both the termination resistors can be enabled or disabled independent of the state of driver or receiver. Termination is OFF if the device is unpowered or in thermal shutdown.

Table 8-4. On-chip termination function table

Signal state	Device mode	Function	Comments
TERM_TX = V_{IO}	Full duplex mode	120 Ω enabled between Y and Z	Termination between Y/Z is disabled by default
TERM_TX = GND or floating	Full duplex mode	120 Ω disabled between Y and Z	
TERM_RX = V_{IO}	Full duplex mode	120 Ω enabled between A and B	Termination between A/B is disabled by default
TERM_RX = GND or floating	Full duplex mode	120 Ω disabled between A and B	
TERM_RX = X, TERM_TX = V_{IO}	Half duplex mode	120 Ω enabled between Y and Z	In half duplex mode, TERM_RX is don't care and TERM_TX has higher priority
TERM_RX = X, TERM_TX = GND	Half duplex mode	120 Ω disabled between Y and Z	

On-chip 120 Ω termination resistor variation with temperature and across common mode voltage is shown in following images.

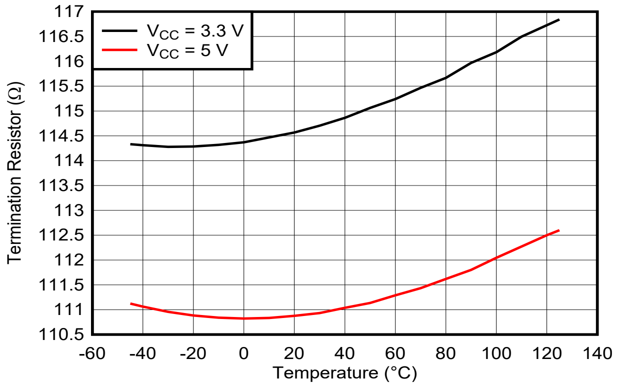


Figure 8-1. Termination resistor vs Temperature

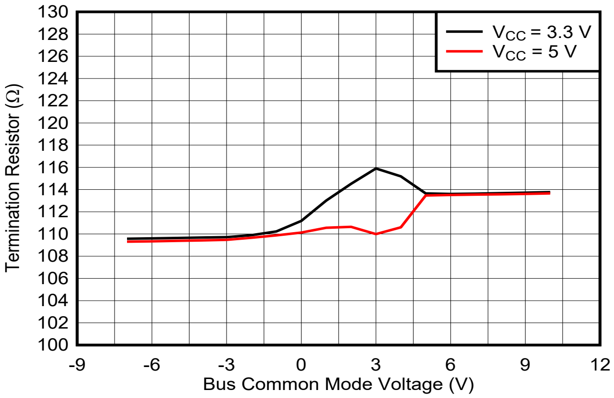


Figure 8-2. Termination resistor vs Bus common mode voltage

THVD1424 on-chip termination resistor has been designed so the termination block offers a resistive load to the bus, and does not alter the magnitude or phase of the bus signals from DC to 20 Mbps signaling. See the following images with the bus voltage swept from -6 V to +6 V. Current into the bus changes linearly in both conditions of termination ON or OFF.

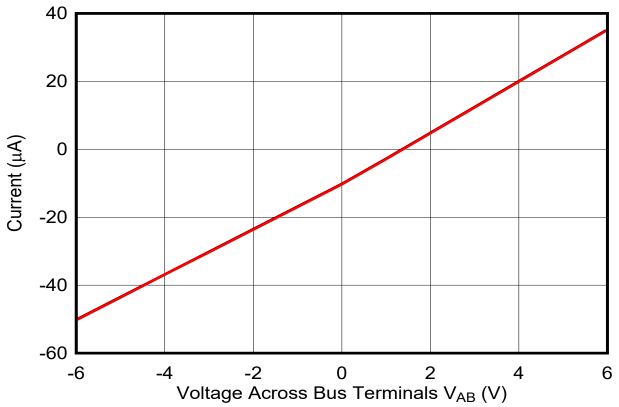


Figure 8-3. Voltage vs Current across AB bus pins with termination OFF

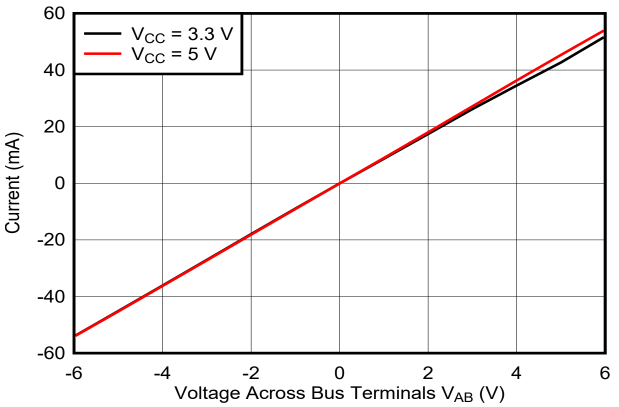


Figure 8-4. Voltage vs Current across AB bus pins with termination ON

8.4.2 Operational Data rate

THVD1424 can be used in slow speed or fast speed RS-485 networks by configuring Slew rate control (SLR) pin. Table below describes slew rate control function.

Table 8-5. Slew rate control function table

Signal state	Driver	Receiver	Comment
SLR = V_{IO}	Maximum speed of operation = 500kbps	Maximum speed of operation = 500kbps	Active high slew rate limiting applied on driver output and glitch filter in receiver path enabled
SLR = GND or floating	Maximum speed of operation = 20Mbps	Maximum speed of operation = 20Mbps	Slew rate limiting on driver output disabled and glitch filter in receiver path disabled

Receiver path in the slow speed mode (500 kbps) provides additional noise filtering. To attenuate high frequency noise pulses from the bus which can be wrongly interpreted as valid data, SLR = V_{IO} enables a low pass filter to filter out pulses with frequency higher than typical 800 kHz.

8.4.3 Protection Features

THVD1424 has in-built protection features such as supply undervoltage, bus short circuit and thermal shutdown.

Supply undervoltage protection is present on both V_{CC} and V_{IO} supplies. This maintains the bus output and receiver logic output in known driven state when both the supplies are above their rising undervoltage thresholds. Table below describes the device behavior in various scenarios of supply levels.

Table 8-6. Supply Function Table

V_{CC}	V_{IO}	Driver Output	Receiver Output	Termination across bus pins YZ and AB
$> UV_{VCC(rising)}$	$> UV_{VIO(rising)}$	Determined by DE and D inputs	Determined by $\overline{RE}$ and A-B	Determined by TERM_TX and TERM_RX pins
$< UV_{VCC(falling)}$	$> UV_{VIO(rising)}$	High impedance	Undetermined	OFF
$> UV_{VCC(rising)}$	$< UV_{VIO(falling)}$	High impedance	High impedance	Undetermined
$< UV_{VCC(falling)}$	$< UV_{VIO(falling)}$	High impedance	High impedance	OFF

Bus terminals are protected against high voltage short circuit events up to ± 16 V. Additionally, bus short circuit current is limited to 250 mA. So in events like bus contention when multiple drivers are driving the bus simultaneously, the current through the bus terminals is internally limited. If the power dissipation makes the junction temperature cross 150 °C, thermal shutdown is activated which disables the driver and receiver and reduces the on-chip power dissipation. The device is enabled once the junction temperature falls by the thermal shutdown hysteresis as specified in electrical parameter section of the data sheet.

9 Application Information Disclaimer

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The THVD1424 is a flexible RS-485 transceiver used for asynchronous data transmissions. The driver and receiver enable pins, slew rate control, duplex control and termination control pins allow the device to be applicable for various point-to-point, multipoint or multidrop network configurations.

9.2 Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T, whose value matches the characteristic impedance, Z_0, of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length. THVD1424 has on-chip 120 Ω termination resistor well suited for most commonly used cables for RS-485 applications. Figure 9-1 shows two end nodes terminated, while remaining nodes unterminated. THVD1424 can be designed in all node designs. TERM_TX pin allows configuring the nodes for end nodes and middle nodes in the network.

Figure 9-2 shows termination on end nodes of each pair of cable in a full duplex network. Once again, THVD1424 makes it possible to have common board design for all nodes. TERM_TX and TERM_RX pins allow configuration for end nodes and middle nodes.

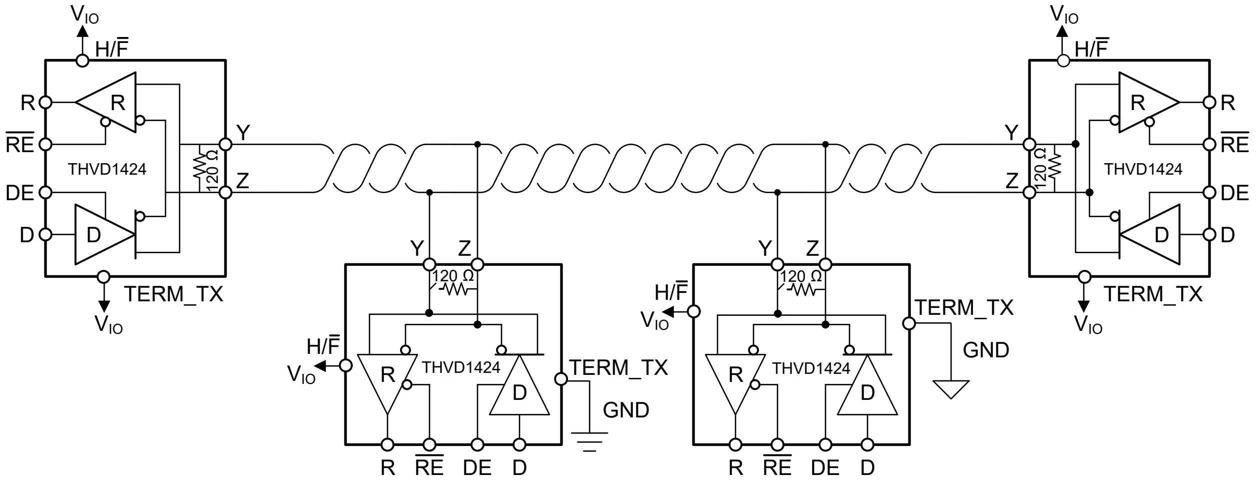


Figure 9-1. Typical RS-485 Network With THVD1424 configured in Half-Duplex mode

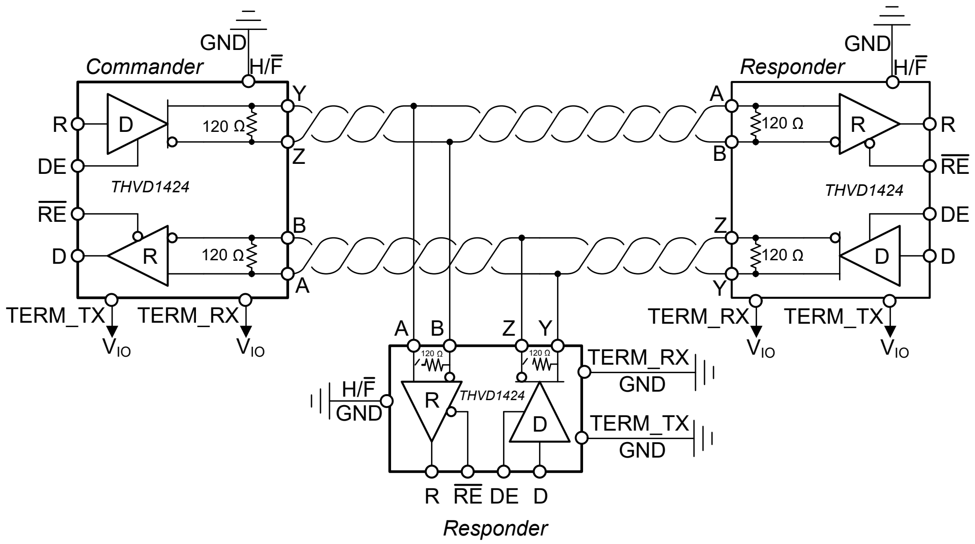


Figure 9-2. Typical RS-485 Network With THVD1424 configured in Full-Duplex mode

9.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

9.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and cable length, which means the higher the data rate, the shorter the cable length; and conversely, the lower the data rate, the longer the cable length. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 300 kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

9.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in Equation 1.

$$L_{(STUB)} \leq 0.1 \times t_r \times v \times c \tag{1}$$

where

- t_r is the 10/90 rise time of the driver
- c is the speed of light (3×10^8 m/s)
- v is the signal velocity of the cable or trace as a factor of c

THVD1424 can be used in both slow-speed and high-speed networks with SLR pin configurability. Slew rate limiting makes the driver output rise/fall time slower so that stub lengths can be increased.

9.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to drive 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12 kΩ. Because the THVD1424 consists of 1/8 UL transceivers, connecting up to 256 transceivers to the bus is possible.

9.2.1.4 Receiver Failsafe

The differential receiver of the THVD1424 is *failsafe* to invalid bus states caused by the following:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver outputs a failsafe logic high state so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds such that the *input indeterminate* range does not include zero volts differential. To comply with the RS-422 and RS-485 standards, the receiver output must output a high when the differential input V_{ID} is more positive than 200 mV, and must output a low when V_{ID} is more negative than –200 mV. The receiver parameters which determine the failsafe performance are V_{TH+}, V_{TH-}, and V_{HYS} (the separation between V_{TH+} and V_{TH-}). As shown in the *Table 8-3*, differential signals more negative than –200 mV always causes a low receiver output, and differential signals more positive than 200 mV always causes a high receiver output.

When the differential input signal is close to zero, it is still above the V_{TH+} threshold, and the receiver output is high. Only when the differential input is more than V_{HYS} below V_{TH+} does the receiver output transition to a low state. Therefore, the noise immunity of the receiver inputs during a bus fault conditions includes the receiver hysteresis value, V_{HYS}, as well as the value of V_{TH+}.

9.2.1.5 Transient Protection

The bus pins of the THVD1424 transceiver family include on-chip ESD protection against ±16-kV HBM and ±8-kV IEC 61000-4-2 contact discharge. The International Electrotechnical Commission (IEC) ESD test is far more severe than the HBM ESD test. The 50% higher charge capacitance, $C_{(S)}$, and 78% lower discharge resistance, $R_{(D)}$, of the IEC model produce significantly higher discharge currents than the HBM model.

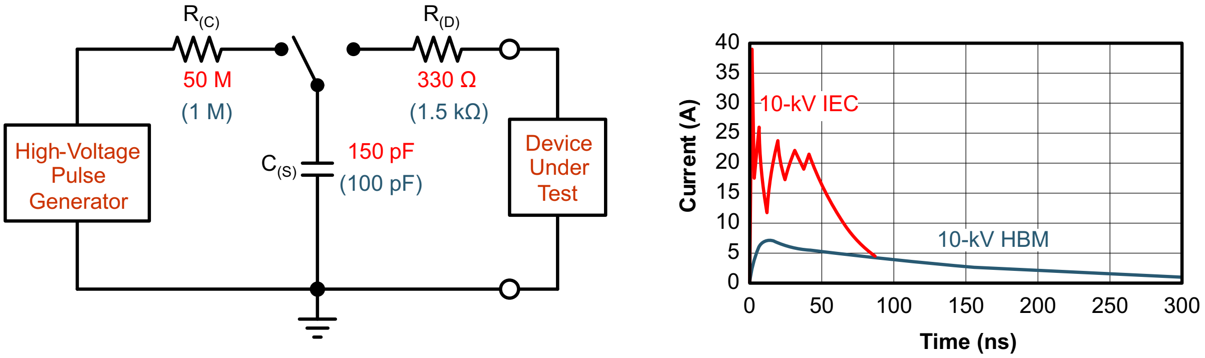


Figure 9-3. HBM and IEC ESD Models and Currents in Comparison (HBM Values in Parenthesis)

The on-chip implementation of IEC ESD protection significantly increases the robustness of equipment. Common discharge events occur because of human contact with connectors and cables. Designers may choose to implement protection against longer duration transients, typically referred to as surge transients.

EFTs are generally caused by relay-contact bounce or the interruption of inductive loads. Surge transients often result from lightning strikes (direct strike or an indirect strike which induce voltages and currents), or the switching of power systems, including load changes and short circuit switching. These transients are often encountered in industrial environments, such as factory automation and power-grid systems.

Figure 9-4 compares the pulse-power of the EFT and surge transients with the power caused by an IEC ESD transient. The left hand diagram shows the relative pulse-power for a 0.5-kV surge transient and 4-kV EFT transient, both of which dwarf the 10-kV ESD transient visible in the lower-left corner. 500-V surge transients are representative of events that may occur in factory environments in industrial and process automation.

The right side diagram shows the pulse-power of a 6-kV surge transient, relative to the same 0.5-kV surge transient. 6-kV surge transients are most likely to occur in power generation and power-grid systems.

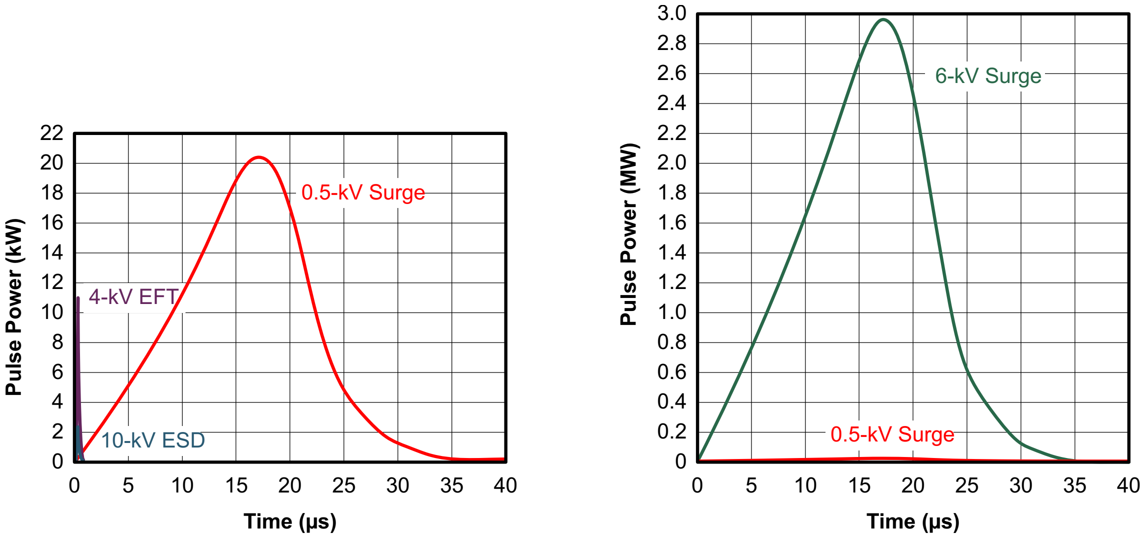


Figure 9-4. Power Comparison of ESD, EFT, and Surge Transients

In the event of surge transients, high-energy content is characterized by long pulse duration and slow decaying pulse power. The electrical energy of a transient that is dumped into the internal protection cells of a transceiver is converted into thermal energy, which heats and destroys the protection cells, thus destroying the transceiver. Figure 9-5 shows the large differences in transient energies for single ESD, EFT, surge transients, and an EFT pulse train that is commonly applied during compliance testing.

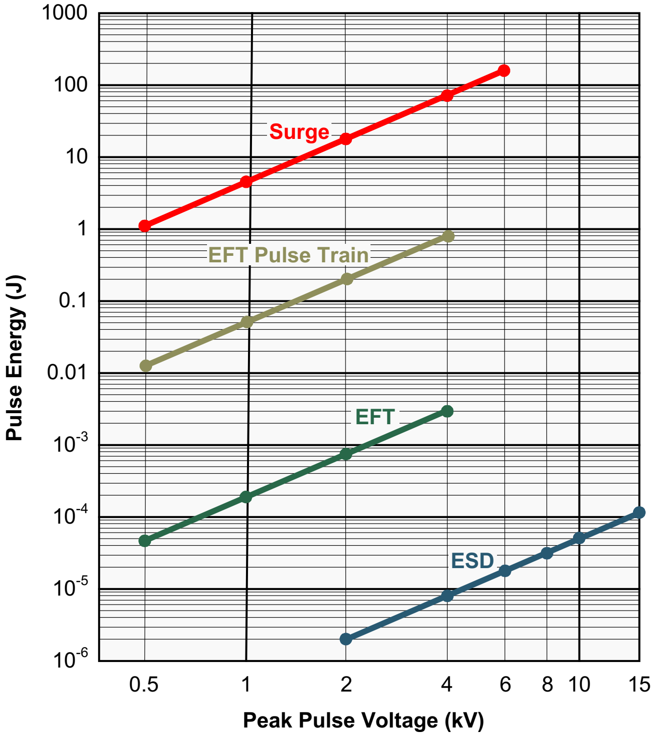


Figure 9-5. Comparison of Transient Energies

9.2.2 Detailed Design Procedure

To protect bus nodes against high-energy transients such as surge, the implementation of external transient protection devices is necessary. Figure 9-6 and Figure 9-7suggest a protection circuit against 1 kV surge (IEC 61000-4-5) transients. Table 9-1 shows the associated bill of materials.

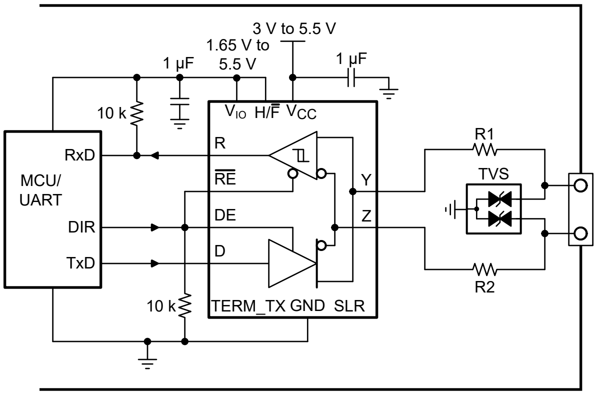


Figure 9-6. Transient Protection Against Surge Transients for THVD1424 Configured in Half-Duplex Mode

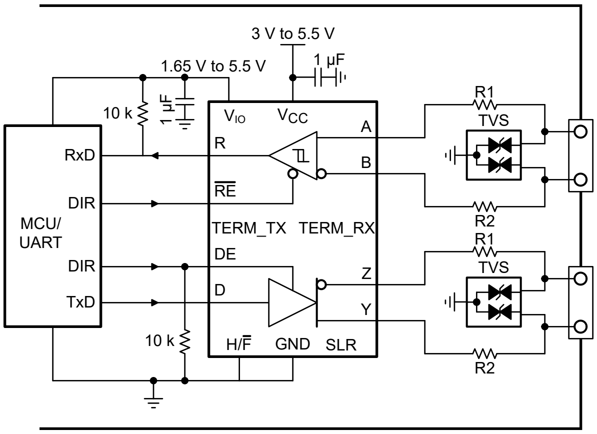


Figure 9-7. Transient Protection Against Surge Transients for THVD1424 Configured in Full-Duplex Mode

Table 9-1. Bill of Materials

DEVICE	FUNCTION	ORDER NUMBER	MANUFACTURER(1)
XCVR	RS-485 transceiver	THVD1424	TI
R1	10-Ω, pulse-proof thick-film resistor	CRCW0603010RJNEAHP	Vishay
R2			
TVS	Bidirectional 400-W transient suppressor	CDSOT23-SM712	Bourns

(1) See the Third Part Disclaimer.

9.2.3 Application Curves

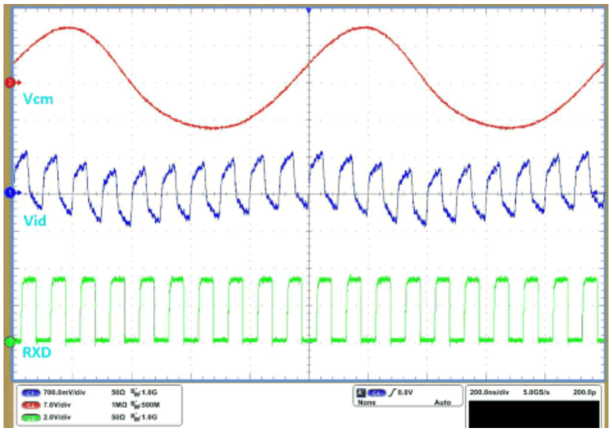


Figure 9-8. THVD1424 Receiver Waveforms at 20 Mbps, with Common Mode Moving at 1 Mhz

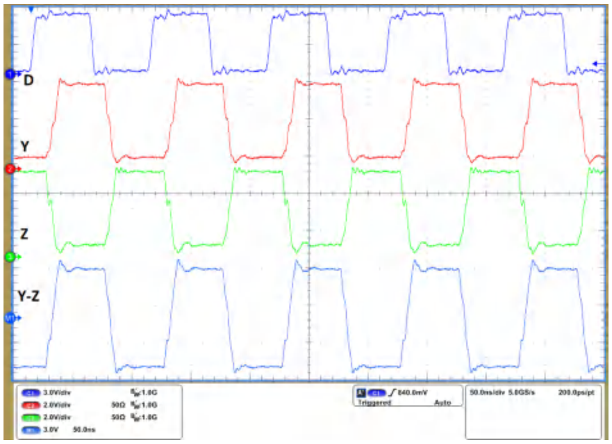


Figure 9-9. THVD1424 Driver Waveforms at 20 Mbps with Termination Enabled

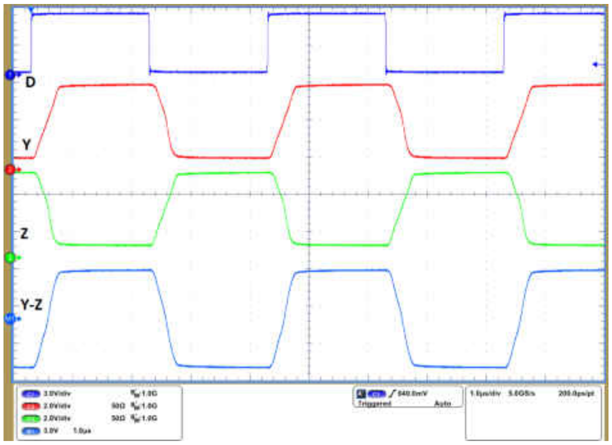


Figure 9-10. THVD1424 Driver Waveforms at 500 kbps with Termination Enabled

9.3 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, both supply pins, V_{CC} and V_{IO}, should be decoupled with at least 1 µF ceramic capacitor located as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes. Proper device operation requires bus side supply V_{CC} to be greater than or equal to logic supply V_{IO} during supply ramp up or during steady state operation.

9.4 Layout

9.4.1 Layout Guidelines

Robust and reliable bus node design often requires the use of external transient protection devices in order to protect against surge transients that may occur in industrial environments. Since these transients have a wide frequency bandwidth (from approximately 3 MHz to 300 MHz), high-frequency layout techniques should be applied during PCB design.

1. Place the protection circuitry close to the bus connector to prevent noise transients from propagating across the board.
2. Use V_{CC} and ground planes to provide low inductance. Note that high-frequency currents tend to follow the path of least impedance and not the path of least resistance.
3. Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
4. Apply at least 1 µF decoupling capacitors as close as possible to the V_{CC} and V_{IO} pins of transceiver, UART and/or controller ICs on the board.
5. Use at least two vias for V_{CC}, V_{IO} and ground connections of decoupling capacitors and protection devices to minimize effective via inductance.
6. Use 1-kΩ to 10-kΩ pull-up and pull-down resistors for logic lines to limit noise currents in these lines during transient events.
7. Insert pulse-proof resistors into the Y, Z, A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
8. While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1 mA.

9.4.2 Layout Example

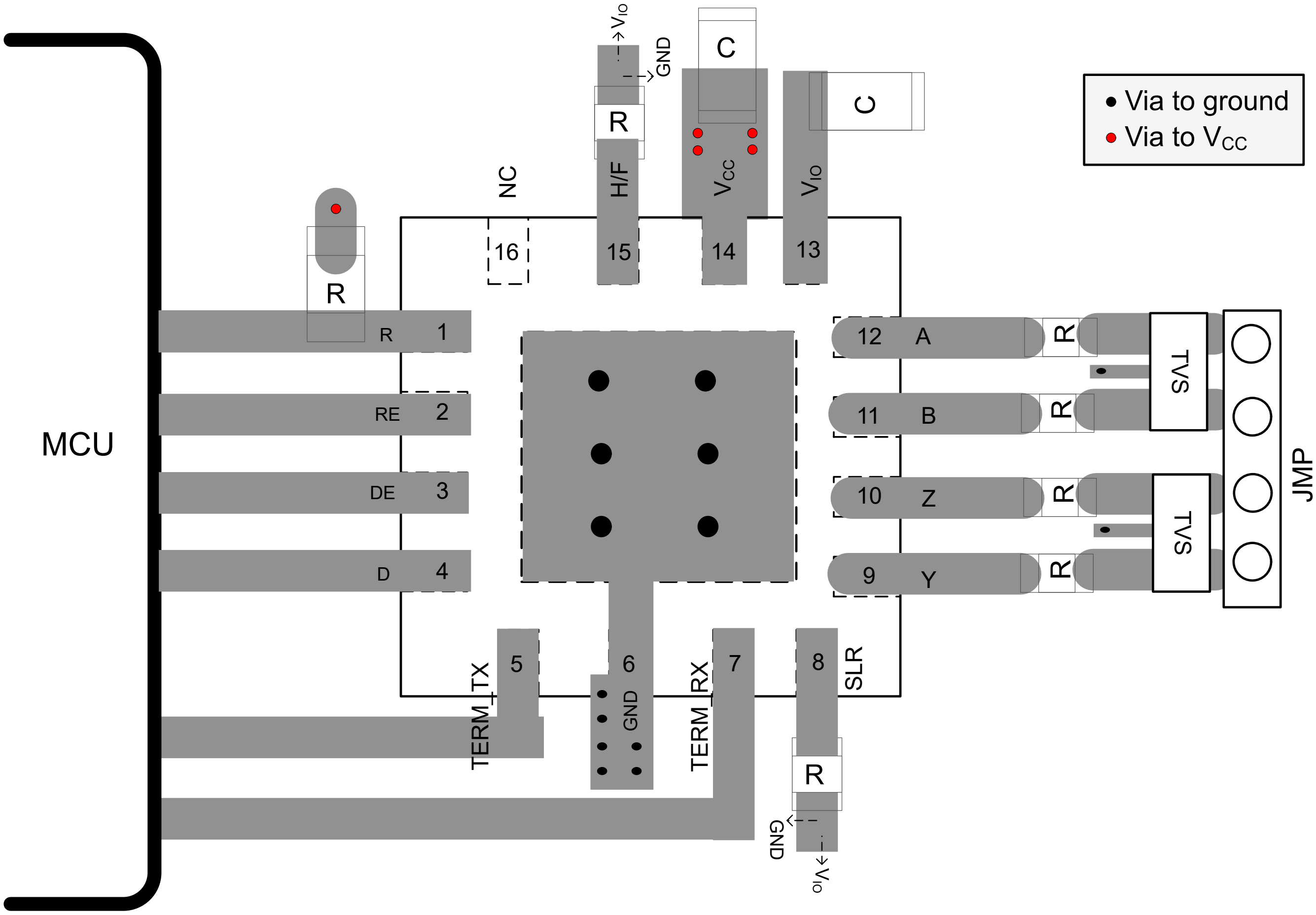


Figure 9-11. Layout Example for THVD1424 in VQFN-16 package

10 Device and Documentation Support

10.1 Device Support

10.1.1 Third-Party Products Disclaimer

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ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THVD1424RGTR	Active	Production	VQFN (RGT) | 16	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1424

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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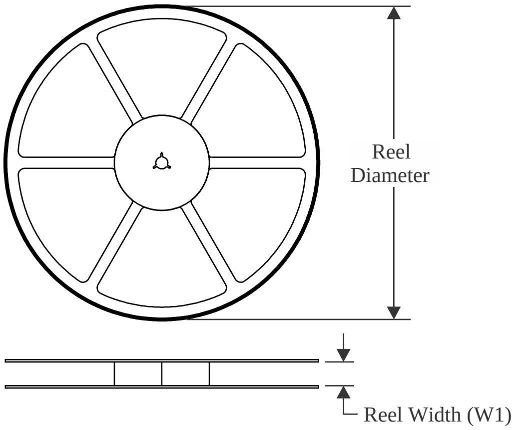
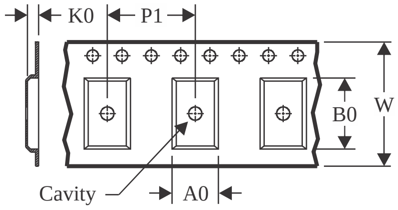
TAPE AND REEL INFORMATION

REEL DIMENSIONS

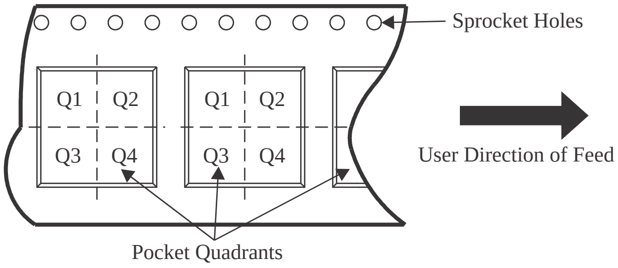


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

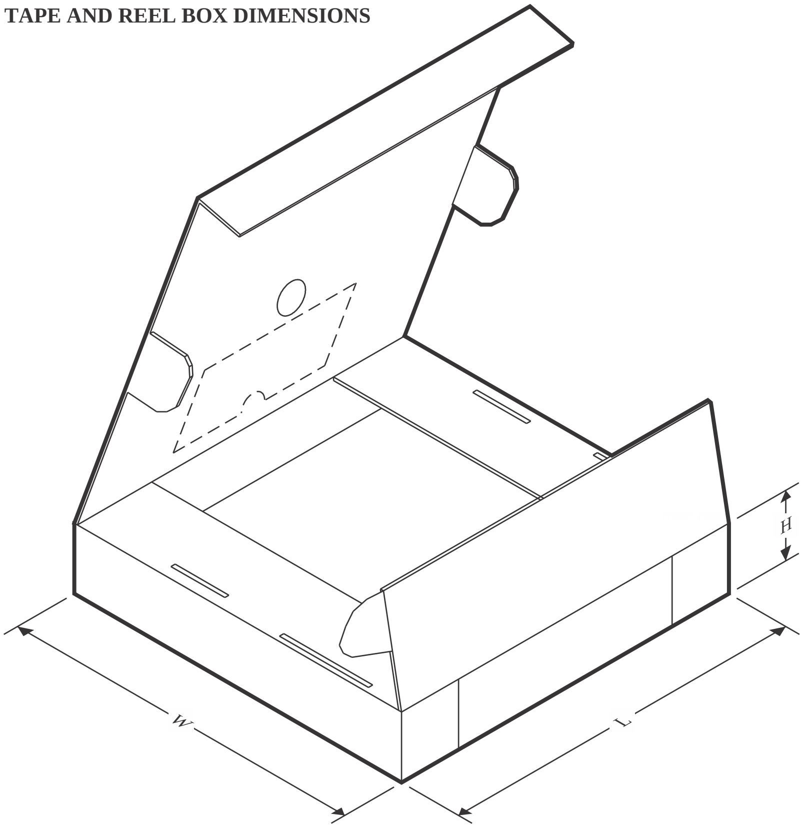
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THVD1424RGTR	VQFN	RGT	16	5000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



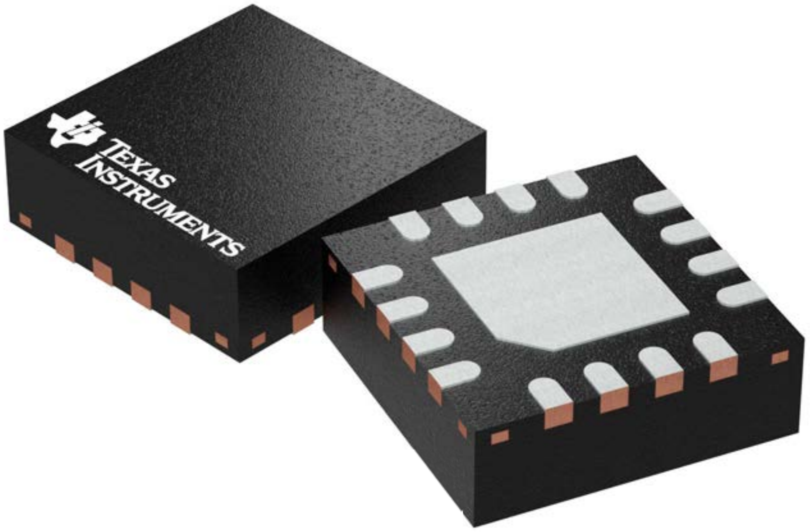
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THVD1424RGTR	VQFN	RGT	16	5000	367.0	367.0	35.0

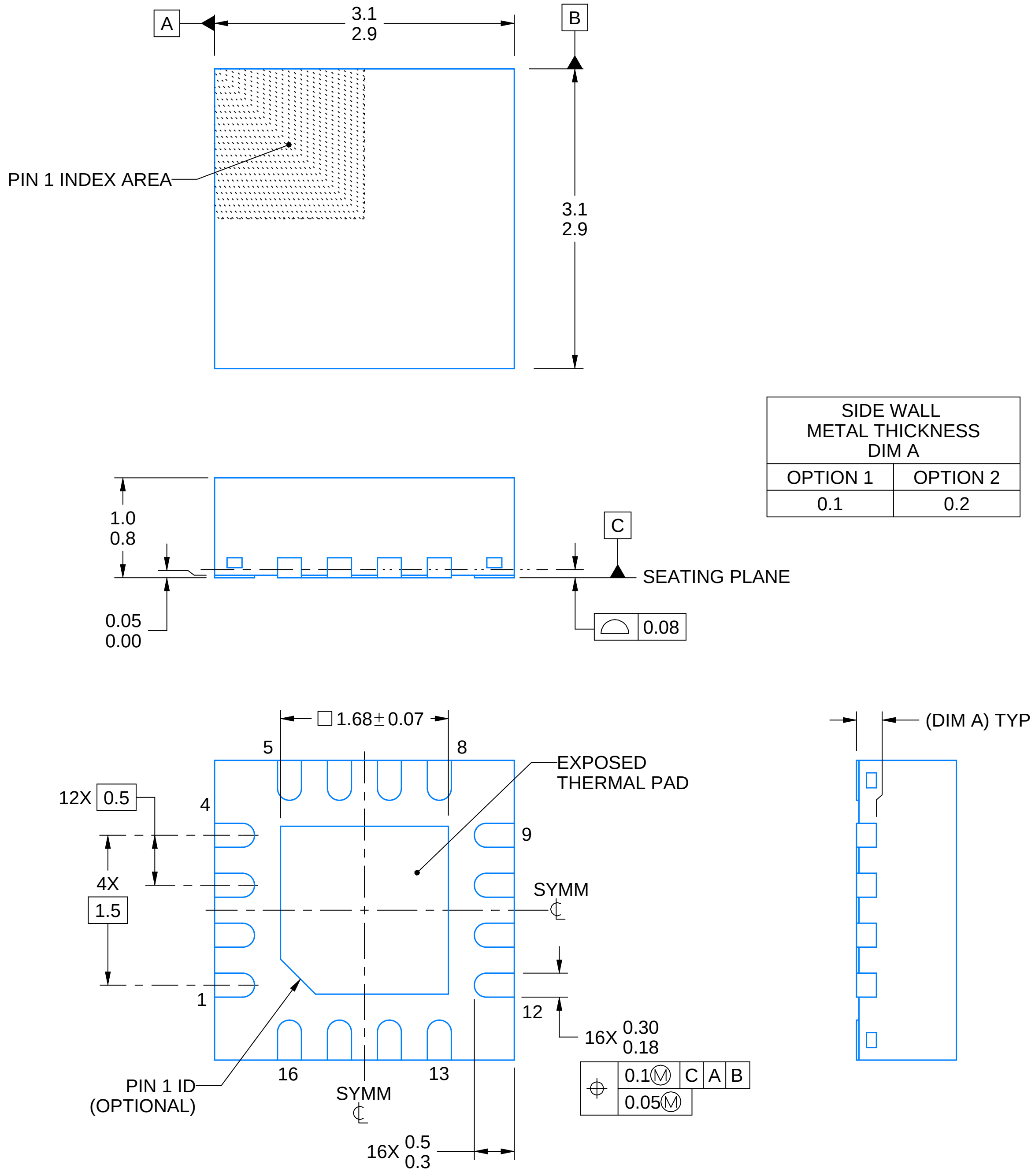
RGT 16

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

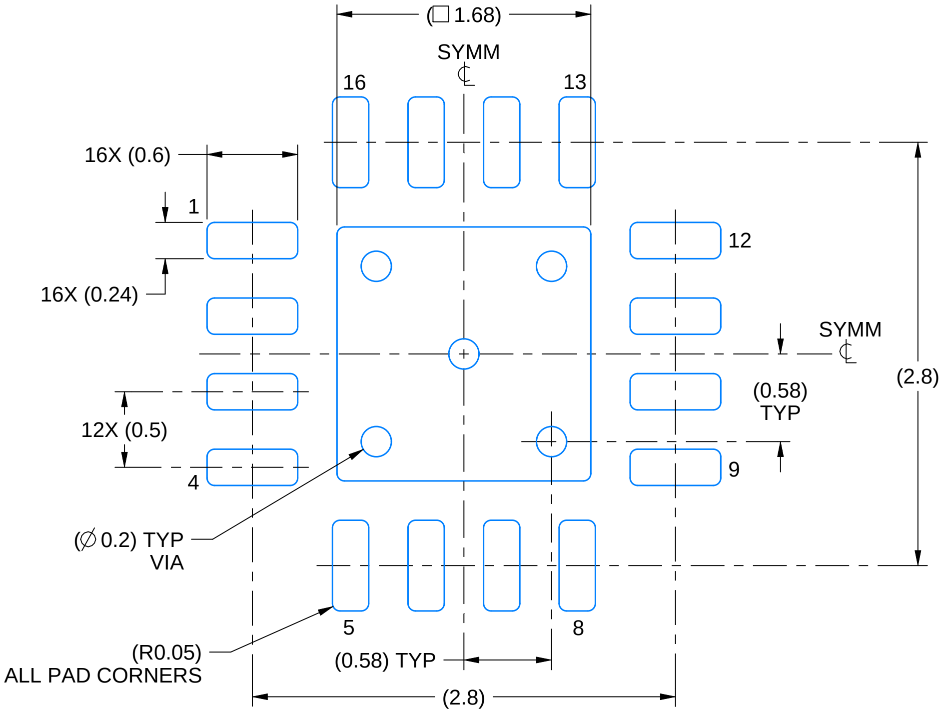


SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

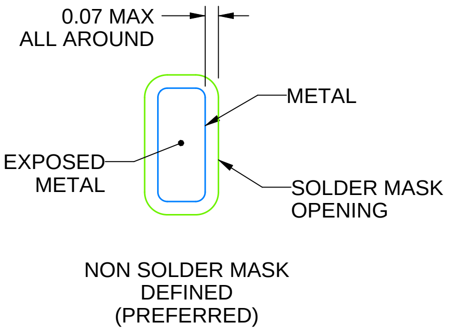
4222419/D 04/2022

NOTES:

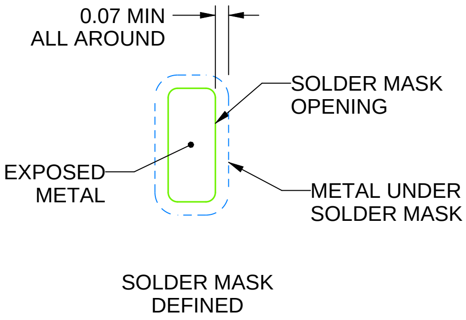
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



NON SOLDER MASK
DEFINED
(PREFERRED)

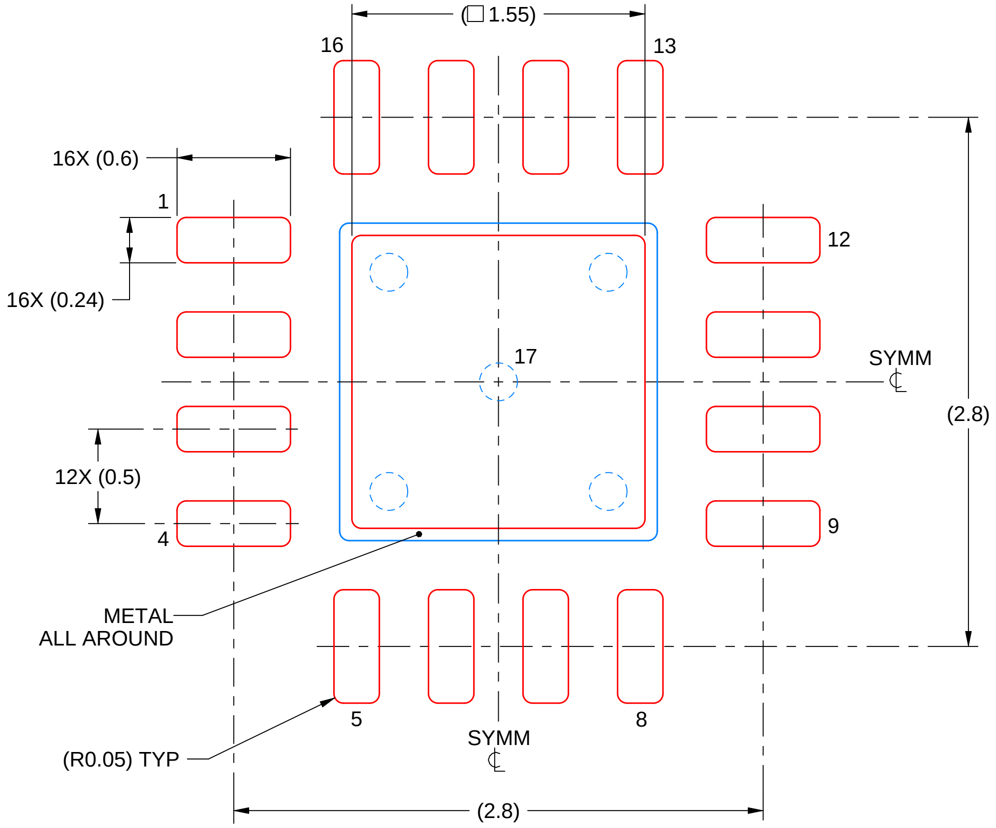


SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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