TEXAS INSTRUMENTS

THVD1510, THVD1512
THVD1550, THVD1551, THVD1552

SLLSEV1C – SEPTEMBER 2017 – REVISED DECEMBER 2018

THVD15xx 5-V RS-485 Transceivers With ±18-kV IEC ESD Protection

1 Features

- Meets or Exceeds the Requirements of the TIA/EIA-485A Standard
- 4.5 V to 5.5 V Supply Voltage
- Integrated Bus I/O Protection
  - ± 30 kV HBM ESD
  - ± 18 kV IEC 61000-4-2 ESD Contact Discharge
  - ± 25 kV IEC 61000-4-2 ESD Air-Gap Discharge
  - ± 4 kV IEC 61000-4-4 Electrical Fast Transient
- Extended Operational Common-mode: ± 15 V
- Low EMI 500 kbps and 50 Mbps Data Rates
- Extended Temperature Range: -40°C to 125°C
- Large Receiver Hysteresis for Noise Rejection
- Low Power Consumption
  - Low Standby Supply Current: < 1 µA
  - Current During Operation: < 1 mA
- Glitch-Free Power-Up/Down for Hot Plug-in Capability
- Open, Short, and Idle Bus Failsafe
- 1/8 Unit Load Options (Up to 256 Bus Nodes)
- Small-Size VSSOP Packages Save Board Space or SOIC for Drop-in Compatibility

2 Applications

- Motor Drives
- Factory Automation and Control
- Grid Infrastructure
- Building Automation
- HVAC Systems
- Video Surveillance
- Process Analytics
- Telecom Infrastructure

3 Description

THVD15xx is a family of noise-immune RS-485/RS-422 transceivers designed to operate in rugged industrial environments. The bus pins of these devices are robust to high levels of IEC electrical fast transients (EFT) and IEC electrostatic discharge (ESD) events, eliminating the need for additional system-level protection components.

Each of these devices operates from a single 5-V supply. The devices in this family feature an extended common-mode voltage range which makes them suitable for multi-point applications over long cable runs.

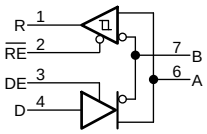
THVD15xx family of devices is available in small VSSOP packages for space-constrained applications. These devices are characterized over ambient free-air temperatures from –40°C to 125°C.

Device Information(1)

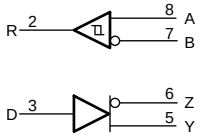
PART NUMBER	PACKAGE	BODY SIZE (NOM)
THVD1510 THVD1550	VSSOP (8)	3.00 mm × 3.00 mm
	SOIC (8)	4.90 mm × 3.91 mm
THVD1551	VSSOP (8)	3.00 mm × 3.00 mm
THVD1512	VSSOP (10)	3.00 mm × 3.00 mm
THVD1552	VSSOP (10)	3.00 mm × 3.00 mm
	SOIC (14)	8.65 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

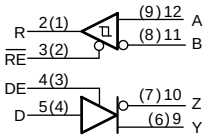
THVD1510 and THVD1550 Simplified Schematic



THVD1551 Simplified Schematic



THVD1512 and THVD1552 Simplified Schematic



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4 Revision History

Changes from Revision B (July 2018) to Revision C **Page**

- Changed the Description of pins 13 and 14 in the *Pin Functions* table for THVD1512, THVD1552 D package ... 5

Changes from Revision A (January 2018) to Revision B **Page**

- Added T_{SD} to the *Electrical Characteristics* table ... 8

Changes from Original (September 2017) to Revision A **Page**

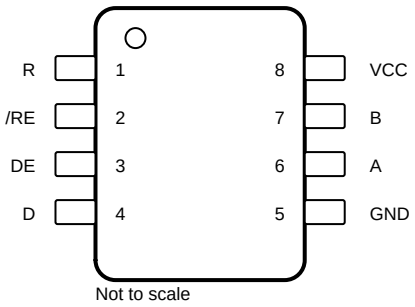
- Changed the Machine model (MM) value From: ±400 To: ±200 in the *ESD Ratings* ... 6
- Changed the V_{OH} MIN value From: 2.4 V To: 4 V in the *Electrical Characteristics* table ... 8

5 Device Comparison Table

PART NUMBER	DUPLEX	ENABLES	SIGNALING RATE	NODES
THVD1512	Full	DE, $\overline{RE}$	up to 500 kbps	256
THVD1510	Half	DE, $\overline{RE}$		
THVD1552	Full	DE, $\overline{RE}$	up to 50 Mbps	196
THVD1551	Full	None		
THVD1550	Half	DE, $\overline{RE}$		

6 Pin Configuration and Functions

THVD1510, THVD1550 Devices
8-Pin D Package (SOIC)
Top View



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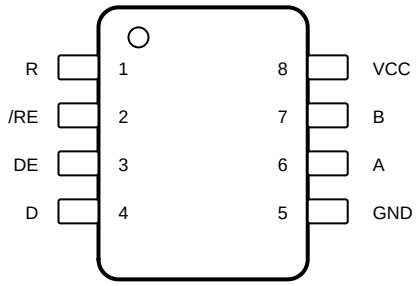
THVD1510, THVD1550 Devices
8-Pin DGK Package (VSSOP)
Top View



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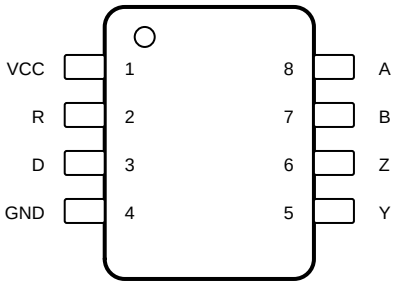
Pin Functions

PIN			I/O	DESCRIPTION
NAME	D	DGK		
A	6	6	Bus input/output	Bus I/O port, A (complementary to B)
B	7	7	Bus input/output	Bus I/O port, B (complementary to A)
D	4	4	Digital input	Driver data input
DE	3	3	Digital input	Driver enable, active high (2 MΩ internal pull-down)
GND	5	5	Ground	Device ground
R	1	1	Digital output	Receive data output
V_{CC}	8	8	Power	5-V supply
$\overline{RE}$	2	2	Digital input	Receiver enable, active low (2 MΩ internal pull-up)

THVD1551 Device
8-Pin DGK Package (VSSOP)
Top View



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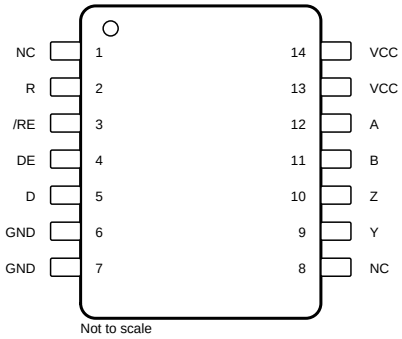
Pin Functions

PIN		I/O	DESCRIPTION
NAME	DGK		
A	8	Bus input	Bus input, A (complementary to B)
B	7	Bus input	Bus input, B (complementary to A)
D	3	Digital input	Driver data input
GND	4	Ground	Device ground
R	2	Digital output	Receive data output
V_{CC}	1	Power	5-V supply
Y	5	Bus output	Bus output, Y (complementary to Z)
Z	6	Bus output	Bus output, Z (complementary to Y)

THVD1552 Device
14-Pin D Package (SOIC)
Top View



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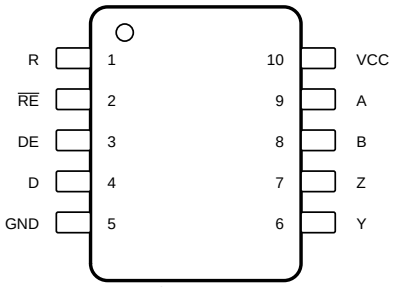
THVD1512, THVD1552 Devices
10-Pin DGS Package (VSSOP)
Top View



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Pin Functions

PIN			I/O	DESCRIPTION
NAME	D	DGS		
A	12	9	Bus input	Bus input, A (complementary to B)
B	11	8	Bus input	Bus input, B (complementary to A)
D	5	4	Digital input	Driver data input
DE	4	3	Digital input	Driver enable, active high (2 MΩ internal pull-down)
GND	6, 7 (1)	5	Ground	Device ground
NC	1, 8	—	—	Internally not connected
R	2	1	Digital output	Receive data output
V_{CC}	—	10	Power	5-V supply.
	13, 14	—	Power	5-V supply. These pins are not connected together internally, so power must be applied to both.
Y	9	6	Bus output	Bus output, Y (Complementary to Z)
Z	10	7	Bus output	Bus output, Z (Complementary to Y)
$\overline{RE}$	3	2	Digital input	Receiver enable, active low (2 MΩ internal pull-up)

(1) These pins are internally connected

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	V_{CC}	–0.5	7	V
Bus voltage	Range at any bus pin (A, B, Y, or Z) as differential or common-mode with respect to GND	–18	18	V
Input voltage	Range at any logic pin (D, DE, or $\overline{RE}$)	–0.3	5.7	V
Receiver output current	I_O	–24	24	mA
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Contact discharge, per IEC 61000-4-2	Bus terminals and GND	±18,000	V
		Air-gap discharge, per IEC 61000-4-2	Bus terminals and GND	±25,000	
		Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Bus terminals and GND	±30,000	
			All pins except Bus terminals and GND	±8,000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1,500	
		Machine model (MM), per JEDEC JESD22-A115-A		±200	
$V_{(EFT)}$	Electrical fast transient	Per IEC 61000-4-4	Bus terminals	±4,000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5		5.5	V
V_I	Input voltage at any bus terminal (1)		-15		15	V
V_{IH}	High-level input voltage (driver, driver enable, and receiver enable inputs)		2		V_{CC}	V
V_{IL}	Low-level input voltage (driver, driver enable, and receiver enable inputs)		0		0.8	V
V_{ID}	Differential input voltage		-15		15	V
I_O	Output current, driver		-60		60	mA
I_{OR}	Output current, receiver		-8		8	mA
R_L	Differential load resistance		54			Ω
$1/t_{UI}$	Signaling rate	THVD1510, THVD1512			500	kbps
		THVD1550, THVD1551, THVD1552			50	Mbps
T_A	Operating ambient temperature		-40		125	°C
T_J	Junction temperature		-40		150	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

7.4 Thermal Information

THERMAL METRIC (1)		THVD1510 THVD1550	THVD1552	THVD1510 THVD1550 THVD1551	THVD1512 THVD1552	UNIT
		D (SOIC)	D (SOIC)	DGK (VSSOP)	DGS (VSSOP)	
		8 PINS	14 PINS	8 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	112.4	88.0	151.7	151.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	62.7	45.4	62.8	59.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62.0	44.1	81.3	81.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	15.4	11.3	7.8	6.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	61.3	43.7	79.8	79.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Power Dissipation

PARAMETER		TEST CONDITIONS			VALUE	UNIT
PD	Driver and receiver enabled, V_{CC} = 5.5 V, T_A = 125 °C, 50% duty cycle square wave at signaling rate	Unterminated R_L = 300 Ω, C_L = 50 pF (driver)	THVD151x	500 kbps	210	mW
			THVD155x	50 Mbps	350	
		RS-422 load R_L = 100 Ω, C_L = 50 pF (driver)	THVD151x	500 kbps	220	mW
			THVD155x	50 Mbps	330	
		RS-485 load R_L = 54 Ω, C_L = 50 pF (driver)	THVD151x	500 kbps	250	mW
			THVD155x	50 Mbps	340	

7.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
Driver								
$\|V_{OD}\|$	Driver differential output voltage magnitude	R_L = 60 Ω, -15 V ≤ V_{test} ≤ 15 V, (See Figure 11)			1.5	2.7		V
		R_L = 100 Ω (See Figure 12)			2	3		V
		R_L = 54 Ω (See Figure 12)			1.5	2.7		V
$\Delta\|V_{OD}\|$	Change in differential output voltage	R_L = 54 Ω (See Figure 12)			–200		200	mV
V_{OC}	Common-mode output voltage				1	V_{CC}/2	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage				–200		200	mV
I_{OS}	Short-circuit output current	DE = V_{CC}, -15 V ≤ V_O ≤ 15V			–250		250	mA
Receiver								
I_I	Bus input current	DE = 0 V, V_{CC} = 0 V or 5.5 V	THVD151x	V_I = 12 V		75	125	µA
				V_I = 15 V		95	156	
				V_I = -7 V	-100	-40		
				V_I = -15 V	-215	-85		
			THVD155x	V_I = 12 V		115	160	
				V_I = 15 V		150	200	
				V_I = -7 V	-130	-75		
				V_I = -15 V	-280	-180		
Receiver								
V_{TH+}	Positive-going input threshold voltage	Over common-mode range of - 7 V to +12 V			See(1)	–85	–20	mV
V_{TH-}	Negative-going input threshold voltage				–200	–135	See(1)	mV
V_{HYS}	Input hysteresis					50		mV
V_{TH+}	Positive-going input threshold voltage	Over common-mode range of ± 15 V			See(1)	–85	–20	mV
V_{TH-}	Negative-going input threshold voltage				–220	–135	See(1)	mV
V_{HYS}	Input hysteresis					50		mV
V_{OH}	Output high voltage	I_{OH} = -8 mA			4	V_{CC} - 0.3		V
V_{OL}	Output low voltage	I_{OL} = 8 mA				0.2	0.4	V
I_{OZ}	Output high-impedance current	V_O = 0 V or V_{CC}, $\overline{RE}$ = V_{CC}			-1		1	µA
Logic								
I_{IN}	Input current (D, DE, $\overline{RE}$)	4.5 V ≤ V_{CC} ≤ 5.5 V, 0 V ≤ V_{IN} ≤ V_{CC}			–5	0	5	µA
Supply								
I_{CC}	Supply current (quiescent)	Driver and receiver enabled		$\overline{RE}$ = 0 V, DE = V_{CC}, No load		700	1000	µA
		Driver enabled, receiver disabled		$\overline{RE}$ = V_{CC}, DE = V_{CC}, No load		400	620	µA
		Driver disabled, receiver enabled		$\overline{RE}$ = 0 V, DE = 0 V, No load		400	630	µA
		Driver and receiver disabled		$\overline{RE}$ = V_{CC}, DE = 0 V, D = open, No load		0.1	1	µA
T_{SD}	Thermal shutdown temperature					170		°C

(1) Under any specific conditions, V_{TH+} is specified to be at least V_{HYS} higher than V_{TH-}.

7.7 Switching Characteristics

500-kbps devices (THVD1510, THVD1512) over recommended operating conditions

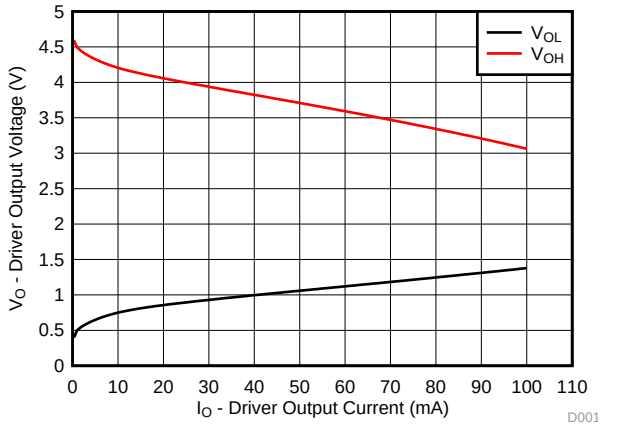
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
t_r, t_f	Differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF	See Figure 13	300	400	600	ns
t_{PHL}, t_{PLH}	Propagation delay				350	500	ns
$t_{SK(P)}$	Pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$					15	ns
t_{PHZ}, t_{PLZ}	Disable time (THVD1510, THVD1512)		See Figure 14 and Figure 15		110	200	ns
t_{PZH}, t_{PZL}	Enable time (THVD1510, THVD1512)	$\overline{RE}$ = 0 V			100	500	ns
		$\overline{RE}$ = V_{CC}			2	4	µs
Receiver							
t_r, t_f	Differential output rise/fall time	C_L = 15 pF	See Figure 16		15	25	ns
t_{PHL}, t_{PLH}	Propagation delay				50	60	ns
$t_{SK(P)}$	Pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$					10	ns
t_{PHZ}, t_{PLZ}	Disable time (THVD1510, THVD1512)				30	40	ns
$t_{PZH(1)}$, $t_{PZL(1)}$, $t_{PZH(2)}$, $t_{PZL(2)}$	Enable time (THVD1510, THVD1512)	DE = V_{CC}	See Figure 17		60	100	ns
		DE = 0 V	See Figure 18		3	8	µs

7.8 Switching Characteristics

50-Mbps devices (THVD1550, THVD1551, THVD1552) over recommended operating conditions

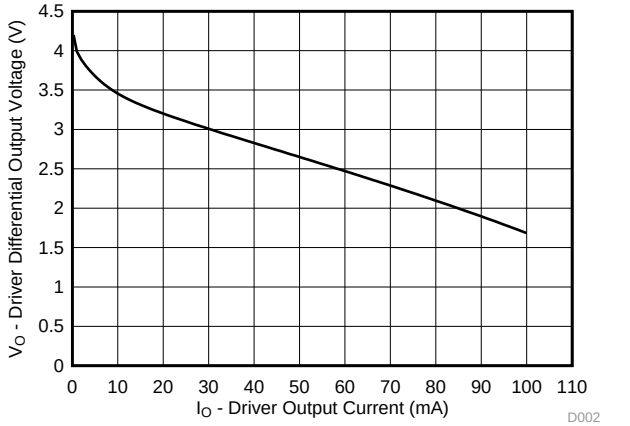
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
t_r, t_f	Differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF	See Figure 13	1	2	6	ns
t_{PHL}, t_{PLH}	Propagation delay			5	10	16	ns
$t_{SK(P)}$	Pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$					3.5	ns
t_{PHZ}, t_{PLZ}	Disable time (THVD1550, THVD1552)		See Figure 14 and Figure 15		10	22	ns
t_{PZH}, t_{PZL}	Enable time (THVD1550, THVD1552)	$\overline{RE}$ = 0 V			10	22	ns
		$\overline{RE}$ = V_{CC}			2	4	µs
Receiver							
t_r, t_f	Differential output rise/fall time	C_L = 15 pF	See Figure 16	1	3	6	ns
t_{PHL}, t_{PLH}	Propagation delay				30	45	ns
$t_{SK(P)}$	Pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$					2	ns
t_{PHZ}, t_{PLZ}	Disable time (THVD1550, THVD1552)				8	18	ns
$t_{PZH(1)}$, $t_{PZL(1)}$, $t_{PZH(2)}$, $t_{PZL(2)}$	Enable time (THVD1550, THVD1552)	DE = V_{CC}	See Figure 17		55	90	ns
		DE = 0 V	See Figure 18		3	8	µs

7.9 Typical Characteristics



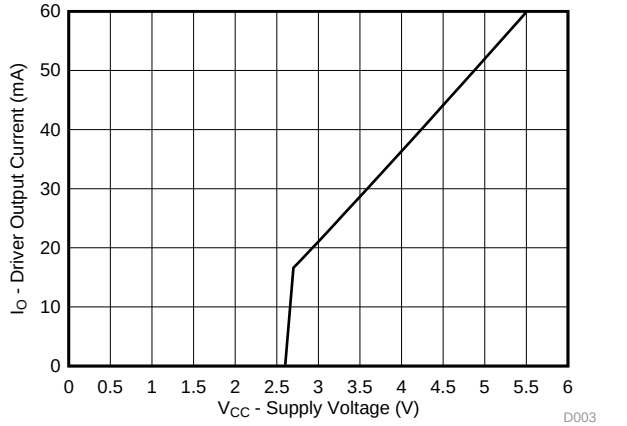
V_{CC} = 5 V DE = V_{CC} D = 0 V

Figure 1. Driver Output Voltage vs Driver Output Current



V_{CC} = 5 V DE = V_{CC} D = 0 V

Figure 2. Driver Differential Output Voltage vs Driver Output



T_A = 25°C R_L = 54 Ω D = V_{CC}
DE = V_{CC}

Figure 3. Driver Output Current vs Supply Voltage

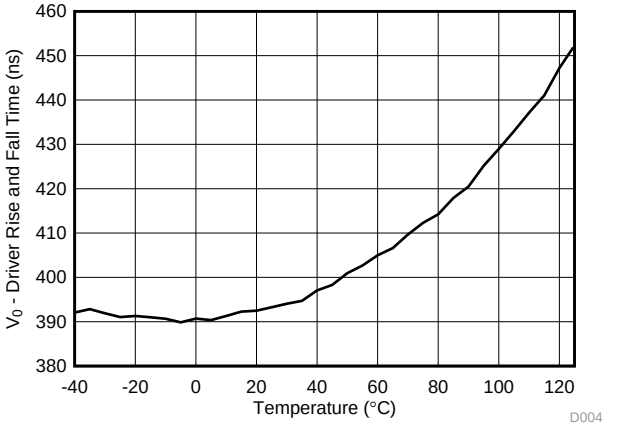


Figure 4. THVD1510 Driver Rise or Fall Time vs Temperature

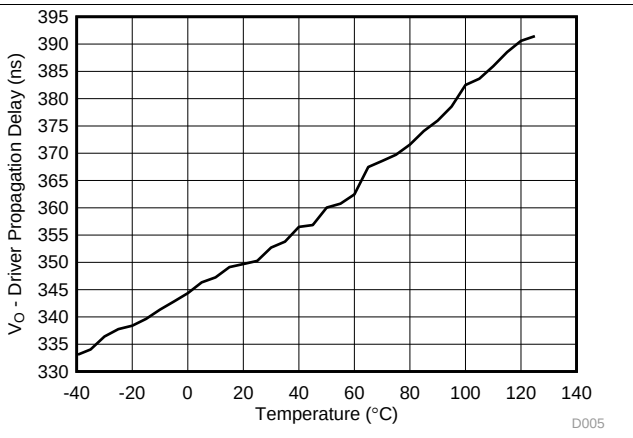


Figure 5. THVD1510 Driver Propagation Delay vs Temperature

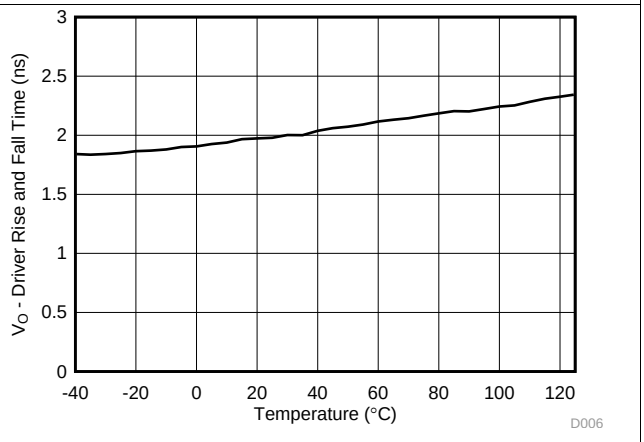


Figure 6. THVD1550 Driver Rise or Fall Time vs Temperature

Typical Characteristics (continued)

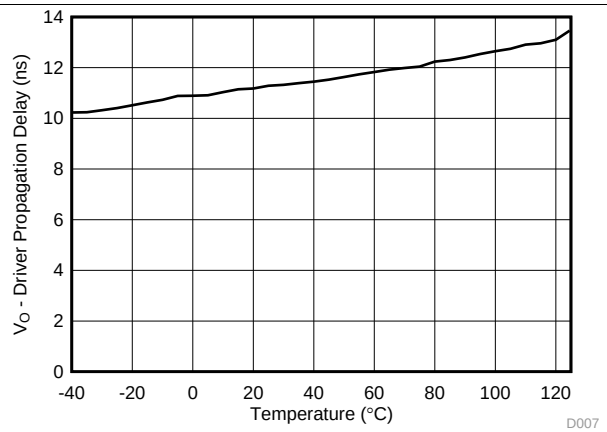


Figure 7. THVD1550 Driver Propagation Delay vs Temperature

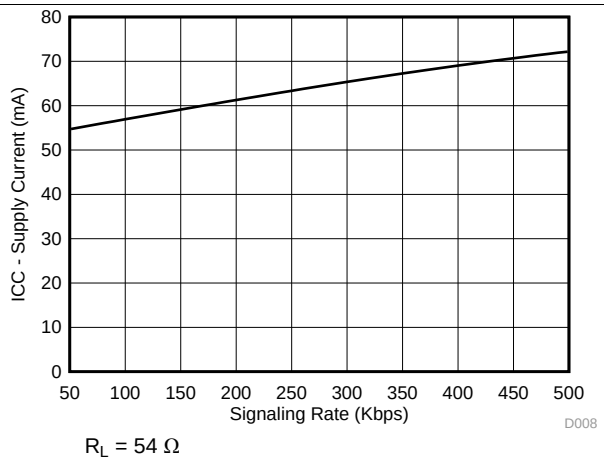


Figure 8. THVD1510 Supply Current vs Signal Rate

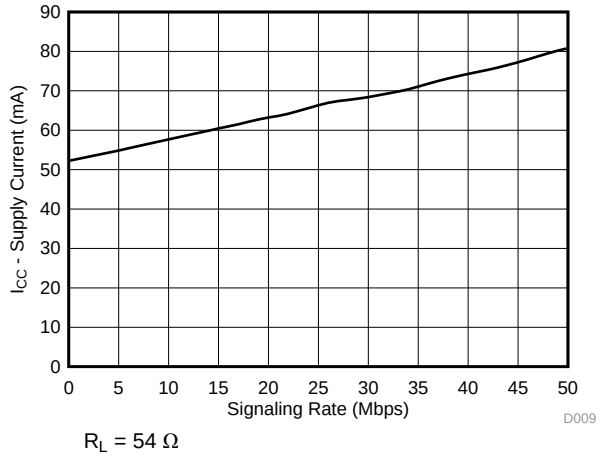


Figure 9. THVD1550 Supply Current vs Signal Rate

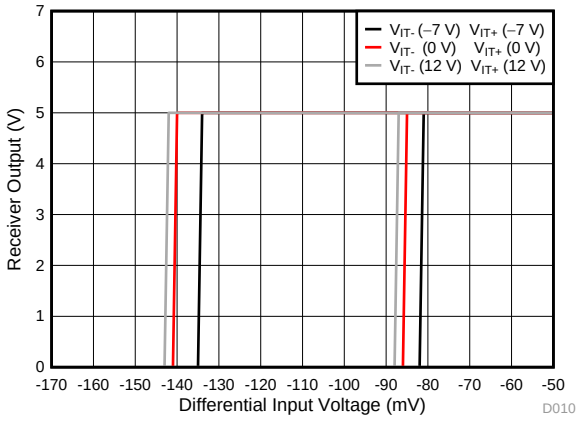


Figure 10. Receiver Output vs Input

8 Parameter Measurement Information

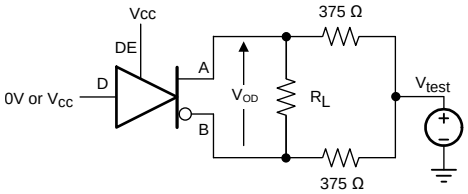


Figure 11. Measurement of Driver Differential Output Voltage With Common-Mode Load

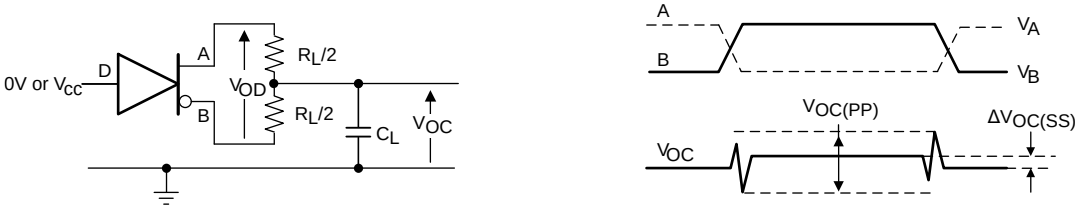


Figure 12. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

Parameter Measurement Information (continued)

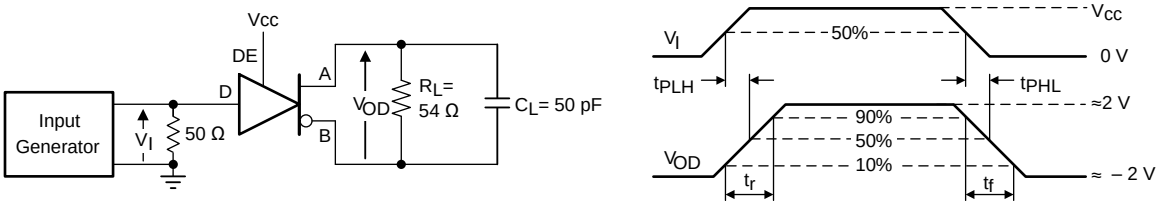


Figure 13. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays

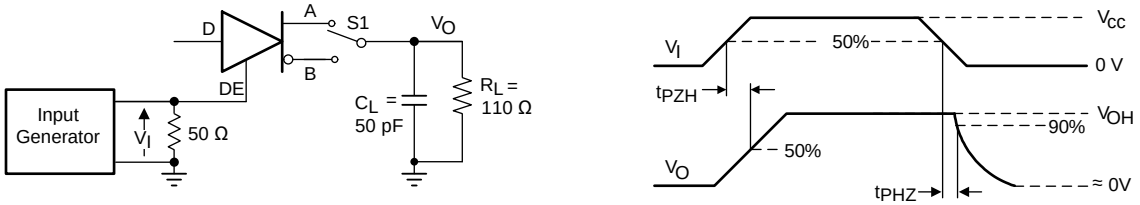


Figure 14. Measurement of Driver Enable and Disable Times With Active High Output and Pull-Down Load

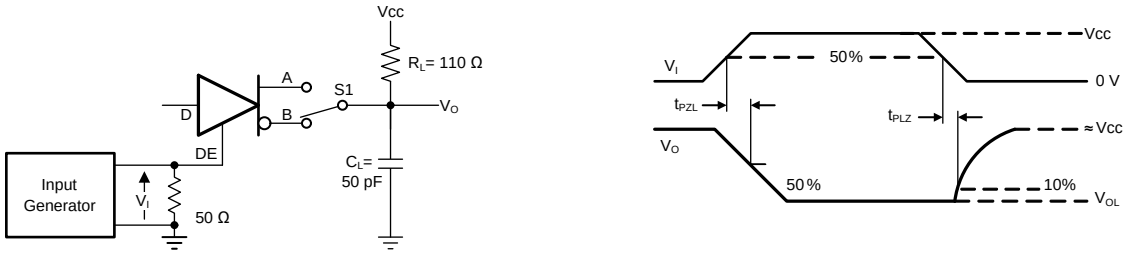


Figure 15. Measurement of Driver Enable and Disable Times With Active Low Output and Pull-up Load

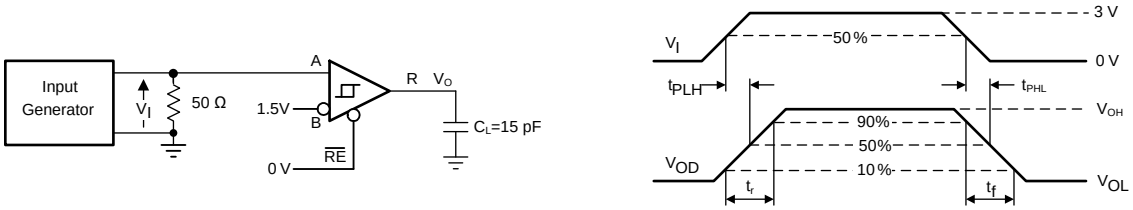


Figure 16. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

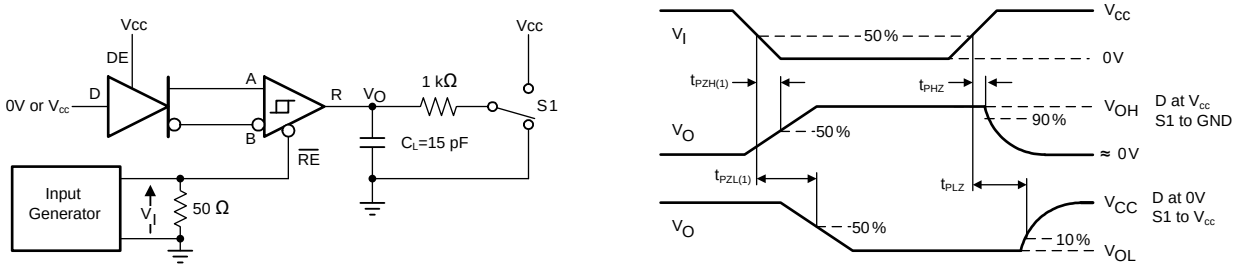


Figure 17. Measurement of Receiver Enable/Disable Times With Driver Enabled

Parameter Measurement Information (continued)

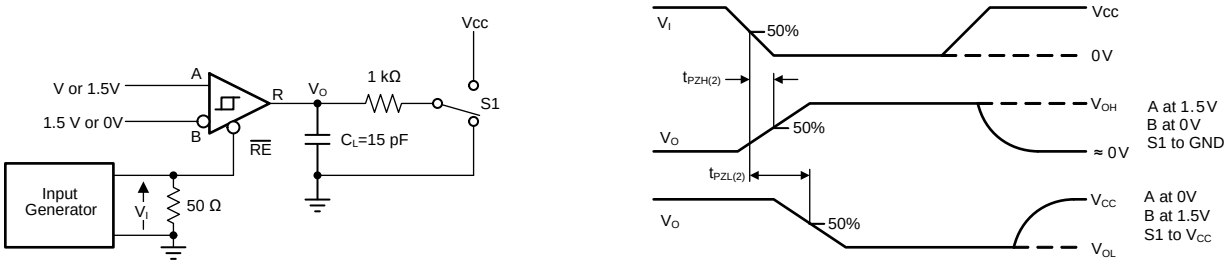


Figure 18. Measurement of Receiver Enable Times With Driver Disabled

9 Detailed Description

9.1 Overview

THVD1510 and THVD1550 are low-power, half-duplex RS-485 transceivers available in two speed grades suitable for data transmission up to 500 kbps and 50 Mbps respectively.

THVD1551 is fully enabled with no external enabling pins. THVD1512 and THVD1552 have active-high driver enables and active-low receiver enables. A standby current of less than 1 µA can be achieved by disabling both driver and receiver.

9.2 Functional Block Diagrams

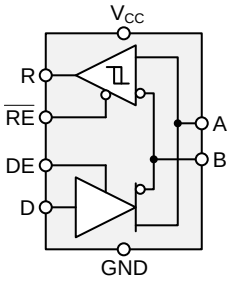


Figure 19. THVD1510 and THVD1550

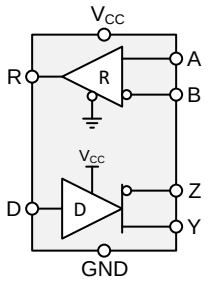


Figure 20. THVD1551

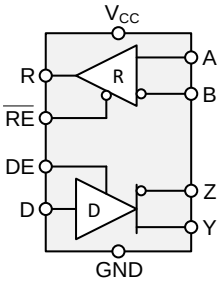


Figure 21. THVD1512 and THVD1552

9.3 Feature Description

Internal ESD protection circuits of the THVD15xx protect the transceivers against electrostatic discharges (ESD) according to IEC 61000-4-2 of up to ±18 kV and against electrical fast transients (EFT) according to IEC 61000-4-4 of up to ±4 kV. With careful system design, one could achieve ±4 kV EFT Criterion A (no data loss when transient noise is present).

Feature Description (continued)

The THVD15xx device family provides internal biasing of the receiver input thresholds in combination with large input-threshold hysteresis. The receiver output remains logic high under a bus-idle or bus-short conditions without the need for external failsafe biasing resistors. Device operation is specified over a wide ambient temperature range from –40°C to 125°C.

9.4 Device Functional Modes

9.4.1 Device Functional Modes for THVD1510 and THVD1550

When the driver enable pin, DE, is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case the differential output voltage defined as $V_{OD} = V_A – V_B$ is positive. When D is low, the output states reverse: B turns high, A becomes low, and V_{OD} is negative.

When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pull-down resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pull-up resistor to V_{CC}, thus, when left open while the driver is enabled, output A turns high and B turns low.

Table 1. Driver Function Table for THVD1510 and THVD1550

INPUT	ENABLE	OUTPUTS		FUNCTION
D	DE	A	B	
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus high by default

When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A – V_B$ is higher than the positive input threshold, V_{TH+}, the receiver output, R, turns high. When V_{ID} is lower than the negative input threshold, V_{TH-}, the receiver output, R, turns low. If V_{ID} is between V_{TH+} and V_{TH-} the output is indeterminate.

When $\overline{RE}$ is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted to one another (short-circuit), or the bus is not actively driven (idle bus).

Table 2. Receiver Function Table for THVD1510 and THVD1550

DIFFERENTIAL INPUT	ENABLE	OUTPUT	FUNCTION
$V_{ID} = V_A – V_B$	$\overline{RE}$	R	
$V_{TH+} < V_{ID}$	L	H	Receive valid bus high
$V_{TH-} < V_{ID} < V_{TH+}$	L	?	Indeterminate bus state
$V_{ID} < V_{TH-}$	L	L	Receive valid bus low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

9.4.2 Device Functional Modes for THVD1551

For this device, the driver and receiver are fully enabled, thus the differential outputs Y and Z follow the logic states at data input D at all times. A logic high at D causes Y to turn high and Z to turn low. In this case, the differential output voltage defined as $V_{OD} = V_Y – V_Z$ is positive. When D is low, the output states reverse: Z turns high, Y becomes low, and VOD is negative. The D pin has an internal pull-up resistor to V_{CC}, thus, when left open while the driver is enabled, output Y turns high and Z turns low.

Table 3. Driver Function Table for THVD1551

INPUT	OUTPUTS		FUNCTIONS
D	Y	Z	
H	H	L	Actively drive bus high
L	L	H	Actively drive bus low
OPEN	H	L	Actively drive bus high by default

When the differential input voltage defined as $V_{ID} = V_A – V_B$ is higher than the positive input threshold, V_{TH+}, the receiver output, R, turns high. When V_{ID} is less than the negative input threshold, $V_{TH–}$, the receiver output, R, turns low. If V_{ID} is between V_{TH+} and $V_{TH–}$ the output is indeterminate. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted to one another (short-circuit), or the bus is not actively driven (idle bus).

Table 4. Receiver Function Table for THVD1551

DIFFERENTIAL INPUT	OUTPUT	FUNCTION
$V_{ID} = V_A – V_B$	R	
$V_{TH+} < V_{ID}$	H	Receive valid bus high
$V_{TH-} < V_{ID} < V_{TH+}$	?	Indeterminate bus state
$V_{ID} < V_{TH-}$	L	Receive valid bus low
Open-circuit bus	H	Fail-safe high output
Short-circuit bus	H	Fail-safe high output
Idle (terminated) bus	H	Fail-safe high output

9.4.3 Device Functional Modes for THVD1512 and THVD1552

When the driver enable pin, DE, is logic high, the differential outputs Y and Z follow the logic states at data input D. A logic high at D causes Y to turn high and Z to turn low. In this case the differential output voltage defined as $V_{OD} = V_Y – V_Z$ is positive. When D is low, the output states reverse: Z turns high, Y becomes low, and V_{OD} is negative.

When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pull-down resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pull-up resistor to V_{CC}, thus, when left open while the driver is enabled, output Y turns high and Z turns low.

Table 5. Driver Function Table for THVD1512 and THVD1552

INPUT	ENABLE	OUTPUTS		FUNCTION
D	DE	Y	Z	
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus high by default

When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A - V_B$ is higher than the positive input threshold, V_{TH+}, the receiver output, R, turns high. When V_{ID} is lower than the negative input threshold, V_{TH-}, the receiver output, R, turns low. If V_{ID} is between V_{TH+} and V_{TH-} the output is indeterminate.

When $\overline{RE}$ is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted to one another (short-circuit), or the bus is not actively driven (idle bus).

Table 6. Receiver Function Table for THVD1512 and THVD1552

DIFFERENTIAL INPUT	ENABLE	OUTPUT	FUNCTION
$V_{ID} = V_A - V_B$	$\overline{RE}$	R	
$V_{TH+} < V_{ID}$	L	H	Receive valid bus high
$V_{TH-} < V_{ID} < V_{TH+}$	L	?	Indeterminate bus state
$V_{ID} < V_{TH-}$	L	L	Receive valid bus low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The THVD15xx family consists of half-duplex and full-duplex RS-485 transceivers commonly used for asynchronous data transmissions. For half-duplex devices, the driver and receiver enable pins allow for the configuration of different operating modes. Full-duplex implementation requires two signal pairs (four wires), and allows each node to transmit data on one pair while simultaneously receiving data on the other pair.

10.2 Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T, whose value matches the characteristic impedance, Z_0, of the cable. This method, known as parallel termination, generally allows for higher data rates over longer cable length.

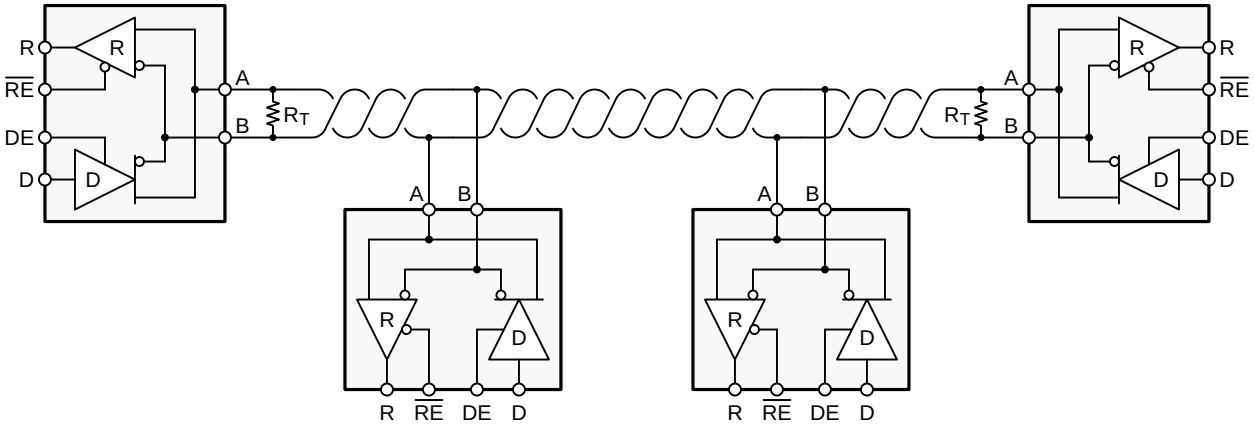


Figure 22. Typical RS-485 Network With Half-Duplex Transceivers

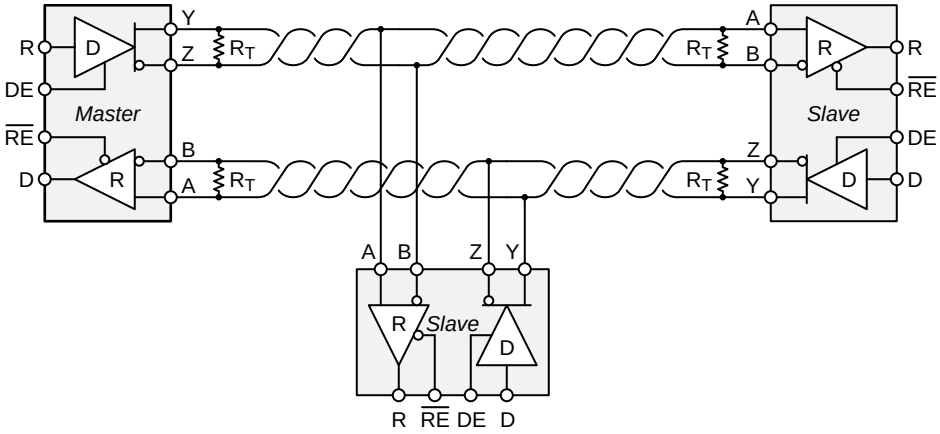


Figure 23. Typical RS-485 Network With Full-Duplex Transceivers

Typical Application (continued)

10.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

10.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and cable length, which means the higher the data rate, the shorter the cable length; and conversely, the lower the data rate, the longer the cable length. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 250 kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

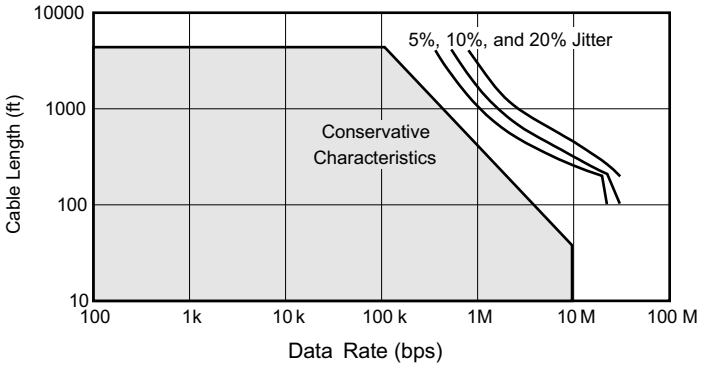


Figure 24. Cable Length vs Data Rate Characteristic

Even higher data rates are achievable (that is, 50 Mbps for the THVD1550, THVD1551 and THVD1552) in cases where the interconnect is short enough (or has suitably low attenuation at signal frequencies) to not degrade the data.

10.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections of varying phase as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in Equation 1.

$$L_{(STUB)} \leq 0.1 \times t_r \times v \times c \quad (1)$$

where

- t_r is the 10/90 rise time of the driver
- c is the speed of light (3×10^8 m/s)
- v is the signal velocity of the cable or trace as a factor of c

10.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to drive 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12 kΩ. Because the THVD15xx family consists of 1/8 UL transceivers, connecting up to 256 receivers to the bus is possible.

Typical Application (continued)

10.2.1.4 Receiver Failsafe

The differential receivers of the THVD15xx family are failsafe to invalid bus states caused by the following:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver will output a failsafe logic high state so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds such that the input indeterminate range does not include zero volts differential. In order to comply with the RS-422 and RS-485 standards, the receiver output must output a high when the differential input V_{ID} is more positive than 200 mV, and must output a low when V_{ID} is more negative than –200 mV. The receiver parameters which determine the failsafe performance are V_{TH+}, $V_{TH–}$, and V_{HYS} (the separation between V_{TH+} and $V_{TH–}$). As shown in the Electrical Characteristics table, differential signals more negative than –200 mV will always cause a low receiver output, and differential signals more positive than 200 mV will always cause a high receiver output.

When the differential input signal is close to zero, it is still above the V_{TH+} threshold, and the receiver output will be high. Only when the differential input is more than V_{HYS} below V_{TH+} will the receiver output transition to a low state. Therefore, the noise immunity of the receiver inputs during a bus fault conditions includes the receiver hysteresis value, V_{hys}, as well as the value of V_{TH+}.

Typical Application (continued)

10.2.1.5 Transient Protection

The bus pins of the THVD15xx transceiver family include on-chip ESD protection against ±30-kV HBM and ±18-kV IEC 61000-4-2 contact discharge. The International Electrotechnical Commission (IEC) ESD test is far more severe than the HBM ESD test. The 50% higher charge capacitance, $C_{(S)}$, and 78% lower discharge resistance, $R_{(D)}$, of the IEC model produce significantly higher discharge currents than the HBM model. As stated in the IEC 61000-4-2 standard, contact discharge is the preferred transient protection test method.

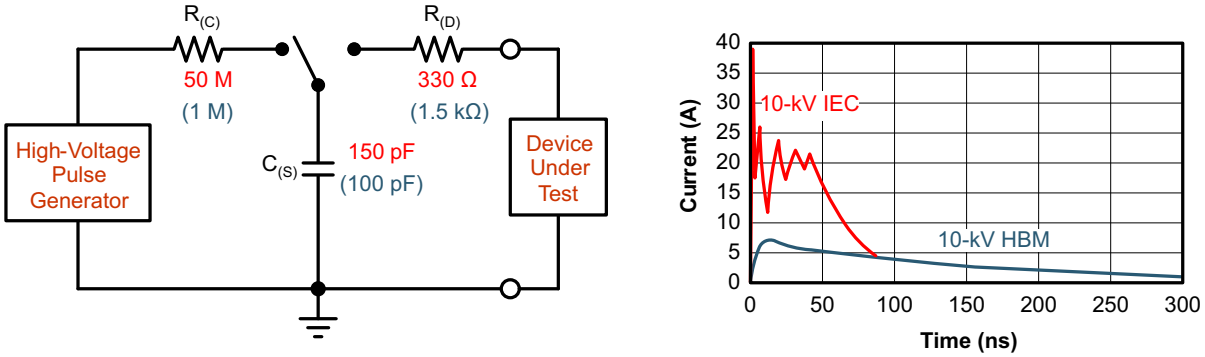


Figure 25. HBM and IEC ESD Models and Currents in Comparison (HBM Values in Parenthesis)

The on-chip implementation of IEC ESD protection significantly increases the robustness of equipment. Common discharge events occur because of human contact with connectors and cables. Designers may choose to implement protection against longer duration transients, typically referred to as surge transients.

EFTs are generally caused by relay-contact bounce or the interruption of inductive loads. Surge transients often result from lightning strikes (direct strike or an indirect strike which induce voltages and currents), or the switching of power systems, including load changes and short circuit switching. These transients are often encountered in industrial environments, such as factory automation and power-grid systems.

Figure 26 compares the pulse power of the EFT and surge transients with the power caused by an IEC ESD transient. The left-hand diagram shows the relative pulse-power for a 0.5-kV surge transient and 4-kV EFT transient, both of which dwarf the 10-kV ESD transient visible in the lower-left corner. 500-V surge transients are representative of events that may occur in factory environments in industrial and process automation.

The right-hand diagram shows the pulse-power of a 6-kV surge transient, relative to the same 0.5-kV surge transient. 6-kV surge transients are most likely to occur in power generation and power-grid systems.

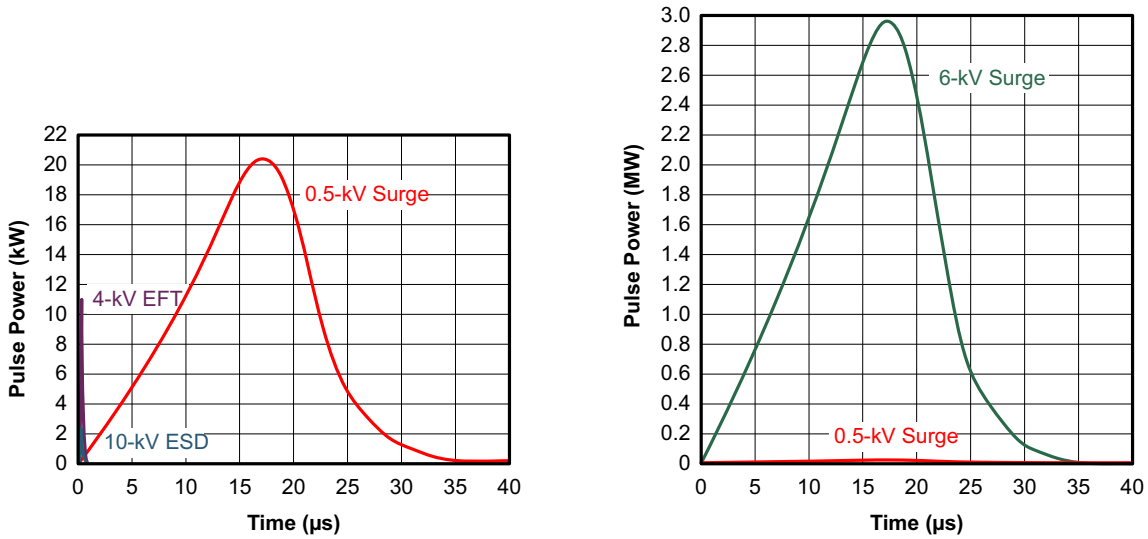


Figure 26. Power Comparison of ESD, EFT, and Surge Transients

Typical Application (continued)

In the case of surge transients, high-energy content is characterized by long pulse duration and slow decaying pulse power. The electrical energy of a transient that is dumped into the internal protection cells of a transceiver is converted into thermal energy, which heats and destroys the protection cells, thus destroying the transceiver. Figure 27 shows the large differences in transient energies for single ESD, EFT, surge transients, and an EFT pulse train that is commonly applied during compliance testing.

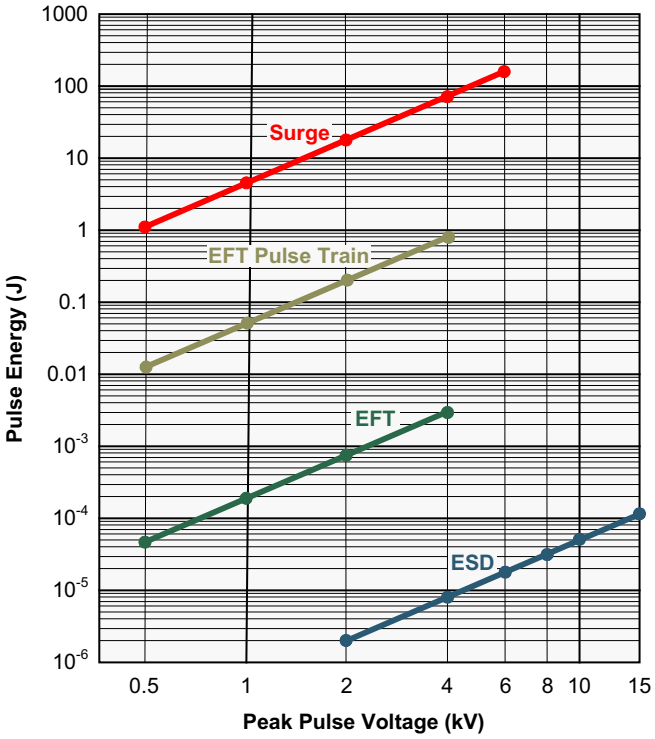


Figure 27. Comparison of Transient Energies

10.2.2 Detailed Design Procedure

Figure 28 and Figure 29 suggest a protection circuit against 1 kV surge (IEC 61000-4-5) transients. Table 7 shows the associated bill of materials.

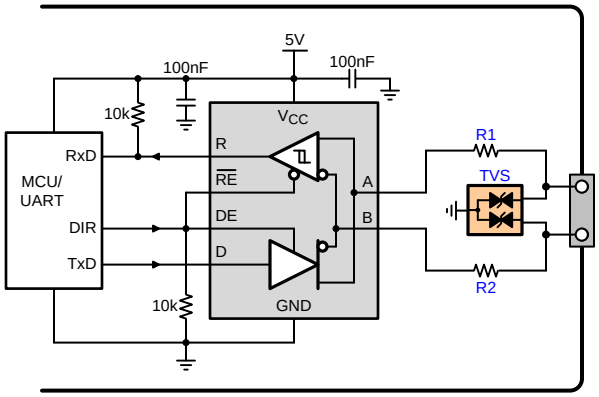


Figure 28. Transient Protection Against Surge Transients for Half-Duplex Devices

Typical Application (continued)

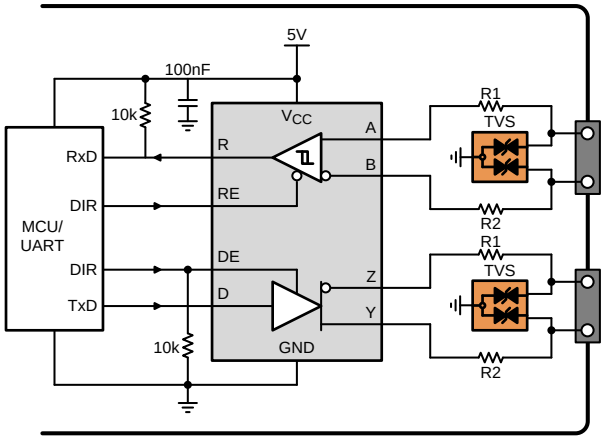
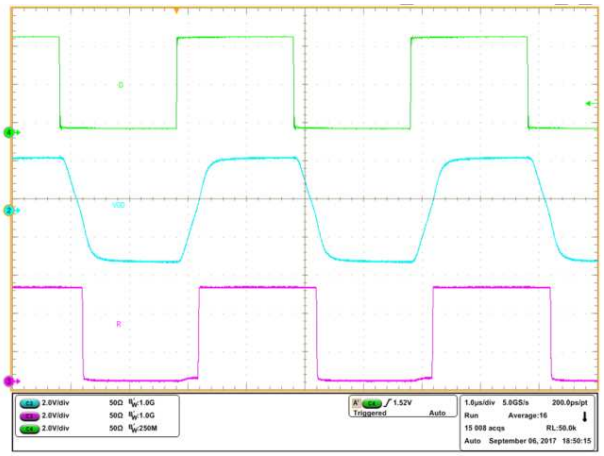


Figure 29. Transient Protection Against Surge Transients for Full-Duplex Devices

Table 7. Bill of Materials

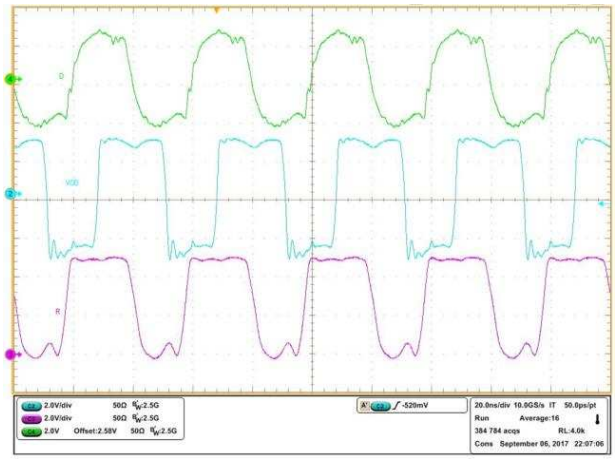
DEVICE	FUNCTION	ORDER NUMBER	MANUFACTURER
XCVR	5-V, RS-485 transceiver	THVD15xx	TI
R1	10-Ω, pulse-proof thick-film resistor	CRCW0603010RJNEAHP	Vishay
R2			
TVS	Bidirectional 400-W transient suppressor	CDSOT23-SM712	Bourns

10.2.3 Application Curves



500 kbps

Figure 30. THVD1510 Waveforms with 60-Ω Termination



50 Mbps

Figure 31. THVD1550 Waveforms with 60-Ω Termination

11 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply should be decoupled with a 100 nF ceramic capacitor located as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes.

12 Layout

12.1 Layout Guidelines

Robust and reliable bus node design often requires the use of external transient protection devices in order to protect against surge transients that may occur in industrial environments. Since these transients have a wide frequency bandwidth (from approximately 3 MHz to 300 MHz), high-frequency layout techniques should be applied during PCB design.

1. Place the protection circuitry close to the bus connector to prevent noise transients from propagating across the board.
2. Use V_{CC} and ground planes to provide low inductance. Note that high-frequency currents tend to follow the path of least impedance and not the path of least resistance.
3. Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
4. Apply 100-nF to 220-nF decoupling capacitors as close as possible to the V_{CC} pins of transceiver, UART and/or controller ICs on the board.
5. Use at least two vias for V_{CC} and ground connections of decoupling capacitors and protection devices to minimize effective via inductance.
6. Use 1-kΩ to 10-kΩ pullup and pulldown resistors for enable lines to limit noise currents in these lines during transient events.
7. Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
8. While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1 mA.

12.2 Layout Example

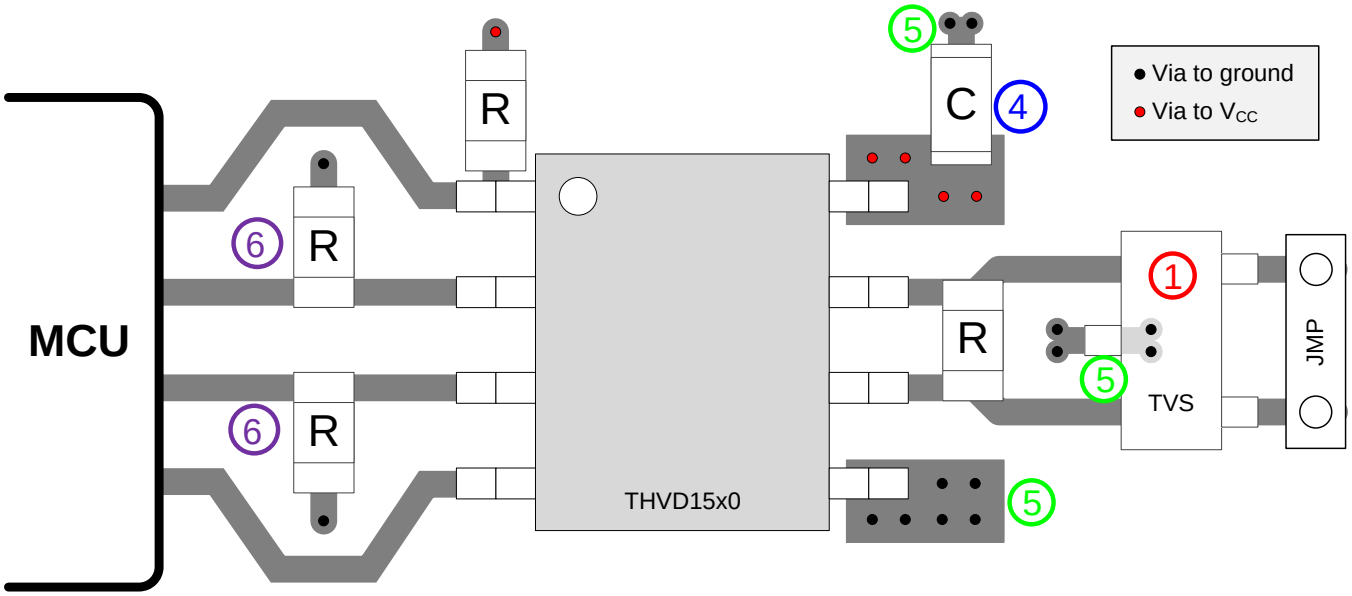


Figure 32. Half-Duplex Layout Example

13 Device and Documentation Support

13.1 Device Support

13.2 Third-Party Products Disclaimer

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13.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 8. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
THVD1510	Click here	Click here	Click here	Click here	Click here
THVD1512	Click here	Click here	Click here	Click here	Click here
THVD1550	Click here	Click here	Click here	Click here	Click here
THVD1551	Click here	Click here	Click here	Click here	Click here
THVD1552	Click here	Click here	Click here	Click here	Click here

13.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates — go to the product folder for your device on ti.com. In the upper right-hand corner, click the *Alert me* button to register and receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

13.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.6 Trademarks

E2E is a trademark of Texas Instruments.

13.7 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

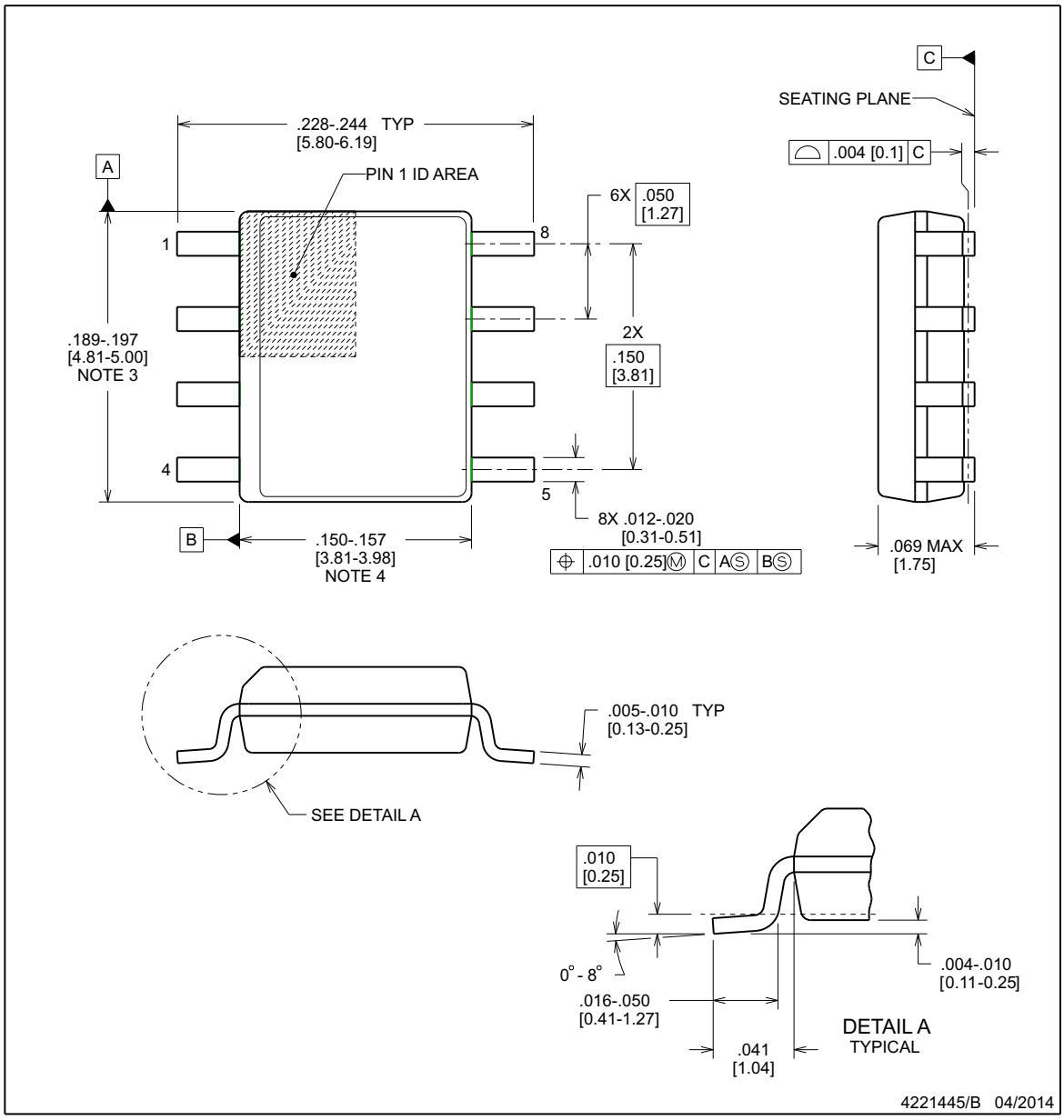
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

D0008B

SOIC - 1.75 mm max height

SOIC



NOTES:

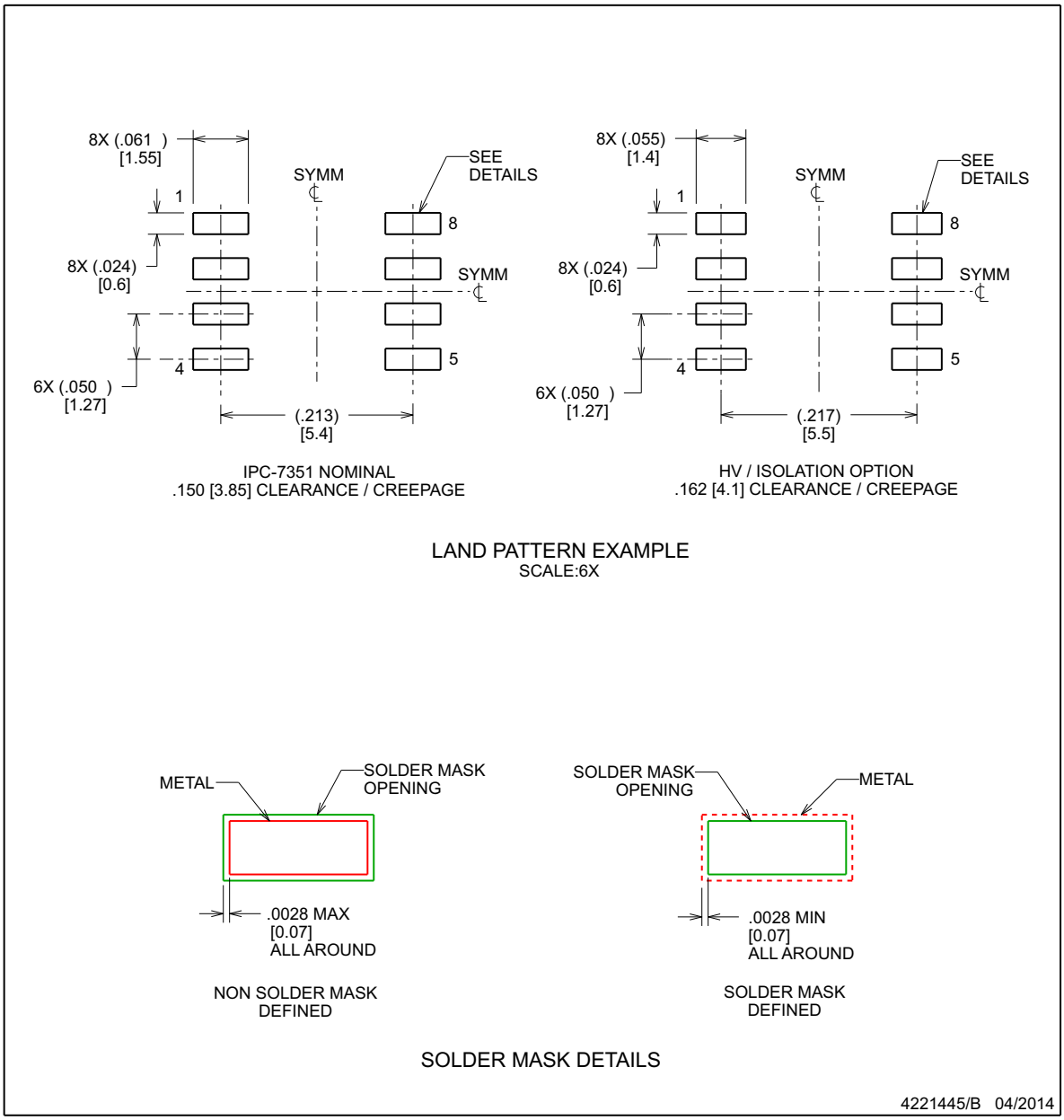
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15], per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008B

SOIC - 1.75 mm max height

SOIC



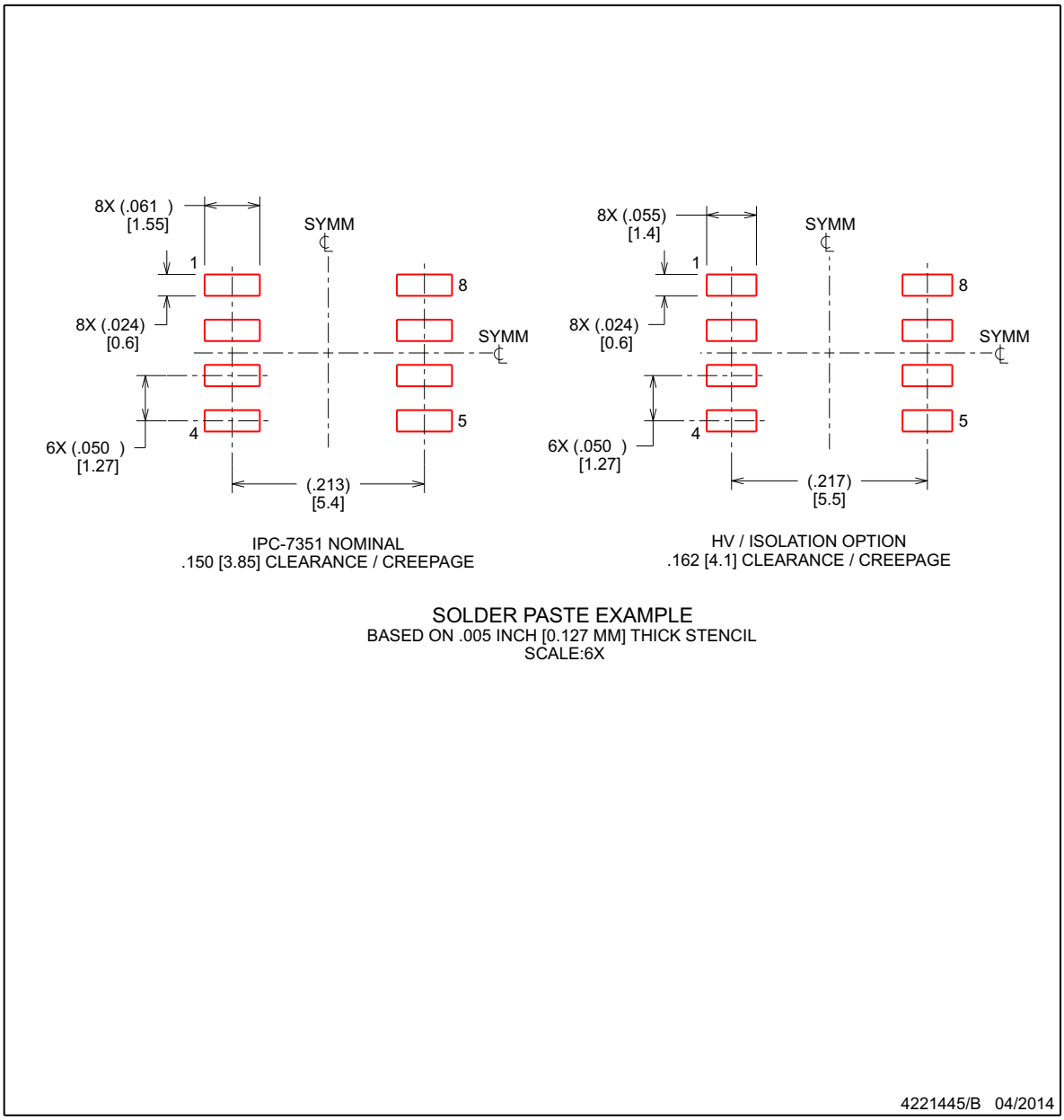
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008B — **SOIC - 1.75 mm max height**

SOIC

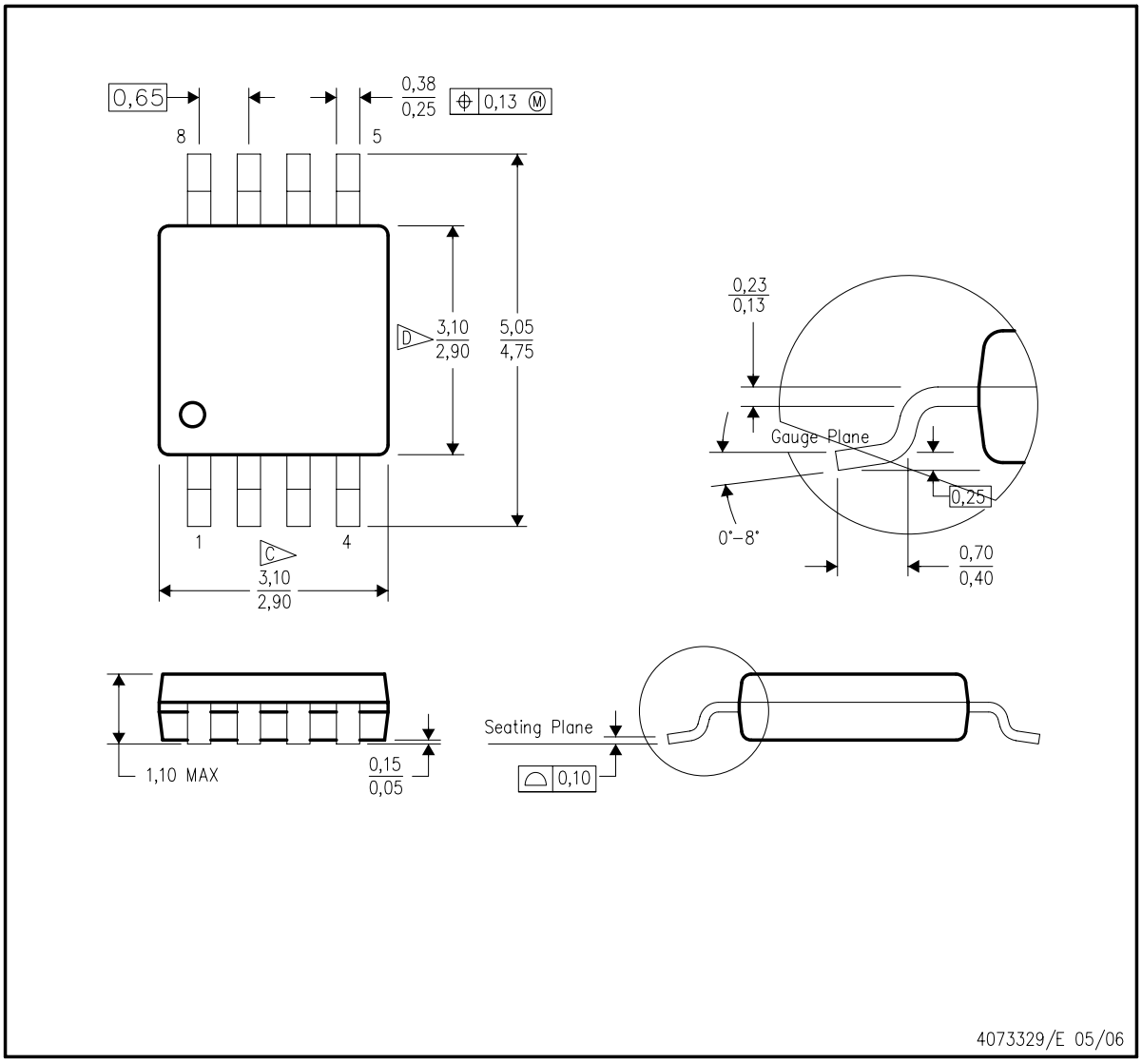


NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

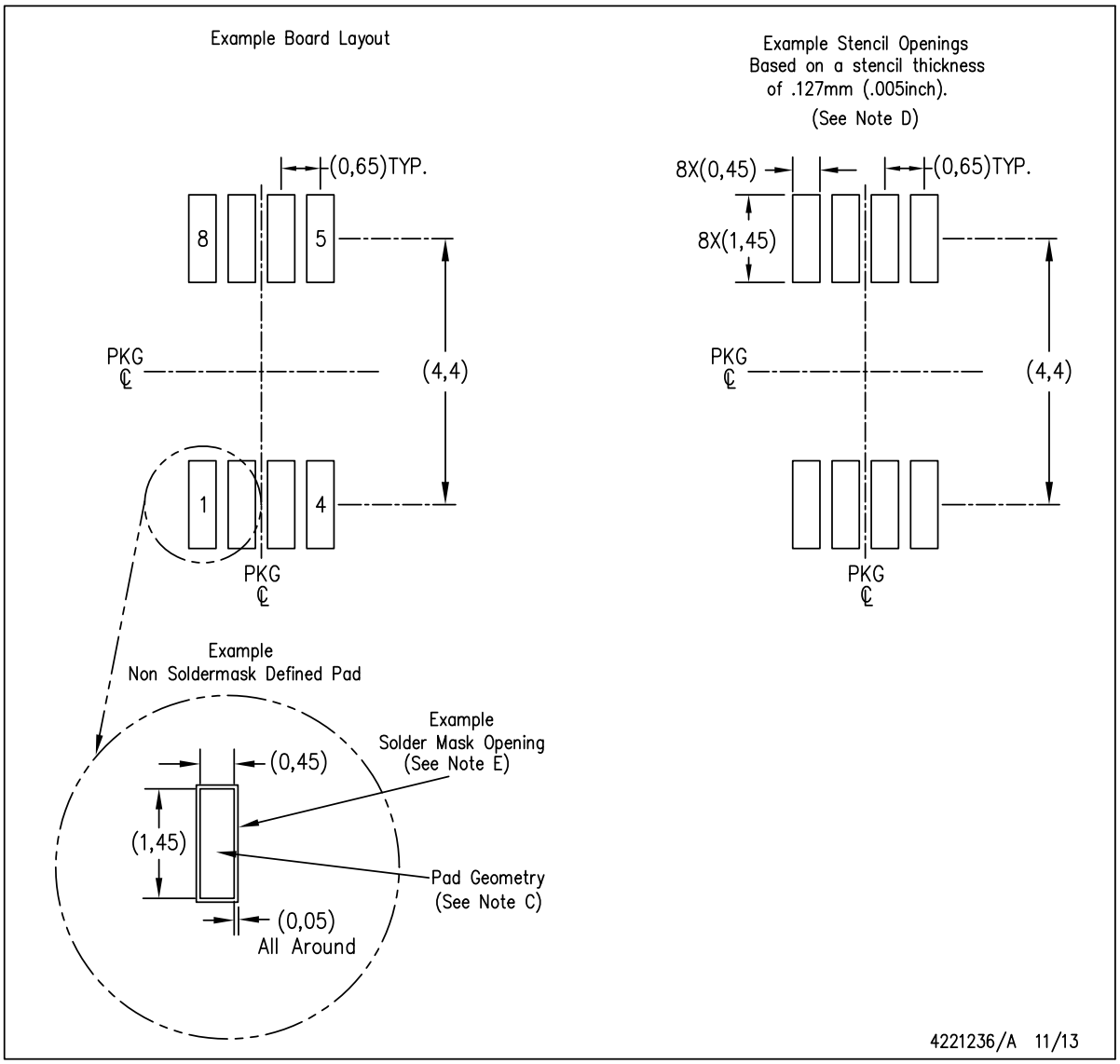
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

LAND PATTERN DATA

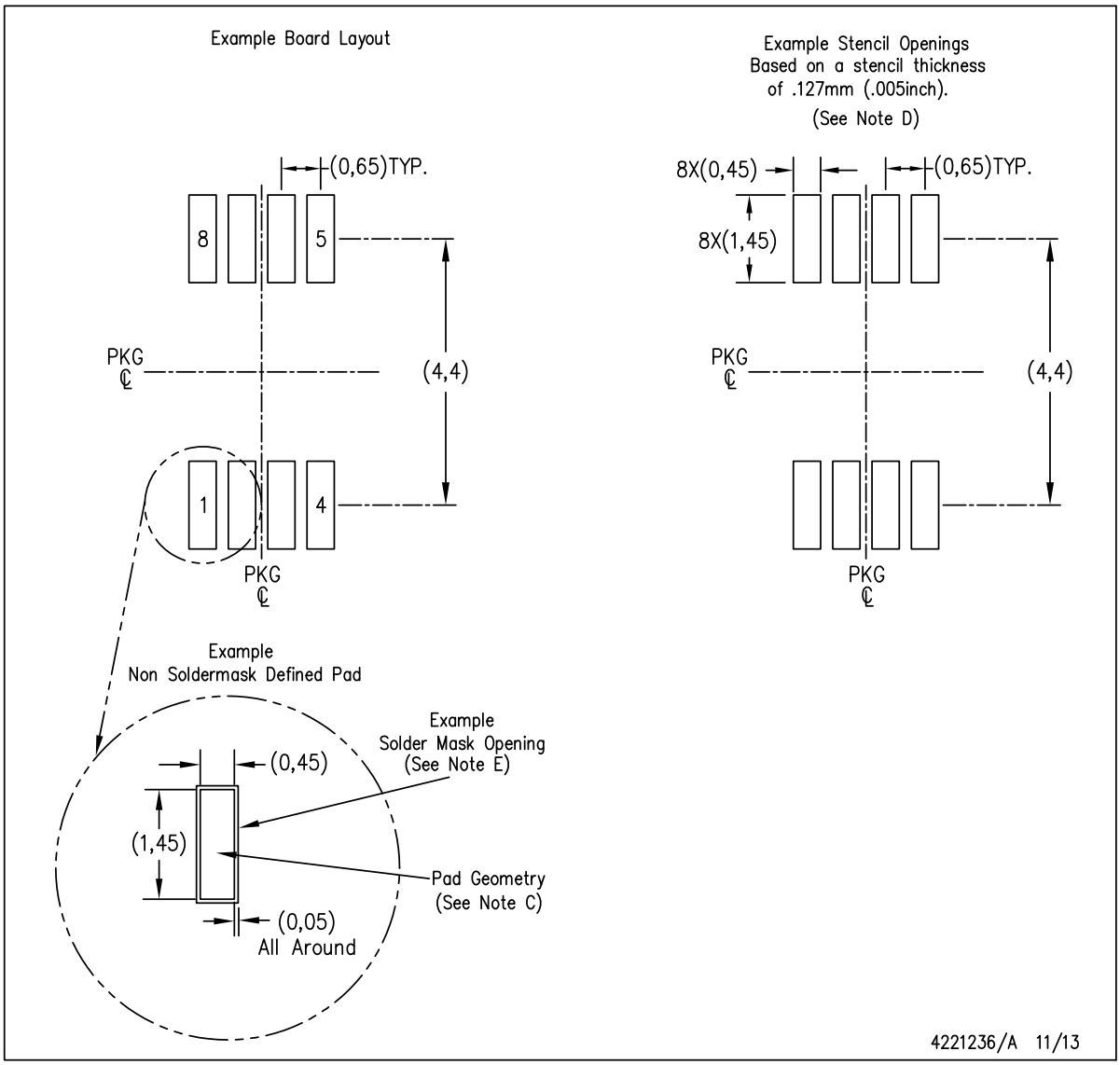
DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

LAND PATTERN DATA

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



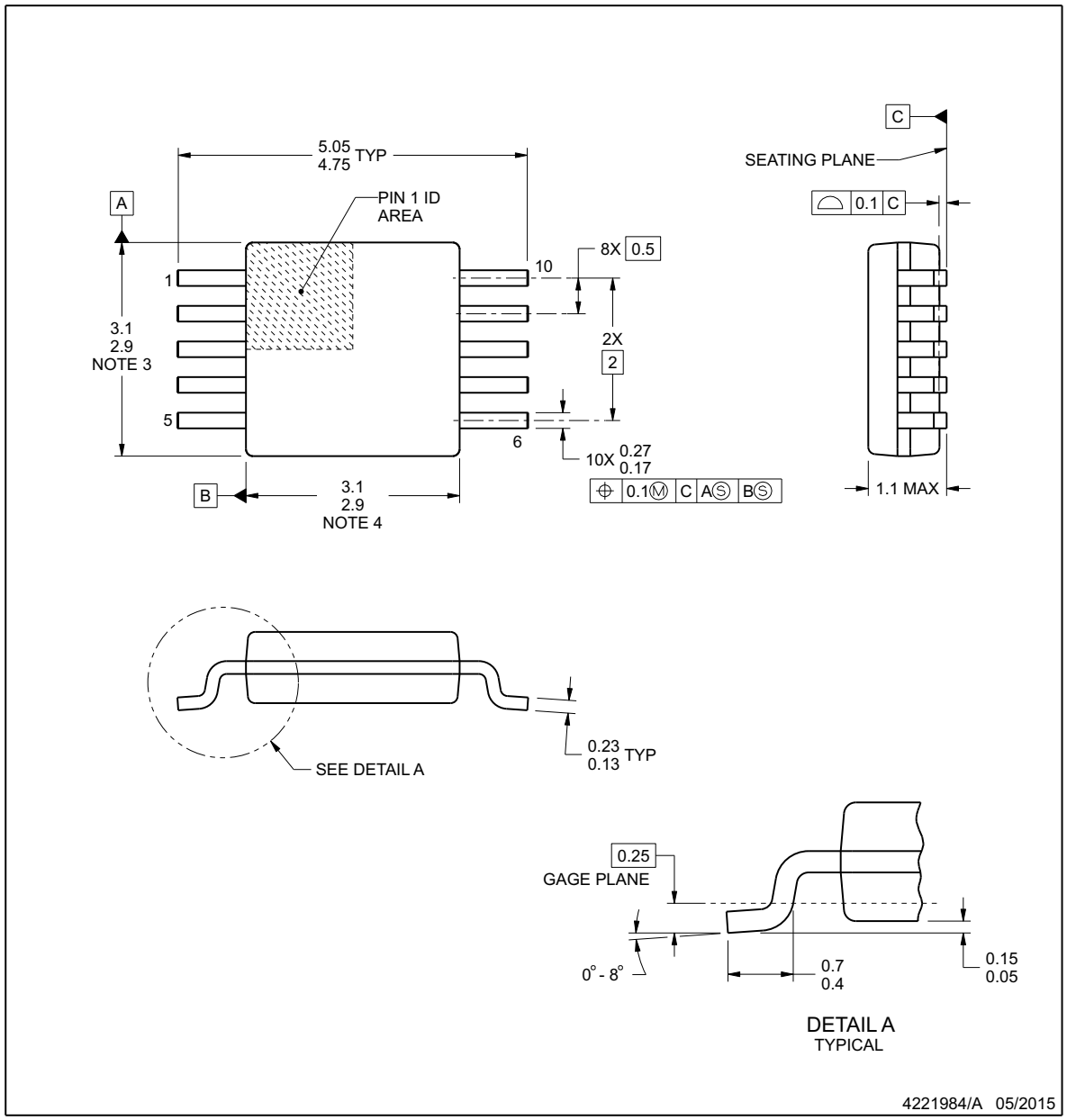
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES:

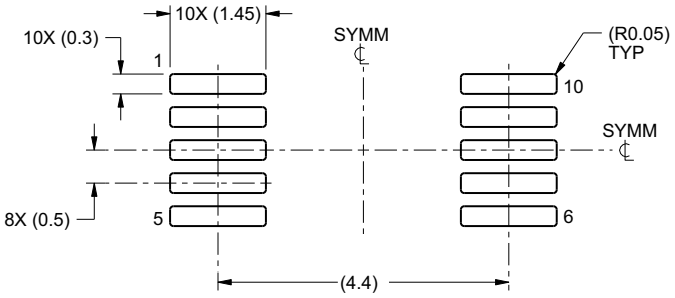
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

EXAMPLE BOARD LAYOUT

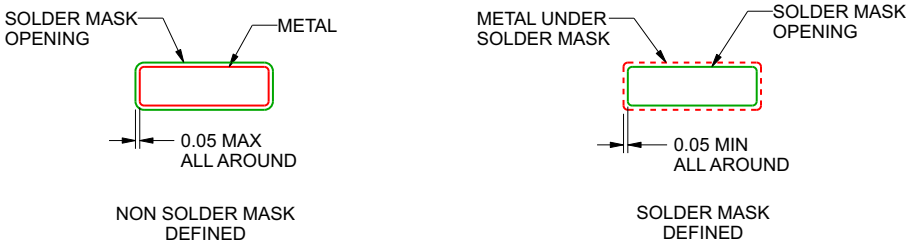
DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

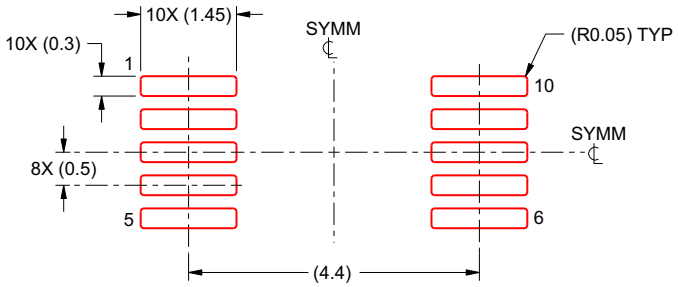
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGS0010A — **VSSOP - 1.1 mm max height**

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THVD1510D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VD1510	Samples
THVD1510DGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1510	Samples
THVD1510DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1510	Samples
THVD1510DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VD1510	Samples
THVD1512DGS	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1512	Samples
THVD1512DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 125	1512	Samples
THVD1550D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VD1550	Samples
THVD1550DGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1550	Samples
THVD1550DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1550	Samples
THVD1550DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VD1550	Samples
THVD1551DGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1551	Samples
THVD1551DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1551	Samples
THVD1552D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1552	Samples
THVD1552DGS	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1552	Samples
THVD1552DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 125	1552	Samples
THVD1552DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1552	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

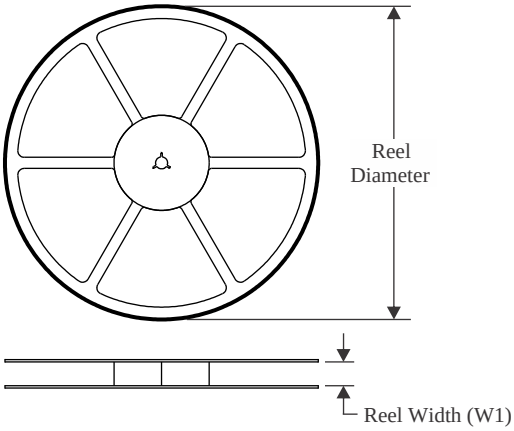
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

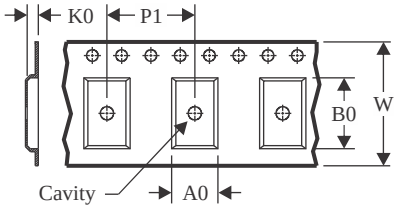
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

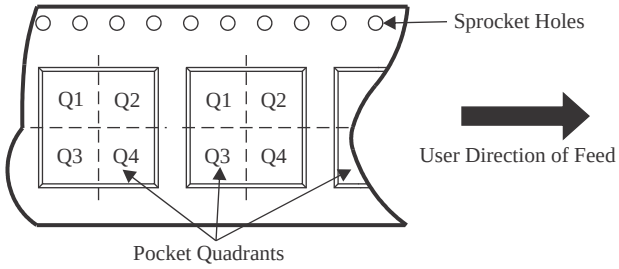


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

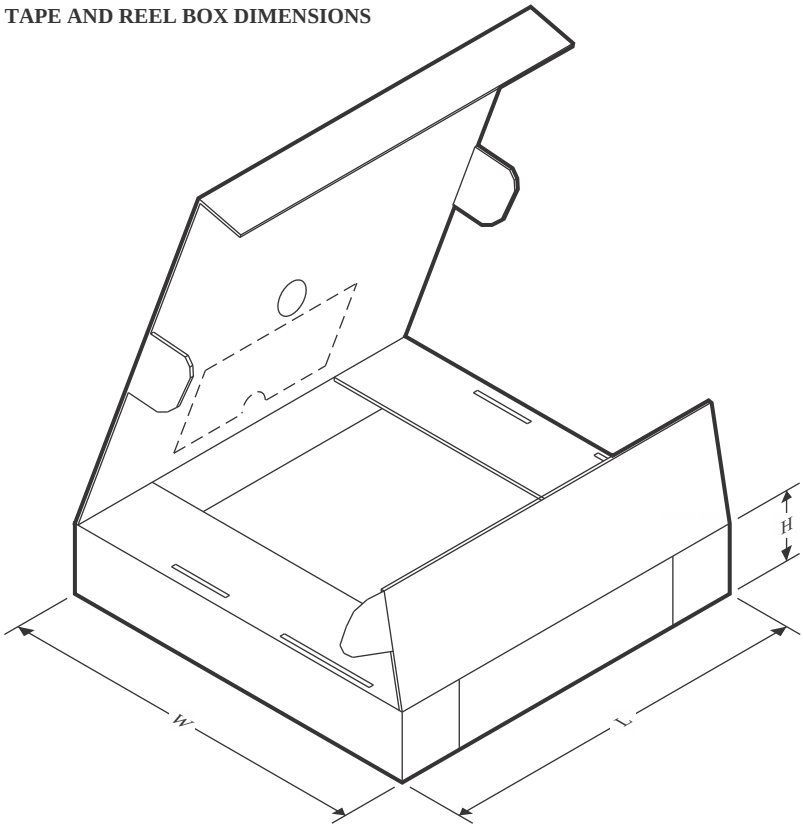
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THVD1510DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THVD1510DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
THVD1510DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THVD1512DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
THVD1550DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THVD1550DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THVD1551DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THVD1552DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
THVD1552DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

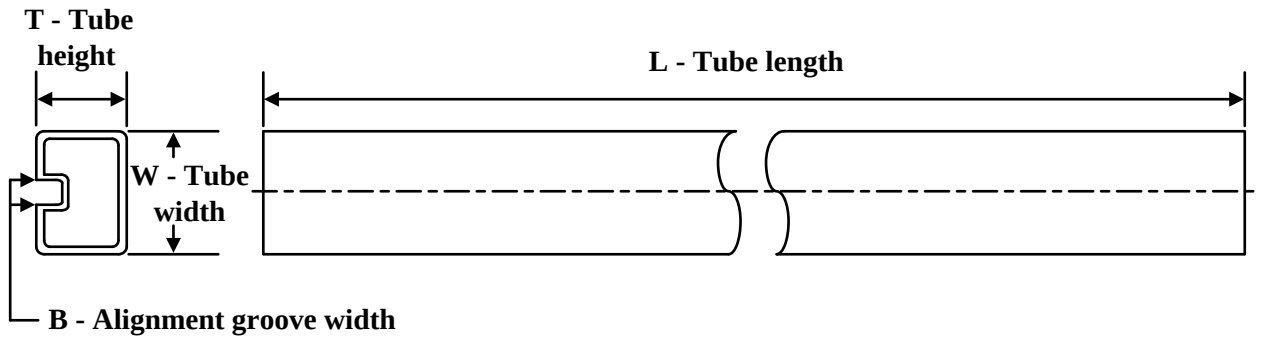
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THVD1510DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
THVD1510DGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
THVD1510DR	SOIC	D	8	2500	353.0	353.0	32.0
THVD1512DGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
THVD1550DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
THVD1550DR	SOIC	D	8	2500	353.0	353.0	32.0
THVD1551DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
THVD1552DGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
THVD1552DR	SOIC	D	14	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
THVD1510D	D	SOIC	8	75	507	8	3940	4.32
THVD1510DGK	DGK	VSSOP	8	80	330	6.55	500	2.88
THVD1512DGS	DGS	VSSOP	10	80	330	6.55	500	2.88
THVD1550D	D	SOIC	8	75	507	8	3940	4.32
THVD1550DGK	DGK	VSSOP	8	80	330	6.55	500	2.88
THVD1551DGK	DGK	VSSOP	8	80	274	6.55	500	2.88
THVD1552D	D	SOIC	14	50	507	8	3940	4.32
THVD1552DGS	DGS	VSSOP	10	80	330	6.55	500	2.88

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