

# TL03x, TL03xA ENHANCED-JFET LOW-POWER LOW-OFFSET OPERATIONAL AMPLIFIERS

SLOS180C – FEBRUARY 1997 – REVISED DECEMBER 2001

- Direct Upgrades for the TL06x Low-Power BiFETs
- Low Power Consumption . . . 6.5 mW/Channel Typ
- On-Chip Offset-Voltage Trimming for Improved DC Performance (1.5 mV, TL031A)
- Higher Slew Rate and Bandwidth Without Increased Power Consumption
- Available in TSSOP for Small Form-Factor Designs

## description

The TL03x series of JFET-input operational amplifiers offer improved dc and ac characteristics over the TL06x family of low-power BiFET operational amplifiers. On-chip zener trimming of offset voltage yields precision grades as low as 1.5 mV (TL031A) for greater accuracy in dc-coupled applications. The Texas Instruments improved BiFET process and optimized designs also yield improved bandwidths and slew rates without increased power consumption. The TL03x devices are pin-compatible with the TL06x and can be used to upgrade existing circuits or for optimal performance in new designs.

BiFET operational amplifiers offer the inherently higher input impedance of the JFET-input transistors without sacrificing the output drive associated with bipolar amplifiers. This higher input impedance makes the TL3x amplifiers better suited for interfacing with high-impedance sensors or very low-level ac signals. These devices also feature inherently better ac response than bipolar or CMOS devices having comparable power consumption.

The TL03x family has been optimized for micropower operation, while improving on the performance of the TL06x series. Designers requiring significantly faster ac response should consider the Excalibur™ TLE206x family of low-power BiFET operational amplifiers.

Because BiFET operational amplifiers are designed for use with dual power supplies, care must be taken to observe common-mode input-voltage limits and output swing when operating from a single supply. DC biasing of the input signal is required, and loads should be terminated to a virtual-ground node at midsupply. The TI TLE2426 integrated virtual-ground generator is useful when operating BiFET amplifiers from single supplies.

The TL03x devices are fully specified at  $\pm 15$  V and  $\pm 5$  V. For operation in low-voltage and/or single-supply systems, the TI LinCMOS families of operational amplifiers (TLC prefix) are recommended. When moving from BiFET to CMOS amplifiers, particular attention should be paid to slew rate, bandwidth requirements, and output loading.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from -40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of -55°C to 125°C.



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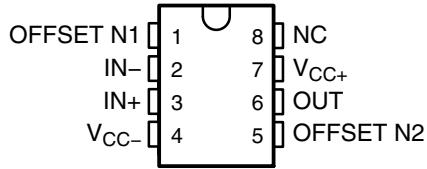
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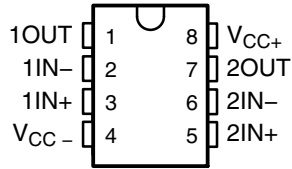
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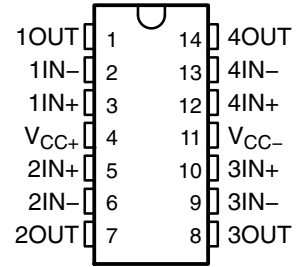
**TL031x, TL031Ax**  
D, JG, OR P PACKAGE  
(TOP VIEW)



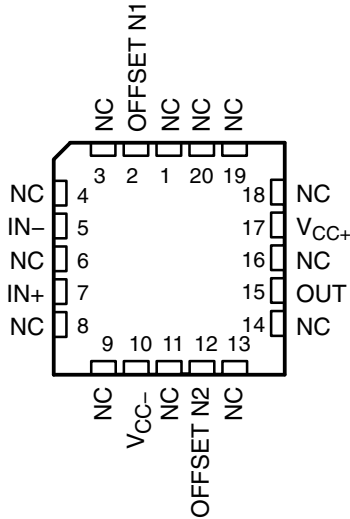
**TL032x, TL032Ax**  
D, JG, OR P PACKAGE  
(TOP VIEW)



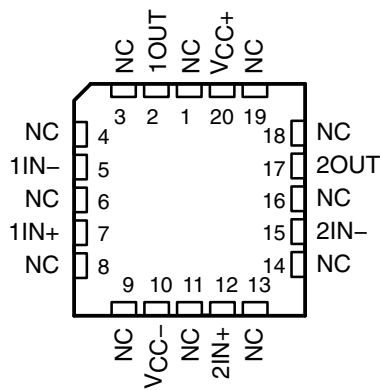
**TL034x, TL034Ax**  
D, J, N, OR PW PACKAGE  
(TOP VIEW)



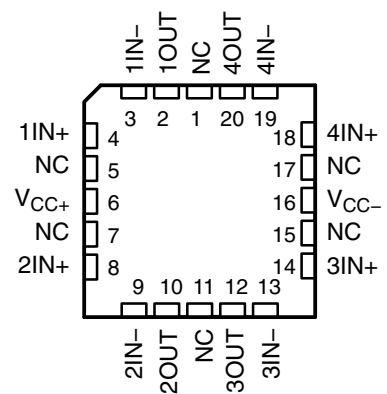
**TL031M, TL031AM**  
FK PACKAGE  
(TOP VIEW)



**TL032M, TL032AM**  
FK PACKAGE  
(TOP VIEW)



**TL034M, TL034AM**  
FK PACKAGE  
(TOP VIEW)



NC – No internal connection

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## AVAILABLE OPTIONS

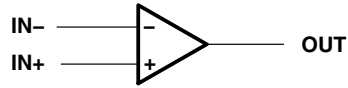
T <sub>A</sub>	V <sub>IO</sub> MAX AT 25°C	PACKAGED DEVICES						
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	CERAMIC DIP (JG)	PLASTIC DIP (N)	PLASTIC DIP (P)	TSSOP (PW)
0°C to 70°C	0.8 mV	TL031ACD TL032ACD	—	—	—	—	TL031ACP TL032ACP	—
	1.5 mV	TL031CD TL032CD TL034ACD	—	—	—	TL034ACN	TL031CP TL032CP	—
	4 mV	TL034CD	—	—	—	TL034CN	—	TL034CPW
–40°C to 85°C	0.8 mV	TL031AID TL032AID	—	—	—	—	TL031AIP TL032AIP	—
	1.5 mV	TL031ID TL032ID TL034AID	—	—	—	TL034AIN	TL031IP TL032IP	—
	4 mV	TL034ID	—	—	—	TL034IN	—	—
–55°C to 125°C	0.8 mV	TL031AMD TL032AMD	TL031AMFK TL032AMFK	—	TL031AMJG TL032AMJG	—	TL031AMP TL032AMP	—
	1.5 mV	TL031MD TL032MD TL034AMD	TL031MFK TL032MFK TL034AMFK	TL034AMJ	TL031MJG TL032MJG	TL034AMN	TL031MP TL032MP	—
	4 mV	TL034MD	TL034MFK	TL034MJ	—	TL034MN	—	—

The D and PW packages are available taped and reeled and are indicated by adding an R suffix to device type (e.g., TL034CDR or TL034CPWR).

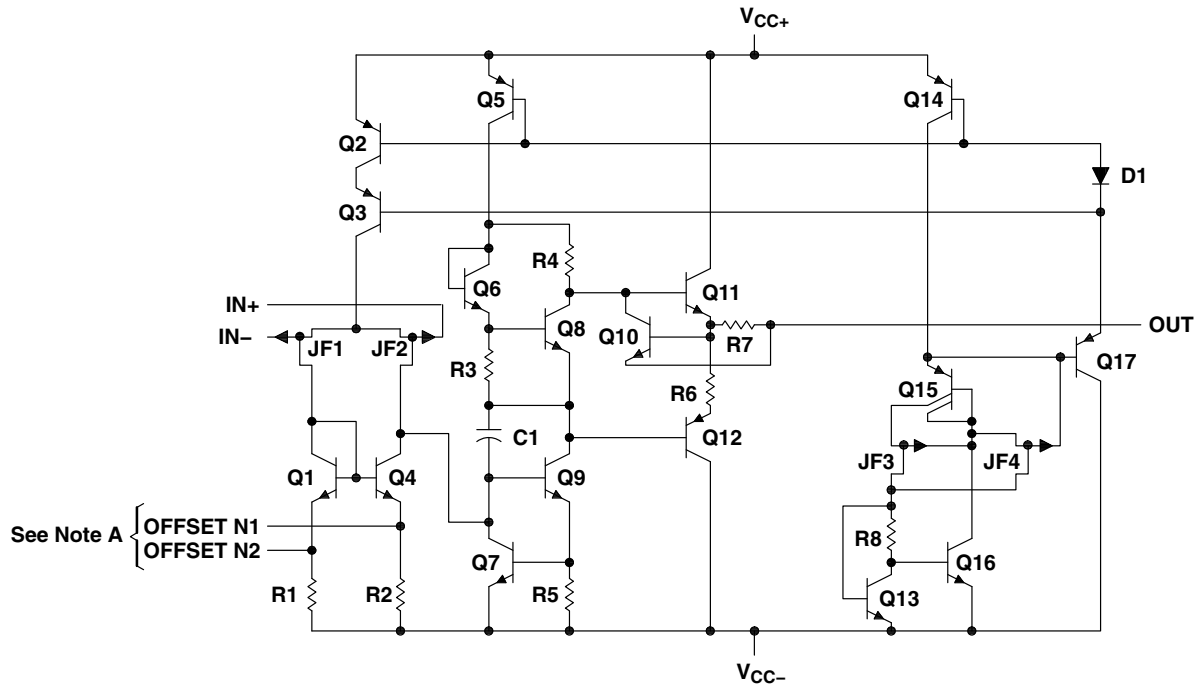
# TL03x, TL03xA ENHANCED-JFET LOW-POWER LOW-OFFSET OPERATIONAL AMPLIFIERS

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symbol (each amplifier)



equivalent schematic (each amplifier)



NOTE A: OFFSET N1 and OFFSET N2 are available only on the TL031, TL031A.

# TL03x, TL03xA ENHANCED-JFET LOW-POWER LOW-OFFSET OPERATIONAL AMPLIFIERS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (see Note 1): $V_{CC+}$ .....	18 V
$V_{CC-}$ .....	-18 V
Differential input voltage, $V_{ID}$ (see Note 2) .....	$\pm 30$ V
Input voltage, $V_I$ (any input) (see Notes 1 and 3) .....	$\pm 15$ V
Input current, $I_I$ (each input) .....	$\pm 1$ mA
Output current, $I_O$ (each output) .....	$\pm 40$ mA
Total current into $V_{CC+}$ .....	160 mA
Total current out of $V_{CC-}$ .....	160 mA
Duration of short-circuit current at (or below) 25°C (see Note 4) .....	Unlimited
Continuous total power dissipation .....	See Dissipation Rating Table
Package thermal impedance, $\theta_{JA}$ (see Note 5): D package (8 pin) .....	97°C/W
D package (14 pin) .....	86°C/W
N package .....	80°C/W
P package .....	85°C/W
PW package .....	113°C/W
Lead temperature 1,6 mm (1 /16 inch) from case for 10 seconds: D, N, P, or PW package .....	260°C
Lead temperature 1,6 mm (1 /16 inch) from case for 60 seconds: J or JG package .....	300°C
Case temperature for 60 seconds: FK package .....	260°C
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
- All voltage values, except differential voltages, are with respect to the midpoint between  $V_{CC+}$  and  $V_{CC-}$ .
  - Differential voltages are at  $IN+$  with respect to  $IN-$ .
  - The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
  - The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.
  - The package thermal impedance is calculated in accordance with JESD 51-7.

**DISSIPATION RATING TABLE**

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW

## recommended operating conditions

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$V_{CC\pm}$	Supply voltage	$\pm 5$	$\pm 15$	$\pm 5$	$\pm 15$	$\pm 5$	$\pm 15$	V
$V_{IC}$	Common-mode input voltage	$V_{CC\pm} = \pm 5$ V		-1.5	4	-1.5	4	V
		$V_{CC\pm} = \pm 15$ V		-11.5	14	-11.5	14	
$T_A$	Operating free-air temperature	0	70	-40	85	-55	125	°C



# TL03x, TL03xA ENHANCED-JFET LOW-POWER LOW-OFFSET OPERATIONAL AMPLIFIERS

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## TL031C and TL031AC electrical characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS		T <sub>A</sub>	TL031C, TL031AC						UNIT
				V <sub>CC±</sub> = ±5 V			V <sub>CC±</sub> = ±15 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>IO</sub> Input offset voltage	V <sub>O</sub> = 0, V <sub>IC</sub> = 0, R <sub>S</sub> = 50 Ω	TL031C	25°C	0.54 3.5		0.5 1.5		mV		
			Full range†	4.5		2.5				
		TL031AC	25°C	0.41	2.8	0.34	0.8			
			Full range†	3.8		1.8				
α <sub>V<sub>IO</sub></sub> Temperature coefficient of input offset voltage	V <sub>O</sub> = 0, V <sub>IC</sub> = 0, R <sub>S</sub> = 50 Ω	TL031C	25°C to 70°C	7.1		5.9		μV/°C		
		TL031AC	25°C to 70°C	7.1		5.9 25				
Input offset voltage long-term drift‡	V <sub>O</sub> = 0, V <sub>IC</sub> = 0, R <sub>S</sub> = 50 Ω		25°C	0.04		0.04		μV/mo		
I <sub>IO</sub> Input offset current	V <sub>O</sub> = 0, V <sub>IC</sub> = 0 See Figure 5		25°C	1	100	1	100	pA		
			70°C	9	200	12	200			
I <sub>IB</sub> Input bias current	V <sub>O</sub> = 0, V <sub>IC</sub> = 0 See Figure 5		25°C	2	200	2	200	pA		
			70°C	50	400	80	400			
V <sub>ICR</sub> Common-mode input voltage range			25°C	-1.5 to 4	-3.4 to 5.4	-11.5 to 14	-13.4 to 15.4	V		
			Full range†	-1.5 to 4		-11.5 to 14				
V <sub>OM+</sub> Maximum positive peak output voltage swing	R <sub>L</sub> = 10 kΩ		25°C	3	4.3	13	14	V		
			0°C	3	4.2	13	14			
			70°C	3	4.3	13	14			
V <sub>OM-</sub> Maximum negative peak output voltage swing	R <sub>L</sub> = 10 kΩ		25°C	-3	-4.2	-12.5	-13.9	V		
			0°C	-3	-4.1	-12.5	-13.9			
			70°C	-3	-4.2	-12.5	-14			
A <sub>VD</sub> Large-signal differential voltage amplification§	R <sub>L</sub> = 10 kΩ		25°C	4	12	5	14.3	V/mV		
			0°C	3	11.1	4	13.5			
			70°C	4	13.3	5	15.2			
r <sub>i</sub> Input resistance			25°C	10 <sup>12</sup>		10 <sup>12</sup>		Ω		
c <sub>i</sub> Input capacitance			25°C	5		4		pF		
CMRR Common-mode rejection ratio	V <sub>IC</sub> = V <sub>ICRmin</sub> , V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω		25°C	70	87	75	94	dB		
			0°C	70	87	75	94			
			70°C	70	87	75	94			
k <sub>SVR</sub> Supply-voltage rejection ratio (ΔV <sub>CC±</sub> /ΔV <sub>IO</sub> )	V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω		25°C	75	96	75	96	dB		
			0°C	75	96	75	96			
			70°C	75	96	75	96			

† Full range is 0°C to 70°C.

‡ Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T<sub>A</sub> = 150°C extrapolated to T<sub>A</sub> = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

§ At V<sub>CC±</sub> = ±5 V, V<sub>O</sub> = ±2.3 V; at V<sub>CC±</sub> = ±15 V, V<sub>O</sub> = ±10 V



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**TL031C and TL031AC electrical characteristics at specified free-air temperature (continued)**

PARAMETER	TEST CONDITIONS	T <sub>A</sub>	TL031C, TL031AC						UNIT
			V <sub>CC±</sub> = ±5 V			V <sub>CC±</sub> = ±15 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
P <sub>D</sub> Total power dissipation	V <sub>O</sub> = 0, No load	25°C		1.9	2.5		6.5	8.4	mW
		0°C		1.8	2.5		6.3	8.4	
		70°C		1.9	2.5		6.3	8.4	
I <sub>CC</sub> Supply current	V <sub>O</sub> = 0, No load	25°C		192	250		217	280	μA
		0°C		184	250		211	280	
		70°C		189	250		210	280	

**TL031C and TL031AC operating characteristics at specified free-air temperature**

PARAMETER	TEST CONDITIONS	T <sub>A</sub>	TL031C, TL031AC						UNIT
			V <sub>CC±</sub> = ±5 V			V <sub>CC±</sub> = ±15 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
SR <sup>+</sup> Positive slew rate at unity gain <sup>†</sup>	R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF See Figure 1	25°C		2		1.5	2.9	V/μs	
		0°C		1.8		1	2.6		
		70°C		2.2		1.5	3.2		
SR <sup>-</sup> Negative slew rate at unity gain <sup>†</sup>	R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF See Figure 1	25°C		3.9		1.5	5.1	V/μs	
		0°C		3.7		1.5	5		
		70°C		4		1.5	5		
t <sub>r</sub> Rise time	V <sub>I(PP)</sub> = ±10 mV, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF See Figures 1 and 2	25°C		138		132	ns		
		0°C		134		127			
		70°C		150		142			
t <sub>f</sub> Fall time	V <sub>I(PP)</sub> = ±10 mV, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF See Figure 1	25°C		138		132	ns		
		0°C		134		127			
		70°C		150		142			
Overshoot factor	V <sub>I(PP)</sub> = ±10 mV, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF See Figures 1 and 2	25°C		11%		5%			
		0°C		10%		4%			
		70°C		12%		6%			
V <sub>n</sub> Equivalent input noise voltage	TL031C R <sub>S</sub> = 20 Ω See Figure 3	25°C	f = 10 Hz		61		61	nV/√Hz	
			f = 1 kHz		41		41		
		25°C	f = 10 Hz		61		61		
			f = 1 kHz		41		41		60
I <sub>n</sub> Equivalent input noise current	f = 1 kHz	25°C		0.003		0.003	pA/√Hz		
B <sub>1</sub> Unity-gain bandwidth	V <sub>I</sub> = 10 mV R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 25 pF See Figure 4	25°C		1		1.1	MHz		
		0°C		1		1.1			
		70°C		1		1			
φ <sub>m</sub> Phase margin at unity gain	V <sub>I</sub> = 10 mV R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 25 pF See Figure 4	25°C		61°		65°			
		0°C		61°		65°			
		70°C		60°		64°			

<sup>†</sup> For V<sub>CC±</sub> = ±5 V, V<sub>I(PP)</sub> = ±1 V; for V<sub>CC±</sub> = ±15 V, V<sub>I(PP)</sub> = ±5 V



# TL03x, TL03xA ENHANCED-JFET LOW-POWER LOW-OFFSET OPERATIONAL AMPLIFIERS

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## TL031I and TL031AI electrical characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS		T <sub>A</sub>	TL031I, TL031AI						UNIT
				V <sub>CC±</sub> = ±5 V			V <sub>CC±</sub> = ±15 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>IO</sub> Input offset voltage	V <sub>O</sub> = 0, V <sub>IC</sub> = 0, R <sub>S</sub> = 50 Ω	TL031I	25°C	0.54	3.5		0.5	1.5	mV	
			Full range†		5.3		3.3			
		TL031AI	25°C	0.41	2.8		0.34	0.8		
			Full range†		4.6		2.6			
α <sub>V<sub>IO</sub></sub> Temperature coefficient of input offset voltage	V <sub>O</sub> = 0, V <sub>IC</sub> = 0, R <sub>S</sub> = 50 Ω	TL031I	25°C to 85°C	6.5		6.2		μV/°C		
		TL031AI	25°C to 85°C	6.5		6.2	25			
Input offset voltage long-term drift‡	V <sub>O</sub> = 0, V <sub>IC</sub> = 0, R <sub>S</sub> = 50 Ω		25°C	0.04		0.04		μV/mo		
I <sub>IO</sub> Input offset current	V <sub>O</sub> = 0, V <sub>IC</sub> = 0 See Figure 5		25°C	1	100	1	100	pA		
			85°C	0.02	0.45	0.02	0.45	nA		
I <sub>IB</sub> Input bias current	V <sub>O</sub> = 0, V <sub>IC</sub> = 0 See Figure 5		25°C	2	200	2	200	pA		
			85°C	0.2	0.9	0.2	0.9	nA		
V <sub>ICR</sub> Common-mode input voltage range			25°C	-1.5 to 4	-3.4 to 5.4	-11.5 to 14	-13.4 to 15.4	V		
			Full range†	-1.5 to 4		-11.5 to 14				
V <sub>OM+</sub> Maximum positive peak output voltage swing	R <sub>L</sub> = 10 kΩ		25°C	3	4.3	13	14	V		
			-40°C	3	4.1	13	14			
			85°C	3	4.4	13	14			
V <sub>OM-</sub> Maximum negative peak output voltage swing	R <sub>L</sub> = 10 kΩ		25°C	-3	-4.2	-12.5	-13.9	V		
			-40°C	-3	-4.1	-12.5	-13.8			
			85°C	-3	-4.2	-12.5	-14			
A <sub>VD</sub> Large-signal differential voltage amplification§	R <sub>L</sub> = 10 kΩ		25°C	4	12	5	14.3	V/mV		
			-40°C	3	8.4	4	11.6			
			85°C	4	13.5	5	15.3			
r <sub>i</sub> Input resistance			25°C	10 <sup>12</sup>		10 <sup>12</sup>		Ω		
c <sub>i</sub> Input capacitance			25°C	5		4		pF		
CMRR Common-mode rejection ratio	V <sub>IC</sub> = V <sub>ICRmin</sub> , V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω		25°C	70	87	75	94	dB		
			-40°C	70	87	75	94			
			85°C	70	87	75	94			
k <sub>SVR</sub> Supply-voltage rejection ratio (ΔV <sub>CC±</sub> /ΔV <sub>IO</sub> )	V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω		25°C	75	96	75	96	dB		
			-40°C	75	96	75	96			
			85°C	75	96	75	96			

† Full range is -40°C to 85°C.

‡ Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T<sub>A</sub> = 150°C extrapolated to T<sub>A</sub> = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

§ At V<sub>CC±</sub> = ±5 V, V<sub>O</sub> = ±2.3 V; at V<sub>CC±</sub> = ±15 V, V<sub>O</sub> = ±10 V





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**TL031I and TL031AI electrical characteristics at specified free-air temperature (continued)**

PARAMETER	TEST CONDITIONS	T <sub>A</sub>	TL031I, TL031AI						UNIT
			V <sub>CC±</sub> = ±5 V			V <sub>CC±</sub> = ±15 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
P <sub>D</sub>	Total power dissipation	V <sub>O</sub> = 0, No load	25°C	1.9	2.5	6.5	8.4	mW	
			-40°C	1.4	2.5	5.4	8.4		
			85°C	1.9	2.5	6.2	8.4		
I <sub>CC</sub>	Supply current	V <sub>O</sub> = 0, No load	25°C	192	250	217	280	μA	
			-40°C	144	250	181	280		
			85°C	189	250	207	280		

**TL031I and TL031AI operating characteristics at specified free-air temperature**

PARAMETER	TEST CONDITIONS	T <sub>A</sub>	TL031I, TL031AI						UNIT	
			V <sub>CC±</sub> = ±5 V			V <sub>CC±</sub> = ±15 V				
			MIN	TYP	MAX	MIN	TYP	MAX		
SR <sub>+</sub>	Positive slew rate at unity gain†	R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF See Figure 1	25°C	2			1.5 2.9		V/μs	
			-40°C	1.6			1 2.1			
			85°C	2.3			1.5 3.3			
SR <sub>-</sub>	Negative slew rate at unity gain†	R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF See Figure 1	25°C	3.9			1.5 5.1		V/μs	
			-40°C	3.3			1.5 4.8			
			85°C	4.1			1.5 4.9			
t <sub>r</sub>	Rise time	V <sub>I(PP)</sub> = ±10 mV, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF See Figures 1 and 2	25°C	138			132		ns	
			-40°C	132			123			
			85°C	154			146			
t <sub>f</sub>	Fall time	V <sub>I(PP)</sub> = ±10 mV, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF See Figure 1	25°C	138			132		ns	
			-40°C	132			123			
			85°C	154			146			
Overshoot factor	Overshoot factor	V <sub>I(PP)</sub> = ±10 mV, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF See Figures 1 and 2	25°C	11%			5%			
			-40°C	12%			5%			
			85°C	13%			7%			
V <sub>n</sub>	Equivalent input noise voltage	TL031I	R <sub>S</sub> = 20 Ω See Figure 3	f = 10 Hz	61			61		nV/√Hz
				f = 1 kHz	41			41		
		TL031AI	f = 10 Hz	61			61			
			f = 1 kHz	41			41 60			
I <sub>n</sub>	Equivalent input noise current	f = 1 kHz	25°C	0.003			0.003		pA/√Hz	
B <sub>1</sub>	Unity-gain bandwidth	V <sub>I</sub> = 10 mV R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 25 pF See Figure 4	25°C	1			1.1		MHz	
			-40°C	1			1.1			
			85°C	0.9			1			
φ <sub>m</sub>	Phase margin at unity gain	V <sub>I</sub> = 10 mV, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 25 pF See Figure 4	25°C	61°			65°			
			-40°C	60°			65°			
			85°C	60°			64°			

† For V<sub>CC±</sub> = ±5 V, V<sub>I(PP)</sub> = ±1 V; for V<sub>CC±</sub> = ±15 V, V<sub>I(PP)</sub> = ±5 V



# TL03x, TL03xA ENHANCED-JFET LOW-POWER LOW-OFFSET OPERATIONAL AMPLIFIERS

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## TL031M and TL031AM electrical characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS		T <sub>A</sub>	TL031M, TL031AM						UNIT
				V <sub>CC±</sub> = ±5 V			V <sub>CC±</sub> = ±15 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>IO</sub> Input offset voltage	V <sub>O</sub> = 0, V <sub>IC</sub> = 0, R <sub>S</sub> = 50 Ω	TL031M	25°C	0.54 3.5		0.5 1.5		mV		
			Full range†	6.5		4.5				
		TL031AM	25°C	0.41 2.8		0.34 0.8				
			Full range†	5.8		3.8				
α <sub>V<sub>IO</sub></sub> Temperature coefficient of input offset voltage	V <sub>O</sub> = 0, V <sub>IC</sub> = 0, R <sub>S</sub> = 50 Ω	TL031M	25°C to 125°C	5.1		4.3		μV/°C		
		TL031AM	25°C to 125°C	5.1		4.3				
Input offset voltage long-term drift‡	V <sub>O</sub> = 0, V <sub>IC</sub> = 0, R <sub>S</sub> = 50 Ω		25°C	0.04		0.04		μV/mo		
I <sub>IO</sub> Input offset current	V <sub>O</sub> = 0, V <sub>IC</sub> = 0 See Figure 5		25°C	1 100		1 100		pA		
			125°C	0.2 10		0.2 10		nA		
I <sub>IB</sub> Input bias current	V <sub>O</sub> = 0, V <sub>IC</sub> = 0 See Figure 5		25°C	2 200		2 200		pA		
			125°C	7 20		8 20		nA		
V <sub>ICR</sub> Common-mode input voltage range			25°C	-1.5 to 4	-3.4 to 5.4	-11.5 to 14	-13.4 to 15.4	V		
			Full range†	-1.5 to 4		-11.5 to 14				
V <sub>OM+</sub> Maximum positive peak output voltage swing	R <sub>L</sub> = 10 kΩ		25°C	3 4.3		13 14		V		
			-55°C	3 4.1		13 14				
			125°C	3 4.4		13 14				
V <sub>OM-</sub> Maximum negative peak output voltage swing	R <sub>L</sub> = 10 kΩ		25°C	-3 -4.2		-12.5 -13.9		V		
			-55°C	-3 -4		-12.5 -13.8				
			125°C	-3 -4.3		-12.5 -14				
A <sub>VD</sub> Large-signal differential voltage amplification§	R <sub>L</sub> = 10 kΩ		25°C	4 12		5 14.3		V/mV		
			-55°C	3 7.1		4 10.4				
			125°C	3 12.9		4 15				
r <sub>i</sub> Input resistance			25°C	10 <sup>12</sup>		10 <sup>12</sup>		Ω		
c <sub>i</sub> Input capacitance			25°C	5		4		pF		
CMRR Common-mode rejection ratio	V <sub>IC</sub> = V <sub>ICRmin</sub> , V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω		25°C	70 87		75 94		dB		
			-55°C	70 87		70 94				
			125°C	70 87		70 94				
k <sub>SVR</sub> Supply-voltage rejection ratio (ΔV <sub>CC±</sub> /ΔV <sub>IO</sub> )	V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω		25°C	75 96		75 96		dB		
			-55°C	75 96		75 95				
			125°C	75 96		75 96				
P <sub>D</sub> Total power dissipation	V <sub>O</sub> = 0, No load		25°C	1.9 2.5		6.5 8.4		mW		
			-55°C	1.1 2.5		4.7 8.4				
			125°C	1.8 2.5		5.8 8.4				

† Full range is -55°C to 125°C.

‡ Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T<sub>A</sub> = 150°C extrapolated to T<sub>A</sub> = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

§ At V<sub>CC±</sub> = ±5 V, V<sub>O</sub> = ±2.3 V; at V<sub>CC±</sub> = ±15 V, V<sub>O</sub> = ±10 V



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**TL031M and TL031AM electrical characteristics at specified free-air temperature (continued)**

PARAMETER	TEST CONDITIONS	T <sub>A</sub>	TL031M, TL031AM						UNIT	
			V <sub>CC±</sub> = ±5 V			V <sub>CC±</sub> = ±15 V				
			MIN	TYP	MAX	MIN	TYP	MAX		
I <sub>CC</sub>	Supply current	V <sub>O</sub> = 0, No load	25°C		192	250		217	280	μA
			-55°C		114	250		156	280	
			125°C		178	250		197	280	

**TL031M and TL031AM operating characteristics at specified free-air temperature**

PARAMETER	TEST CONDITIONS	T <sub>A</sub>	TL031M, TL031AM						UNIT
			V <sub>CC±</sub> = ±5 V			V <sub>CC±</sub> = ±15 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
SR <sub>+</sub>	Positive slew rate at unity gain†	R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF See Figure 1	25°C		2		1.5	2.9	V/μs
			-55°C		1.4		1	1.9	
			125°C		2.4		1	3.5	
SR <sub>-</sub>	Negative slew rate at unity gain†	R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF See Figure 1	25°C		3.9		1.5	5.1	V/μs
			-55°C		3.2		1	4.6	
			125°C		4.1		1	4.7	
t <sub>r</sub>	Rise time	V <sub>I(PP)</sub> = ±10 mV, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF See Figures 1 and 2	25°C		138		132	ns	
			-55°C		142		123		
			125°C		166		158		
t <sub>f</sub>	Fall time	V <sub>I(PP)</sub> = ±10 mV, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF See Figure 1	25°C		138		132	ns	
			-55°C		142		123		
			125°C		166		158		
Overshoot factor		V <sub>I(PP)</sub> = ±10 mV, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF See Figures 1 and 2	25°C		11%		5%		
			-55°C		16%		6%		
			125°C		14%		8%		
V <sub>n</sub>	Equivalent input noise voltage	TL031M R <sub>S</sub> = 20 Ω See Figure 3	25°C	f = 10 Hz		61		61	nV/√Hz
				f = 1 kHz		41		41	
			25°C	f = 10 Hz		61		61	
				f = 1 kHz		41		41	
I <sub>n</sub>	Equivalent input noise current	f = 1 kHz	25°C		0.003		0.003	pA/√Hz	
B <sub>1</sub>	Unity-gain bandwidth	V <sub>I</sub> = 10 mV, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 25 pF See Figure 4	25°C		1		1.1	MHz	
			-55°C		1		1.1		
			125°C		0.9		0.9		
φ <sub>m</sub>	Phase margin at unity gain	V <sub>I</sub> = 10 mV, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 25 pF See Figure 4	25°C		61°		65°		
			-55°C		57°		64°		
			125°C		59°		62°		

† For V<sub>CC±</sub> = ±5 V, V<sub>I(PP)</sub> = ±1 V; for V<sub>CC±</sub> = ±15 V, V<sub>I(PP)</sub> = ±5 V



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## TL032C and TL032AC electrical characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS		T <sub>A</sub>	TL032C, TL032AC						UNIT
				V <sub>CC±</sub> = ±5 V			V <sub>CC±</sub> = ±15 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>IO</sub> Input offset voltage	V <sub>O</sub> = 0, V <sub>IC</sub> = 0, R <sub>S</sub> = 50 Ω	TL032C	25°C	0.69 3.5		0.57 1.5		mV		
			Full range†	4.5		2.5				
		TL032AC	25°C	0.53 2.8		0.39 0.8				
			Full range†	3.8		1.8				
α <sub>V<sub>IO</sub></sub> Temperature coefficient of input offset voltage	V <sub>O</sub> = 0, V <sub>IC</sub> = 0, R <sub>S</sub> = 50 Ω	TL032C	25°C to 70°C	11.5		10.8		μV/°C		
		TL032AC	25°C to 70°C	11.5		10.8 25				
Input offset voltage long-term drift‡	V <sub>O</sub> = 0, V <sub>IC</sub> = 0, R <sub>S</sub> = 50 Ω		25°C	0.04		0.04		μV/mo		
I <sub>IO</sub> Input offset current	V <sub>O</sub> = 0, See Figure 5	V <sub>IC</sub> = 0	25°C	1 100		1 100		pA		
			70°C	9 200		12 200				
I <sub>IB</sub> Input bias current	V <sub>O</sub> = 0, See Figure 5	V <sub>IC</sub> = 0	25°C	2 200		2 200		pA		
			70°C	50 400		80 400				
V <sub>ICR</sub> Common-mode input voltage range			25°C	-1.5 to 4	-3.4 to 5.4	-11.5 to 14	-13.4 to 15.4	V		
			Full range†	-1.5 to 4		-11.5 to 14				
V <sub>OM+</sub> Maximum positive peak output voltage swing	R <sub>L</sub> = 10 kΩ		25°C	3 4.3		13 14		V		
			0°C	3 4.2		13 14				
			70°C	3 4.3		13 14				
V <sub>OM-</sub> Maximum negative peak output voltage swing	R <sub>L</sub> = 10 kΩ		25°C	-3 -4.2		-12.5 -13.9		V		
			0°C	-3 -4.1		-12.5 -13.9				
			70°C	-3 -4.2		-12.5 -14				
A <sub>VD</sub> Large-signal differential voltage amplification§	R <sub>L</sub> = 10 kΩ		25°C	4 12		5 14.3		V/mV		
			0°C	3 11.1		4 13.5				
			70°C	4 13.3		5 15.2				
r <sub>i</sub> Input resistance			25°C	10 <sup>12</sup>		10 <sup>12</sup>		Ω		
c <sub>i</sub> Input capacitance			25°C	5		14		pF		
CMRR Common-mode rejection ratio	V <sub>IC</sub> = V <sub>ICRmin</sub> , V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω		25°C	70 87		75 94		dB		
			0°C	70 87		75 94				
			70°C	70 87		75 94				
k <sub>SVR</sub> Supply-voltage rejection ratio (ΔV <sub>CC±</sub> /ΔV <sub>IO</sub> )	V <sub>CC±</sub> = ±5 V to ±15 V, V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω		25°C	75 96		75 96		dB		
			0°C	75 96		75 96				
			70°C	75 96		75 96				

† Full range is 0°C to 70°C.

‡ Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T<sub>A</sub> = 150°C extrapolated to T<sub>A</sub> = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

§ At V<sub>CC±</sub> = ±5 V, V<sub>O</sub> = 2.3 V; at V<sub>CC±</sub> = ±15 V, V<sub>O</sub> = ±10 V



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**TL032C and TL032AC electrical characteristics at specified free-air temperature (continued)**

PARAMETER	TEST CONDITIONS	T <sub>A</sub>	TL032C, TL032AC						UNIT
			V <sub>CC±</sub> = ±5 V			V <sub>CC±</sub> = ±15 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
P <sub>D</sub>	Total power dissipation (two amplifiers)	V <sub>O</sub> = 0, No load	25°C	3.8	5	13	17	mW	
			0°C	3.7	5	12.7	17		
			70°C	3.8	5	12.6	17		
I <sub>CC</sub>	Supply current (two amplifiers)	V <sub>O</sub> = 0, No load	0°C	368	500	422	560	μA	
			70°C	378	500	420	560		
V <sub>O1</sub> /V <sub>O2</sub>	Crosstalk attenuation	A <sub>VD</sub> = 100 dB	25°C	120		120		dB	

**TL032C and TL032AC operating characteristics at specified free-air temperature**

PARAMETER	TEST CONDITIONS	T <sub>A</sub>	TL032C, TL032AC						UNIT
			V <sub>CC±</sub> = ±5 V			V <sub>CC±</sub> = ±15 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
SR <sub>+</sub>	Positive slew rate at unity gain†	R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF See Figure 1	25°C	1.2		1.5	2.9	V/μs	
			0°C	1.8		1	2.6		
			70°C	2.2		1.5	3.2		
SR <sub>-</sub>	Negative slew rate at unity gain†	R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF See Figure 1	25°C	3.9		1.5	5.1	V/μs	
			0°C	3.7		1.5	5		
			70°C	4		1.5	5		
t <sub>r</sub>	Rise time	V <sub>I(PP)</sub> = ±10 V, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF See Figures 1 and 2	25°C	138		132	ns		
			0°C	134		127			
			70°C	150		142			
t <sub>f</sub>	Fall time	V <sub>I(PP)</sub> = ±10 V, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF See Figures 1 and 2	25°C	138		132	ns		
			0°C	134		127			
			70°C	150		142			
Overshoot factor		V <sub>I(PP)</sub> = ±10 V, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF See Figures 1 and 2	25°C	11%		5%			
			0°C	10%		4%			
			70°C	12%		6%			
V <sub>n</sub>	Equivalent input noise voltage	TL032C	R <sub>S</sub> = 20 Ω See Figure 3	f = 10 Hz		49	nV/√Hz		
				f = 1 kHz		41			
		TL032AC	f = 10 Hz		49				
			f = 1 kHz		41	60			
I <sub>n</sub>	Equivalent input noise current	f = 1 kHz	25°C	0.003		0.003	pA/√Hz		
B <sub>1</sub>	Unity-gain bandwidth	V <sub>I</sub> = 10 mV, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 25 pF See Figure 4	25°C	1		1.1	MHz		
			0°C	1		1.1			
			70°C	1		1			
φ <sub>m</sub>	Phase margin at unity gain	V <sub>I</sub> = 10 mV, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 25 pF See Figure 4	25°C	61°		65°			
			0°C	61°		65°			
			70°C	60°		64°			

† For V<sub>CC±</sub> = ±5 V, V<sub>I(PP)</sub> = ±1 V; for V<sub>CC±</sub> = ±15 V, V<sub>I(PP)</sub> = ±5 V



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## TL032I and TL032AI electrical characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS		T <sub>A</sub>	TL032I, TL032AI						UNIT
				V <sub>CC±</sub> = ±5 V			V <sub>CC±</sub> = ±15 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>IO</sub> Input offset voltage	V <sub>O</sub> = 0, V <sub>IC</sub> = 0, R <sub>S</sub> = 50 Ω	TL032I	25°C	0.69	3.5		0.57	1.5	mV	
			Full range†			5.3		3.3		
		TL032AI	25°C	0.53	2.8		0.39	0.8		
			Full range†			4.6		2.6		
α <sub>V<sub>IO</sub></sub> Temperature coefficient of input offset voltage	V <sub>O</sub> = 0, V <sub>IC</sub> = 0, R <sub>S</sub> = 50 Ω	TL032I	25°C to 85°C	11.4		10.8		μV/°C		
		TL032AI	25°C to 85°C	11.4		10.8	25			
Input offset voltage long-term drift‡	V <sub>O</sub> = 0, V <sub>IC</sub> = 0, R <sub>S</sub> = 50 Ω		25°C	0.04		0.04		μV/mo		
I <sub>IO</sub> Input offset current	V <sub>O</sub> = 0, See Figure 5	V <sub>IC</sub> = 0	25°C	1	100		1	100	pA	
			85°C	0.02	0.45		0.02	0.45	nA	
I <sub>IB</sub> Input bias current	V <sub>O</sub> = 0, See Figure 5	V <sub>IC</sub> = 0	25°C	2	200		2	200	pA	
			85°C	0.2	0.9		0.3	0.9	nA	
V <sub>ICR</sub> Common-mode input voltage range			25°C	-1.5 to 4	-3.4 to 5.4		-11.5 to 14	-13.4 to 15.4	V	
			Full range†	-1.5 to 4			-11.5 to 14			
V <sub>OM+</sub> Maximum positive peak output voltage swing	R <sub>L</sub> = 10 kΩ		25°C	3	4.3		13	14	V	
			-40°C	3	4.2		13	14		
			85°C	3	4.4		13	14		
V <sub>OM-</sub> Maximum negative peak output voltage swing	R <sub>L</sub> = 10 kΩ		25°C	-3	-4.2		-12.5	-13.9	V	
			-40°C	-3	-4.1		-12.5	-13.8		
			85°C	-3	-4.2		-12.5	-14		
A <sub>VD</sub> Large-signal differential voltage amplification§	R <sub>L</sub> = 10 kΩ		-40°C	3	8.4		4	11.6	V/mV	
			85°C	4	13.5		5	15.3		
r <sub>i</sub> Input resistance			25°C	10 <sup>12</sup>		10 <sup>12</sup>		Ω		
c <sub>i</sub> Input capacitance			25°C	5		4		pF		
CMRR Common-mode rejection ratio	V <sub>IC</sub> = V <sub>ICRmin</sub> , V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω		25°C	70	87		75	94	dB	
			-40°C	70	87		75	94		
			85°C	70	87		75	94		
k <sub>SVR</sub> Supply-voltage rejection ratio (ΔV <sub>CC±</sub> /ΔV <sub>IO</sub> )	V <sub>CC±</sub> = ±5 V to ±15 V, V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω		25°C	75	96		75	96	dB	
			-40°C	75	96		75	96		
			85°C	75	96		75	96		

† Full range is -40°C to 85°C.

‡ Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T<sub>A</sub> = 150°C extrapolated to T<sub>A</sub> = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

§ At V<sub>CC±</sub> = ±5 V, V<sub>O</sub> = 2.3 V; at V<sub>CC±</sub> = ±15 V, V<sub>O</sub> = ±10 V



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**TL032I and TL032AI electrical characteristics at specified free-air temperature (continued)**

PARAMETER	TEST CONDITIONS	T <sub>A</sub>	TL032I, TL032AI						UNIT
			V <sub>CC±</sub> = ±5 V			V <sub>CC±</sub> = ±15 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
P <sub>D</sub> Total power dissipation (two amplifiers)	V <sub>O</sub> = 0, No load	25°C		3.8	5		13	17	mW
		-40°C		2.9	5		10.9	17	
		85°C		3.7	5		12.4	17	
I <sub>CC</sub> Supply current (two amplifiers)	V <sub>O</sub> = 0, No load	25°C		384	500		434	560	μA
		-40°C		288	500		362	560	
		85°C		372	500		414	560	
V <sub>O1</sub> /V <sub>O2</sub> Crosstalk attenuation	A <sub>VD</sub> = 100 dB	25°C		120		120		dB	

**TL032I and TL032AI operating characteristics at specified free-air temperature**

PARAMETER	TEST CONDITIONS	T <sub>A</sub>	TL032I, TL032AI						UNIT
			V <sub>CC±</sub> = ±5 V			V <sub>CC±</sub> = ±15 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
SR <sub>+</sub> Positive slew rate at unity gain†	R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF	25°C		2		1.5	2.9	V/μs	
		-40°C		1.6		1	2.1		
		85°C		2.3		1.5	3.3		
SR <sub>-</sub> Negative slew rate at unity gain†	R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF	25°C		3.9		1.5	5.1	V/μs	
		-40°C		3.3		1.5	4.8		
		85°C		4.1		1.5	4.9		
t <sub>r</sub> Rise time	V <sub>I(PP)</sub> = ±10 V, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF See Figures 1 and 2	25°C		138		132		ns	
		-40°C		132		123			
		85°C		154		146			
t <sub>f</sub> Fall time	V <sub>I(PP)</sub> = ±10 V, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF See Figure 1	25°C		138		132		ns	
		-40°C		132		123			
		85°C		154		146			
Overshoot factor	V <sub>I(PP)</sub> = ±10 V, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF See Figures 1 and 2	25°C		11%		5%			
		-40°C		12%		5%			
		85°C		13%		7%			
V <sub>n</sub> Equivalent input noise voltage	TL032I R <sub>S</sub> = 20 Ω See Figure 3	25°C	f = 10 Hz		49		49	nV/√Hz	
			f = 1 kHz		41		41		
		25°C	f = 10 Hz		49		49		
			f = 1 kHz		41		41 60		
I <sub>n</sub> Equivalent input noise current	f = 1 kHz	25°C		0.003		0.003	pA/√Hz		
B <sub>1</sub> Unity-gain bandwidth	V <sub>I</sub> = 10 mV, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 25 pF See Figure 4	25°C		1		1.1	MHz		
		-40°C		1		1.1			
		85°C		0.9		1			
φ <sub>m</sub> Phase margin at unity gain	V <sub>I</sub> = 10 mV, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 25 pF See Figure 4	25°C		61°		65°			
		-40°C		61°		65°			
		85°C		60°		64°			

† For V<sub>CC±</sub> = ±5 V, V<sub>I(PP)</sub> = ±1 V; for V<sub>CC±</sub> = ±15 V, V<sub>I(PP)</sub> = ±5 V



# TL03x, TL03xA ENHANCED-JFET LOW-POWER LOW-OFFSET OPERATIONAL AMPLIFIERS

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## TL032M and TL032AM electrical characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS		T <sub>A</sub>	TL032M, TL032AM						UNIT
				V <sub>CC±</sub> = ±5 V			V <sub>CC±</sub> = ±15 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>IO</sub> Input offset voltage	V <sub>O</sub> = 0, V <sub>IC</sub> = 0, R <sub>S</sub> = 50 Ω	TL032M	25°C	0.69	3.5		0.57	1.5	mV	
			Full range†			6.5		4.5		
		TL032AM	25°C	0.53	2.8		0.39	0.8		
			Full range†			5.8		3.8		
α <sub>V<sub>IO</sub></sub> Temperature coefficient of input offset voltage	V <sub>O</sub> = 0, V <sub>IC</sub> = 0, R <sub>S</sub> = 50 Ω	TL032M	25°C to 125°C	9.7			9.7		μV/°C	
		TL032AM	25°C to 125°C	9.7			9.7			
Input offset voltage long-term drift‡	V <sub>O</sub> = 0, V <sub>IC</sub> = 0, R <sub>S</sub> = 50 Ω		25°C	0.04			0.04		μV/mo	
I <sub>IO</sub> Input offset current	V <sub>O</sub> = 0, V <sub>IC</sub> = 0 See Figure 5		25°C	1	100		1	100	pA	
			125°C	0.2	10		0.2	10	nA	
I <sub>IB</sub> Input bias current	V <sub>O</sub> = 0, V <sub>IC</sub> = 0 See Figure 5		25°C	2	200		2	200	pA	
			125°C	7	20		8	20	nA	
V <sub>ICR</sub> Common-mode input voltage range			25°C	-1.5 to 4	-3.4 to 5.4		-11.5 to 14	-13.4 to 15.4	V	
		Full range†		-1.5 to 4			-11.5 to 14			
V <sub>OM+</sub> Maximum positive peak output voltage swing	R <sub>L</sub> = 10 kΩ		25°C	3	4.3		13	14	V	
			-55°C	3	4.1		13	14		
			125°C	3	4.4		13	14		
V <sub>OM-</sub> Maximum negative peak output voltage swing	R <sub>L</sub> = 10 kΩ		25°C	-3	-4.2		-12.5	-13.9	V	
			-55°C	-3	-4		-12.5	-13.8		
			125°C	-3	-4.3		-12.5	-14		
A <sub>VD</sub> Large-signal differential voltage amplification§	R <sub>L</sub> = 10 kΩ		25°C	4	12		5	14.3	V/mV	
			-55°C	3	7.1		4	10.4		
			125°C	3	12.9		4	15		
r <sub>i</sub> Input resistance			25°C	10 <sup>12</sup>			10 <sup>12</sup>		Ω	
c <sub>i</sub> Input capacitance			25°C	5			4		pF	
CMRR Common-mode rejection ratio	V <sub>IC</sub> = V <sub>ICRmin</sub> , V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω		25°C	70	87		75	94	dB	
			-55°C	70	87		70	94		
			125°C	70	87		70	94		
k <sub>SVR</sub> Supply-voltage rejection ratio (ΔV <sub>CC±</sub> /ΔV <sub>IO</sub> )	V <sub>CC±</sub> = ±5 V to ±15 V, V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω		25°C	75	96		75	96	dB	
			-55°C	75	95		75	95		
			125°C	75	96		75	96		

† Full range is -55°C to 125°C.

‡ Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T<sub>A</sub> = 150°C extrapolated to T<sub>A</sub> = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

§ At V<sub>CC±</sub> = ±5 V, V<sub>O</sub> = 2.3 V; at V<sub>CC±</sub> = ±15 V, V<sub>O</sub> = ±10 V





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**TL032M and TL032AM electrical characteristics at specified free-air temperature (continued)**

PARAMETER	TEST CONDITIONS	T <sub>A</sub>	TL032M, TL032AM						UNIT
			V <sub>CC±</sub> = ±5 V			V <sub>CC±</sub> = ±15 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
P <sub>D</sub> Total power dissipation (two amplifiers) V <sub>O</sub> = 0,	V <sub>O</sub> = 0, No load	25°C		3.8	5		13	17	mW
		-55°C		2.3	5		9.4	17	
		125°C		3.6	5		11.8	17	
I <sub>CC</sub> Supply current (two amplifiers)	V <sub>O</sub> = 0, No load	25°C		384	500		434	560	μA
		-55°C		228	500		312	560	
		125°C		356	500		394	560	
V <sub>O1</sub> /V <sub>O2</sub> Crosstalk attenuation	A <sub>VD</sub> = 100 dB	25°C		120			120		dB

**TL032M and TL032AM operating characteristics at specified free-air temperature**

PARAMETER	TEST CONDITIONS	T <sub>A</sub>	TL032M, TL032AM						UNIT
			V <sub>CC±</sub> = ±5 V			V <sub>CC±</sub> = ±15 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
SR <sub>+</sub> Positive slew rate at unity gain†	R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF See and Figure 1	25°C		2		1.5	2.9	V/μs	
		-55°C		1.4		1	1.9		
		125°C		2.4		1	3.5		
SR <sub>-</sub> Negative slew rate at unity gain†	R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF See and Figure 1	25°C		3.9		1.5	5.1	V/μs	
		-55°C		3.2		1	4.6		
		125°C		4.1		1	4.7		
t <sub>r</sub> Rise time	V <sub>I(PP)</sub> = ±10 V, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF See Figures 1 and 2	25°C		138		132	ns		
		-55°C		142		123			
		125°C		166		58			
t <sub>f</sub> Fall time	V <sub>I(PP)</sub> = ±10 V, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF See Figure 1	25°C		138		132	ns		
		-55°C		142		123			
		125°C		166		158			
Overshoot factor	V <sub>I(PP)</sub> = ±10 V, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF See Figures 1 and 2	25°C		11%		5%			
		-55°C		16%		6%			
		125°C		14%		8%			
V <sub>n</sub> Equivalent input noise voltage	TL032M R <sub>S</sub> = 20 Ω See Figure 3	25°C	f = 10 Hz		49		49	nV/√Hz	
			f = 1 kHz		41		41		
		25°C	f = 10 Hz		49		49		
			f = 1 kHz		41		41		
I <sub>n</sub> Equivalent input noise current	f = 1 kHz	25°C		0.003		0.003	pA/√Hz		
B1 Unity-gain bandwidth	V <sub>I</sub> = 10 mV, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 25 pF See Figure 4	25°C		1		1.1	MHz		
		-55°C		1		1.1			
		125°C		0.9		0.9			
φ <sub>m</sub> Phase margin at unity gain	V <sub>I</sub> = 10 mV, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 25 pF See Figure 4	25°C		61°		65°			
		-55°C		57°		64°			
		125°C		59°		62°			

† For V<sub>CC±</sub> = ±5 V, V<sub>I(PP)</sub> = ±1 V; for V<sub>CC±</sub> = ±15 V, V<sub>I(PP)</sub> = ±5 V



# TL03x, TL03xA ENHANCED-JFET LOW-POWER LOW-OFFSET OPERATIONAL AMPLIFIERS

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## TL034C and TL034AC electrical characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS		T <sub>A</sub>	TL034C, TL034AC						UNIT
				V <sub>CC±</sub> = ±5 V			V <sub>CC±</sub> = ±15 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>IO</sub> Input offset voltage	V <sub>O</sub> = 0, V <sub>IC</sub> = 0, R <sub>S</sub> = 50 Ω	TL034C	25°C	0.91	6		0.79	4	mV	
			Full range†			8.2		6.2		
		TL034AC	25°C	0.7	3.5		0.58	1.5		
			Full range†			5.7		3.7		
α <sub>V<sub>IO</sub></sub> Temperature coefficient of input offset voltage	V <sub>O</sub> = 0, V <sub>IC</sub> = 0, R <sub>S</sub> = 50 Ω	TL034C	25°C to 70°C	11.6		12		μV/°C		
		TL034AC	25°C to 70°C	11.6		12	25			
Input offset voltage long-term drift‡	V <sub>O</sub> = 0, V <sub>IC</sub> = 0, R <sub>S</sub> = 50 Ω		25°C	0.04		0.04		μV/mo		
I <sub>IO</sub> Input offset current	V <sub>O</sub> = 0, V <sub>IC</sub> = 0 See Figure 5		25°C	1	100		1	100	pA	
			70°C	9	200		12	200		
I <sub>IB</sub> Input bias current	V <sub>O</sub> = 0, V <sub>IC</sub> = 0 See Figure 5		25°C	2	200		2	200	pA	
			70°C	50	400		80	400		
V <sub>ICR</sub> Common-mode input voltage range			25°C	-1.5 to 4	-3.4 to 5.4		-11.5 to 14	-13.4 to 15.4	V	
			Full range†	-1.5 to 4			-11.5 to 14			
V <sub>OM+</sub> Maximum positive peak output voltage swing	R <sub>L</sub> = 10 kΩ		25°C	3	4.3		13	14	V	
			0°C	3	4.2		13	14		
			70°C	3	4.3		13	14		
V <sub>OM-</sub> Maximum negative peak output voltage swing	R <sub>L</sub> = 10 kΩ		25°C	-3	-4.2		-12.5	-13.9	V	
			0°C	-3	-4.1		-12.5	-13.9		
			70°C	-3	-4.2		-12.5	-14		
A <sub>VD</sub> Large-signal differential voltage amplification§	R <sub>L</sub> = 10 kΩ		25°C	4	12		5	14.3	V/mV	
			0°C	3	11.1		4	13.5		
			70°C	4	13.3		5	15.2		
r <sub>i</sub> Input resistance			25°C	10 <sup>12</sup>		10 <sup>12</sup>		Ω		
c <sub>i</sub> Input capacitance			25°C	5		14		pF		
CMRR Common-mode rejection ratio	V <sub>IC</sub> = V <sub>ICRmin</sub> , V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω		25°C	70	87		75	94	dB	
			0°C	70	87		75	94		
			70°C	70	87		75	94		
k <sub>SVR</sub> Supply-voltage rejection ratio (ΔV <sub>CC±</sub> /ΔV <sub>IO</sub> )	V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω		25°C	75	96		75	96	dB	
			0°C	75	96		75	96		
			70°C	75	96		75	96		

† Full range is 0°C to 70°C.

‡ Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T<sub>A</sub> = 150°C extrapolated to T<sub>A</sub> = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

§ At V<sub>CC±</sub> = ±5 V, V<sub>O</sub> = ±2.3 V; at V<sub>CC±</sub> = ±15 V, V<sub>O</sub> = ±10 V



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## TL034C and TL034AC electrical characteristics at specified free-air temperature (continued)

PARAMETER	TEST CONDITIONS	T <sub>A</sub>	TL034C, TL034AC						UNIT
			V <sub>CC±</sub> = ±5 V			V <sub>CC±</sub> = ±15 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
P <sub>D</sub>	Total power dissipation (two amplifiers)	V <sub>O</sub> = 0, No load	25°C	7.7	10		26	34	mW
			0°C	7.4	10		25.3	34	
			70°C	7.6	10		25.2	34	
I <sub>CC</sub>	Supply current (four amplifiers)	V <sub>O</sub> = 0, No load	25°C	0.77	1		0.87	1.12	mA
			0°C	0.74	1		0.85	1.12	
			70°C	0.76	1		0.84	1.12	
V <sub>O1</sub> /V <sub>O2</sub>	Crosstalk attenuation	A <sub>VD</sub> = 100	25°C	120			120		dB

## TL034C and TL034AC operating characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS	T <sub>A</sub>	TL034C, TL034AC						UNIT	
			V <sub>CC±</sub> = ±5 V			V <sub>CC±</sub> = ±15 V				
			MIN	TYP	MAX	MIN	TYP	MAX		
SR <sub>+</sub>	Positive slew rate at unity gain†	R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF See Figure 1	25°C	2			1.5 2.9		V/μs	
			0°C	1.8			1 2.6			
			70°C	2.2			1.5 3.2			
SR <sub>-</sub>	Negative slew rate at unity gain†	R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF See Figure 1	25°C	3.9			1.5 5.1		V/μs	
			0°C	3.7			1.5 5			
			70°C	4			1.5 5			
t <sub>r</sub>	Rise time	V <sub>I(PP)</sub> = ±10 V, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF See Figures 1 and 2	25°C	138			132		ns	
			0°C	134			127			
			70°C	150			142			
t <sub>f</sub>	Fall time	V <sub>I(PP)</sub> = ±10 V, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF See Figure 1	25°C	138			132		ns	
			0°C	134			127			
			70°C	150			142			
Overshoot factor		V <sub>I(PP)</sub> = ±10 V, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF See Figures 1 and 2	25°C	11%			5%			
			0°C	10%			4%			
			70°C	12%			6%			
V <sub>n</sub>	Equivalent input noise voltage	TL034C	R <sub>S</sub> = 20 Ω See Figure 3	f = 10 Hz	83			83		nV/√Hz
				f = 1 kHz	43			43		
		TL034AC	f = 10 Hz	83			83			
			f = 1 kHz	43			43 60			
I <sub>n</sub>	Equivalent input noise current	f = 1 kHz	25°C	0.003			0.003		pA/√Hz	
B <sub>1</sub>	Unity-gain bandwidth	V <sub>I</sub> = 10 mV R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 25 pF See Figure 4	25°C	1			1.1		MHz	
			0°C	1			1.1			
			70°C	1			1			
φ <sub>m</sub>	Phase margin at unity gain	V <sub>I</sub> = 10 mV, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 25 pF See Figure 4	25°C	61°			65°			
			0°C	61°			65°			
			70°C	60°			64°			

† For V<sub>CC±</sub> = ±5 V, V<sub>I(PP)</sub> = ±1 V; for V<sub>CC±</sub> = ±15 V, V<sub>I(PP)</sub> = ±5 V

# TL03x, TL03xA ENHANCED-JFET LOW-POWER LOW-OFFSET OPERATIONAL AMPLIFIERS

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## TL034I and TL034AI electrical characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS		T <sub>A</sub>	TL034I, TL034AI						UNIT
				V <sub>CC±</sub> = ±5 V			V <sub>CC±</sub> = ±15 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>IO</sub> Input offset voltage	V <sub>O</sub> = 0, V <sub>IC</sub> = 0, R <sub>S</sub> = 50 Ω	TL034I	25°C	0.91	3.6		0.79	4	mV	
			Full range†			9.3		7.3		
		TL034AI	25°C		0.7	3.5		0.58		1.5
			Full range†			6.8		4.8		
α <sub>V<sub>IO</sub></sub> Temperature coefficient of input offset voltage	V <sub>O</sub> = 0, V <sub>IC</sub> = 0, R <sub>S</sub> = 50 Ω	TL034I	25°C to 85°C		11.5		11.6		μV/°C	
		TL034AI	25°C to 85°C		11.5		11.6	25		
Input offset voltage long-term drift‡	V <sub>O</sub> = 0, V <sub>IC</sub> = 0, R <sub>S</sub> = 50 Ω		25°C		0.04		0.04		μV/mo	
I <sub>IO</sub> Input offset current	V <sub>O</sub> = 0, V <sub>IC</sub> = 0 See Figure 5		25°C		1	100	1	100	pA	
			85°C		0.02	0.45	0.02	0.45	nA	
I <sub>IB</sub> Input bias current	V <sub>O</sub> = 0, V <sub>IC</sub> = 0 See Figure 5		25°C		2	200	2	200	pA	
			85°C		0.2	0.9	0.3	0.9	nA	
V <sub>ICR</sub> Common-mode input voltage range			25°C	-1.5 to 4	-3.4 to 5.4		-11.5 to 14	-13.4 to 15.4	V	
			Full range†	-1.5 to 4			-11.5 to 14			
V <sub>OM+</sub> Maximum positive peak output voltage swing	R <sub>L</sub> = 10 kΩ		25°C	3	4.3		13	14	V	
			-40°C	3	4.1		13	14		
			85°C	3	4.4		13	14		
V <sub>OM-</sub> Maximum negative peak output voltage swing	R <sub>L</sub> = 10 kΩ		25°C	-3	-4.2		-12.5	-13.9	V	
			-40°C	-3	-4.1		-12.5	-13.8		
			85°C	-3	-4.2		-12.5	-14		
A <sub>VD</sub> Large-signal differential voltage amplification§	R <sub>L</sub> = 10 kΩ		-40°C	4	12		5	14.3	V/mV	
			85°C	3	8.4		4	11.6		
r <sub>i</sub> Input resistance			25°C		10 <sup>12</sup>		10 <sup>12</sup>	Ω		
c <sub>i</sub> Input capacitance			25°C		5		4	pF		
CMRR Common-mode rejection ratio	V <sub>IC</sub> = V <sub>ICRmin</sub> , V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω		25°C	70	87		75	94	dB	
			-40°C	70	87		75	94		
			85°C	70	87		75	94		
k <sub>SVR</sub> Supply-voltage rejection ratio (ΔV <sub>CC±</sub> /ΔV <sub>IO</sub> )	V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω		25°C	75	96		75	96	dB	
			-40°C	75	96		75	96		
			85°C	75	96		75	96		

† Full range is -40°C to 85°C.

‡ Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T<sub>A</sub> = 150°C extrapolated to T<sub>A</sub> = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

§ At V<sub>CC±</sub> = ±5 V, V<sub>O</sub> = ±2.3 V; at V<sub>CC±</sub> = ±15 V, V<sub>O</sub> = ±10 V



**TL03x, TL03xA**  
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**TL034I and TL034AI electrical characteristics at specified free-air temperature (continued)**

PARAMETER	TEST CONDITIONS	T <sub>A</sub>	TL034I, TL034AI						UNIT
			V <sub>CC±</sub> = ±5 V			V <sub>CC±</sub> = ±15 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
P <sub>D</sub>	Total power dissipation (four amplifiers)	V <sub>O</sub> = 0, No load	25°C	7.7	10		26	34	mW
			-40°C	5.8	10		21.7	34	
			85°C	7.4	10		24.8	34	
I <sub>CC</sub>	Supply current (four amplifiers)	V <sub>O</sub> = 0, No load	25°C	0.77	1		0.87	1.12	mA
			-40°C	0.58	1		0.72	1.12	
			85°C	0.74	1		0.83	1.12	
V <sub>O1</sub> /V <sub>O2</sub>	Crosstalk attenuation	A <sub>VD</sub> = 100	25°C	120			120	dB	

**TL034I and TL034AI operating characteristics**

PARAMETER	TEST CONDITIONS	T <sub>A</sub>	TL034I, TL034AI						UNIT	
			V <sub>CC±</sub> = ±5 V			V <sub>CC±</sub> = ±15 V				
			MIN	TYP	MAX	MIN	TYP	MAX		
SR <sub>+</sub>	Positive slew rate at unity gain†	R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF See Figure 1	25°C	2			1.5 2.9			V/μs
			-40°C	1.6			1 2.1			
			85°C	2.3			1.5 3.3			
SR <sub>-</sub>	Negative slew rate at unity gain†	R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF See Figure 1	25°C	3.9			1.5 5.1			V/μs
			-40°C	3.3			1.5 4.8			
			85°C	4.1			1.5 4.9			
t <sub>r</sub>	Rise time	V <sub>I(PP)</sub> = ±10 V, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF See Figures 1 and 2	25°C	138			132			ns
			-40°C	132			123			
			85°C	154			146			
t <sub>f</sub>	Fall time	V <sub>I(PP)</sub> = ±10 V, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF See Figures 1 and 2	25°C	138			132			ns
			-40°C	132			123			
			85°C	154			146			
Overshoot factor		V <sub>I(PP)</sub> = ±10 V, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF See Figures 1 and 2	25°C	11%			5%			
			-40°C	12%			5%			
			85°C	13%			7%			
V <sub>n</sub>	Equivalent input noise voltage	TL034I R <sub>S</sub> = 20 Ω See Figure 3	25°C	f = 10 Hz			83			nV/√Hz
				f = 1 kHz			43			
			25°C	f = 10 Hz			83			
				f = 1 kHz			43 60			
I <sub>n</sub>	Equivalent input noise current	f = 1 kHz	25°C	0.003			0.003			pA/√Hz
B <sub>1</sub>	Unity-gain bandwidth	V <sub>I</sub> = 10 mV, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 25 pF See Figure 4	25°C	1			1.1			MHz
			-40°C	1			1.1			
			85°C	0.9			1			
φ <sub>m</sub>	Phase margin at unity gain	V <sub>I</sub> = 10 mV, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 25 pF See Figure 4	25°C	61°			65°			
			-40°C	61°			65°			
			85°C	60°			64°			

† For V<sub>CC±</sub> = ±5 V, V<sub>I(PP)</sub> = ±1 V; for V<sub>CC±</sub> = ±15 V, V<sub>I(PP)</sub> = ±5 V



# TL03x, TL03xA ENHANCED-JFET LOW-POWER LOW-OFFSET OPERATIONAL AMPLIFIERS

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## TL034M and TL034AM electrical characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS		T <sub>A</sub>	TL034M, TL034AM						UNIT
				V <sub>CC±</sub> = ±5 V			V <sub>CC±</sub> = ±15 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>IO</sub> Input offset voltage	V <sub>O</sub> = 0, V <sub>IC</sub> = 0, R <sub>S</sub> = 50 Ω	TL034M	25°C	0.91	3.6		0.78	4	mV	
			Full range†		11			9		
		TL034AM	25°C	0.7	3.5		0.58	1.5		
			Full range†		8.5			6.5		
α <sub>V<sub>IO</sub></sub> Temperature coefficient of input offset voltage	V <sub>O</sub> = 0, V <sub>IC</sub> = 0, R <sub>S</sub> = 50 Ω	TL034M	25°C to 125°C	10.6		10.9		μV/°C		
		TL034AM	25°C to 125°C	10.6		10.9				
Input offset voltage long-term drift‡	V <sub>O</sub> = 0, V <sub>IC</sub> = 0, R <sub>S</sub> = 50 Ω		25°C	0.04		0.04		μV/mo		
I <sub>IO</sub> Input offset current	V <sub>O</sub> = 0, V <sub>IC</sub> = 0 See Figure 5		25°C	1	100		1	100	pA	
			125°C	0.2	10		0.2	10	nA	
I <sub>IB</sub> Input bias current	V <sub>O</sub> = 0, V <sub>IC</sub> = 0 See Figure 5		25°C	2	200		2	200	pA	
			125°C	7	20		8	20	nA	
V <sub>ICR</sub> Common-mode input voltage range			25°C	-1.5 to 4	-3.4 to 5.4		-11.5 to 14	-13.4 to 15.4	V	
			Full range†	-1.5 to 4			-11.5 to 14			
V <sub>OM+</sub> Maximum positive peak output voltage swing	R <sub>L</sub> = 10 kΩ		25°C	3	4.3		13	14	V	
			-55°C	3	4.1		13	14		
			125°C	3	4.4		13	14		
V <sub>OM-</sub> Maximum negative peak output voltage swing	R <sub>L</sub> = 10 kΩ		25°C	-3	-4.2		-12.5	-13.9	V	
			-55°C	-3	-4		-12.5	-13.8		
			125°C	-3	-4.3		-12.5	-14		
A <sub>VD</sub> Large-signal differential voltage amplification§	R <sub>L</sub> = 10 kΩ		25°C	4	12		5	14.3	V/mV	
			-55°C	3	7.1		4	10.4		
			125°C	3	12.9		4	15		
r <sub>i</sub> Input resistance			25°C	10 <sup>12</sup>		10 <sup>12</sup>		Ω		
c <sub>i</sub> Input capacitance			25°C	5		4		pF		
CMRR Common-mode rejection ratio	V <sub>IC</sub> = V <sub>ICRmin</sub> , V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω		25°C	70	87		75	94	dB	
			-55°C	70	87		70	94		
			125°C	70	87		70	94		
k <sub>SVR</sub> Supply-voltage rejection ratio (ΔV <sub>CC±</sub> /ΔV <sub>IO</sub> )	V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω		25°C	75	96		75	96	dB	
			-55°C	75	95		75	95		
			125°C	75	96		75	96		

† Full range is -55°C to 125°C.

‡ Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T<sub>A</sub> = 150°C extrapolated to T<sub>A</sub> = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

§ At V<sub>CC±</sub> = ±5 V, V<sub>O</sub> = ±2.3 V; at V<sub>CC±</sub> = ±15 V, V<sub>O</sub> = ±10 V



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**TL034M and TL034AM electrical characteristics at specified free-air temperature (continued)**

PARAMETER	TEST CONDITIONS	T <sub>A</sub>	TL034M, TL034AM						UNIT
			V <sub>CC±</sub> = ±5 V			V <sub>CC±</sub> = ±15 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
P <sub>D</sub>	Total power dissipation (two amplifiers)	V <sub>O</sub> = 0, No load	25°C	7.7	10		26	34	mW
			-55°C	4.6	12		18.7	45	
			125°C	7.1	12		23.6	45	
I <sub>CC</sub>	Supply current (two amplifiers)	V <sub>O</sub> = 0, No load	25°C	0.77	1		0.87	1.12	mA
			-55°C	0.46	1.2		0.62	1.5	
			125°C	0.71	1.2		0.79	1.5	
V <sub>O1</sub> /V <sub>O2</sub>	Crosstalk attenuation	A <sub>VD</sub> = 100	25°C	120			120		dB

**TL034M and TL034AM operating characteristics at specified free-air temperature**

PARAMETER	TEST CONDITIONS	T <sub>A</sub>	TL034M, TL034AM						UNIT		
			V <sub>CC±</sub> = ±5 V			V <sub>CC±</sub> = ±15 V					
			MIN	TYP	MAX	MIN	TYP	MAX			
SR <sub>+</sub>	Positive slew rate at unity gain†	R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF See Figure 1	25°C	2			1.5 2.9			V/μs	
			-55°C	1.4			1 1.9				
			125°C	2.4			1 3.5				
SR <sub>-</sub>	Negative slew rate at unity gain†	R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF See Figure 1	25°C	3.9			1.5 5.1			V/μs	
			-55°C	3.2			1 4.6				
			125°C	4.1			1 4.7				
t <sub>r</sub>	Rise time	V <sub>I(PP)</sub> = ±10 V, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF See Figures 1 and 2	25°C	138			132			ns	
			-55°C	142			123				
			125°C	166			58				
t <sub>f</sub>	Fall time	V <sub>I(PP)</sub> = ±10 V, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF See Figure 1	25°C	138			132			ns	
			-55°C	142			123				
			125°C	166			158				
Overshoot factor		V <sub>I(PP)</sub> = ±10 V, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF See Figures 1 and 2	25°C	11%			5%				
			-55°C	16%			6%				
			125°C	14%			8%				
V <sub>n</sub>	Equivalent input noise voltage	TL034M	R <sub>S</sub> = 20 Ω See Figure 3	f = 10 Hz	25°C			83			nV/√Hz
				f = 1 kHz	25°C			43			
		TL034AM		f = 10 Hz	25°C			83			
				f = 1 kHz	25°C			43			
I <sub>n</sub>	Equivalent input noise current	f = 1 kHz	25°C	0.003			0.003			pA/√Hz	
B1	Unity-gain bandwidth	V <sub>I</sub> = 10 mV, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 25 pF See Figure 4	25°C	1			1.1			MHz	
			-55°C	1			1.1				
			125°C	0.9			0.9				
φ <sub>m</sub>	Phase margin at unity gain	V <sub>I</sub> = 10 mV, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 25 pF See Figure 4	25°C	61°			65°				
			-55°C	57°			64°				
			125°C	59°			62°				

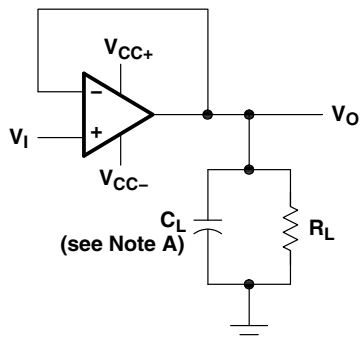
† For V<sub>CC±</sub> = ±5 V, V<sub>I(PP)</sub> = ±1 V; for V<sub>CC±</sub> = ±15 V, V<sub>I(PP)</sub> = ±5 V



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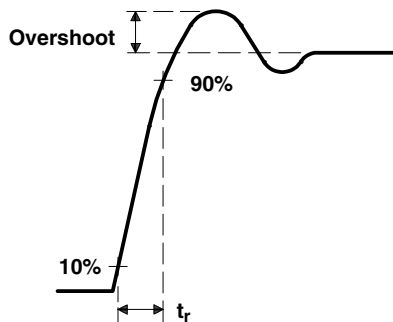
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**PARAMETER MEASUREMENT INFORMATION**

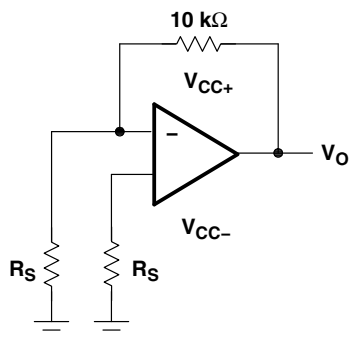


NOTE A:  $C_L$  includes fixture capacitance.

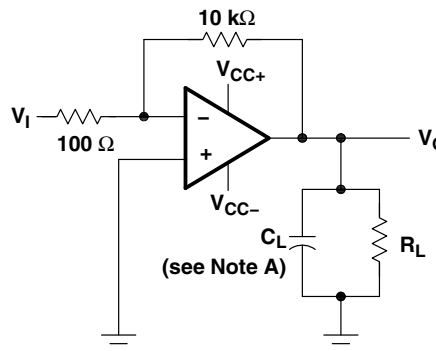
**Figure 1. Slew-Rate and Overshoot Test Circuit**



**Figure 2. Rise Time and Overshoot Waveform**

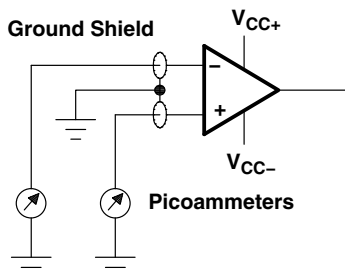


**Figure 3. Noise-Voltage Test Circuit**



NOTE A:  $C_L$  includes fixture capacitance.

**Figure 4. Unity-Gain Bandwidth and Phase-Margin Test Circuit**



**Figure 5. Input-Bias and Offset-Current Test Circuit**



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## PARAMETER MEASUREMENT INFORMATION

### typical values

Typical values presented in this data sheet represent the median (50% point) of device parametric performance.

### input bias and offset current

At the picoampere bias current level typical of the TL03x and TL03xA, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test-socket leakages easily can exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted into the socket and a second test that measures both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

### noise

With the increasing emphasis on low noise levels in many of today's applications, the input noise voltage density is performed at  $f = 1$  kHz, unless otherwise noted.

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**TYPICAL CHARACTERISTICS**

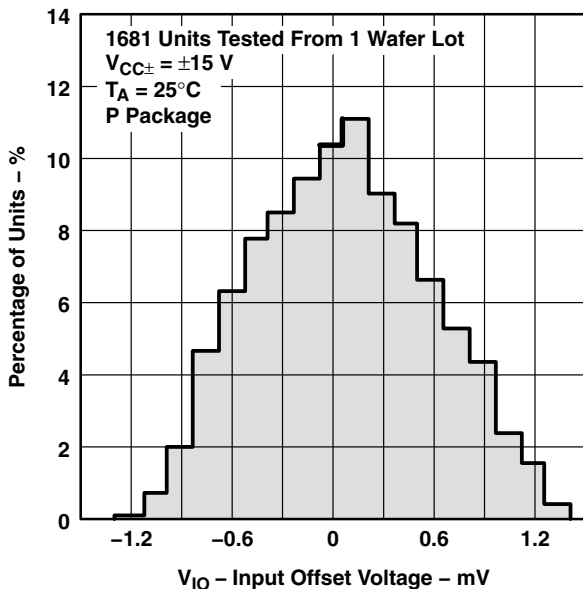
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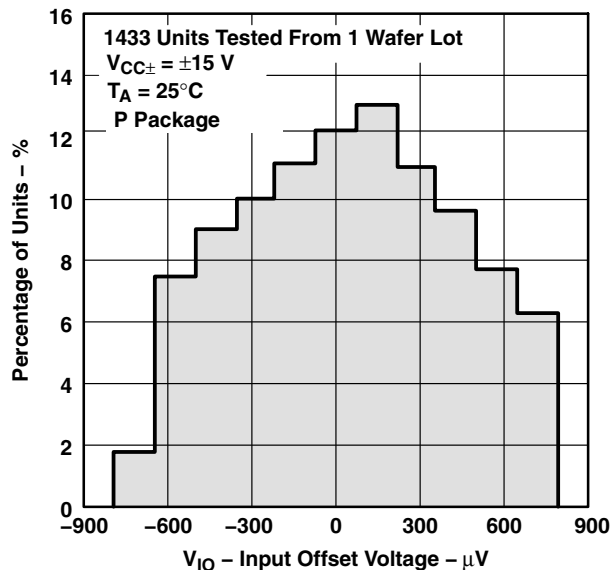
**TYPICAL CHARACTERISTICS**

**DISTRIBUTION OF TL031  
INPUT OFFSET VOLTAGE**



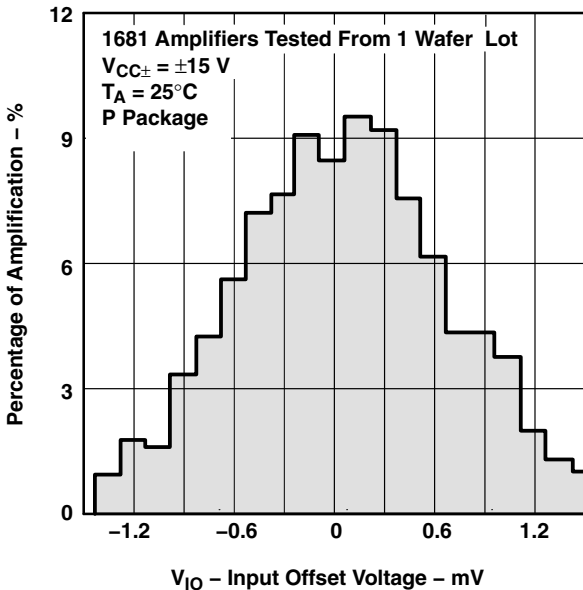
**Figure 6**

**DISTRIBUTION OF TL031A  
INPUT OFFSET VOLTAGE**



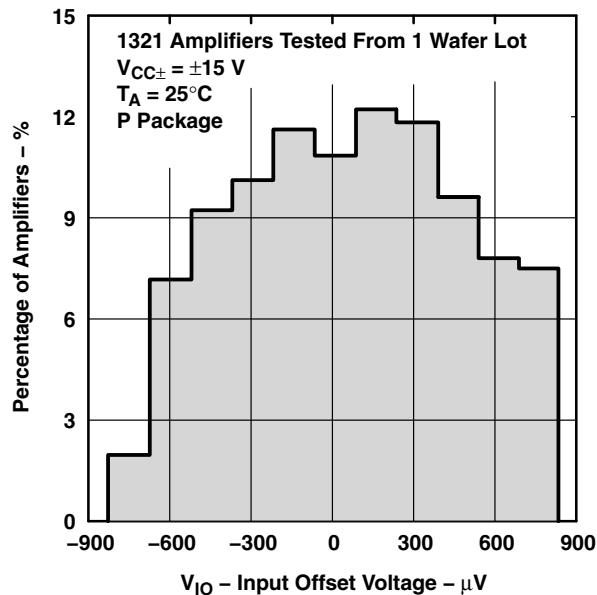
**Figure 7**

**DISTRIBUTION OF TL032  
INPUT OFFSET VOLTAGE**



**Figure 8**

**DISTRIBUTION OF TL032A  
INPUT OFFSET VOLTAGE**



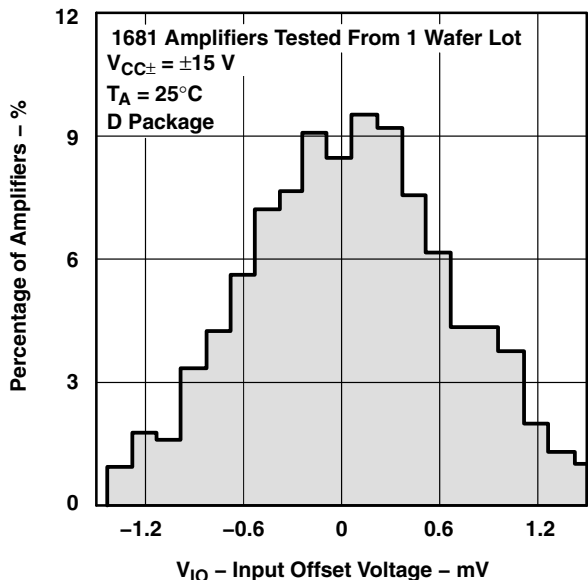
**Figure 9**

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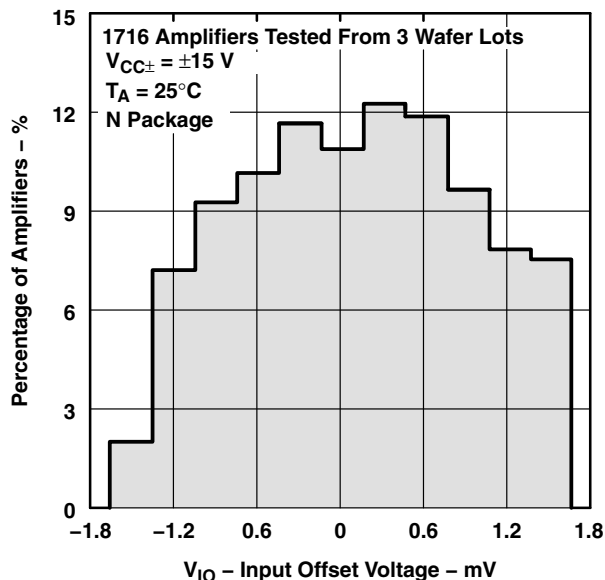
## TYPICAL CHARACTERISTICS

**DISTRIBUTION OF TL034  
INPUT OFFSET VOLTAGE**



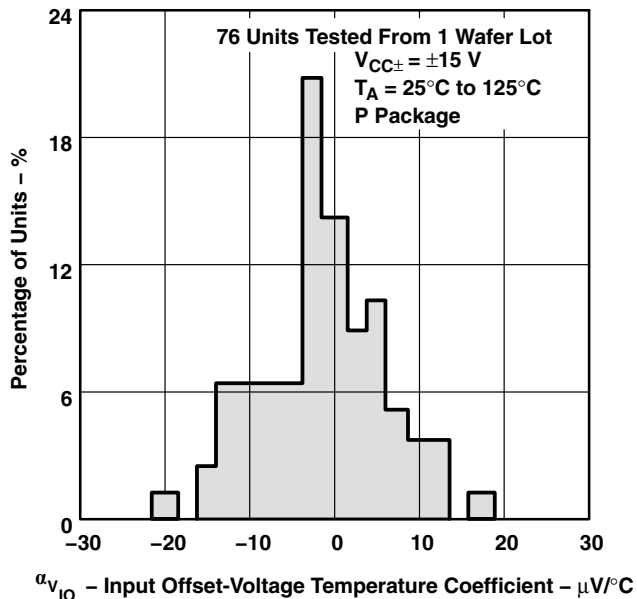
**Figure 10**

**DISTRIBUTION OF TL034A  
INPUT OFFSET VOLTAGE**



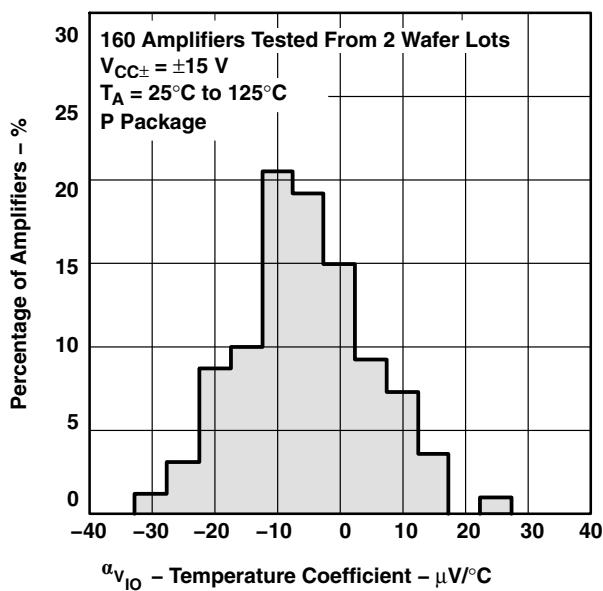
**Figure 11**

**DISTRIBUTION OF TL031  
INPUT OFFSET-VOLTAGE  
TEMPERATURE COEFFICIENT**



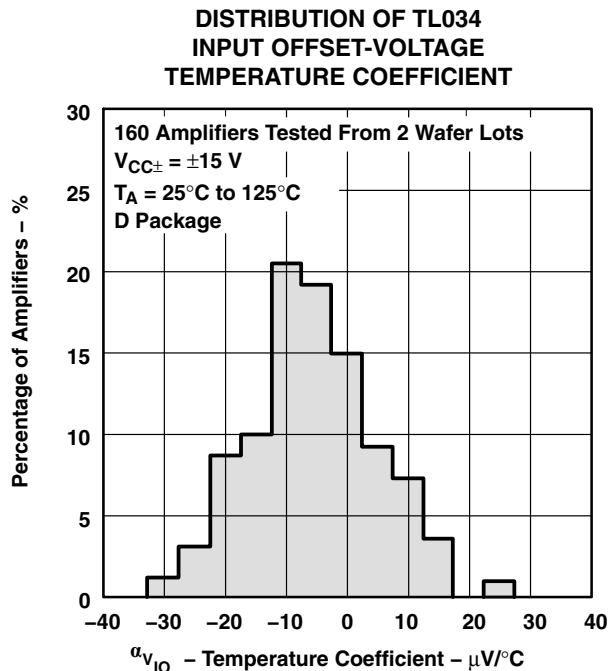
**Figure 12**

**DISTRIBUTION OF TL032  
INPUT OFFSET-VOLTAGE  
TEMPERATURE COEFFICIENT**

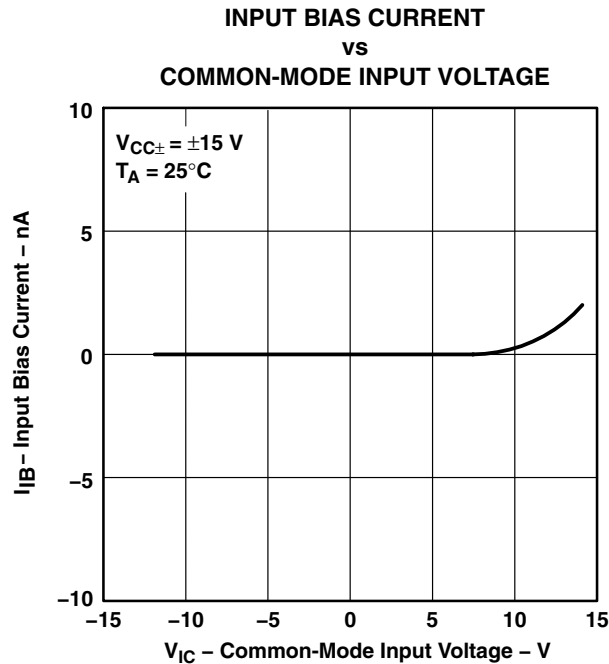


**Figure 13**

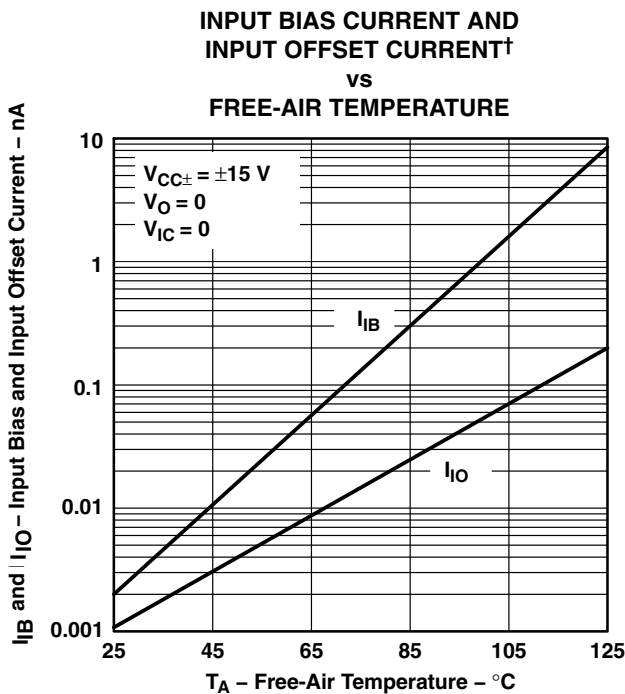
**TYPICAL CHARACTERISTICS**



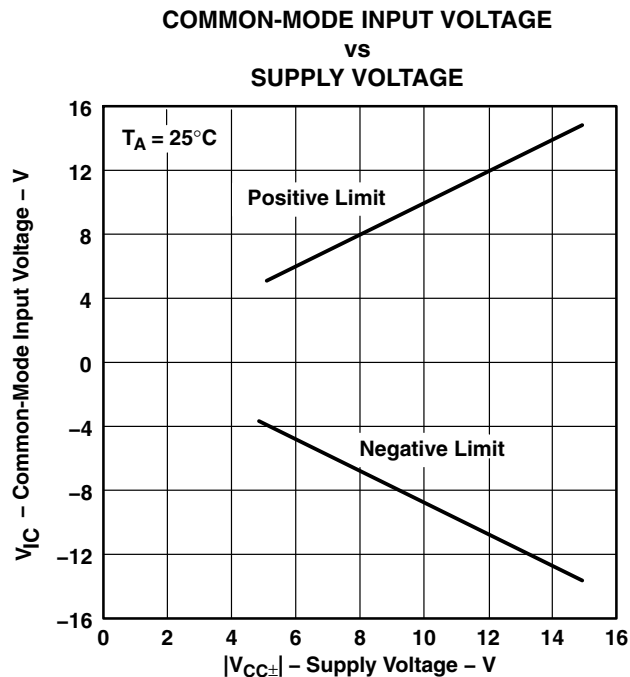
**Figure 14**



**Figure 15**



**Figure 16**



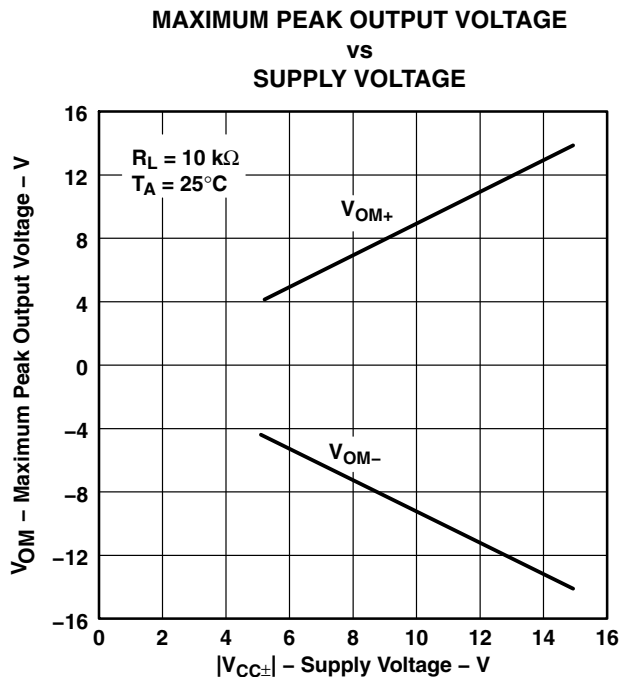
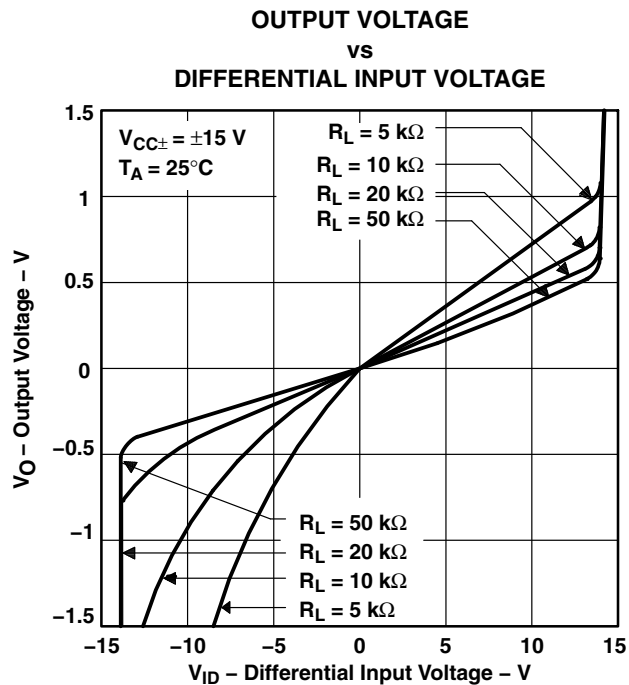
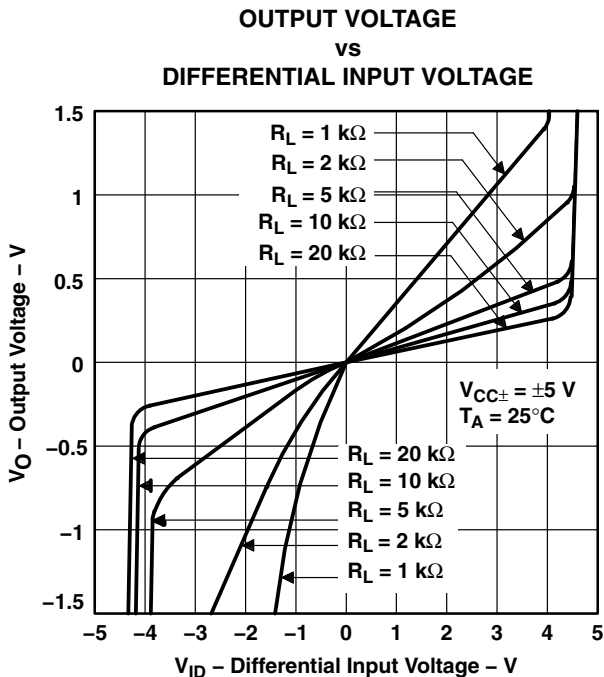
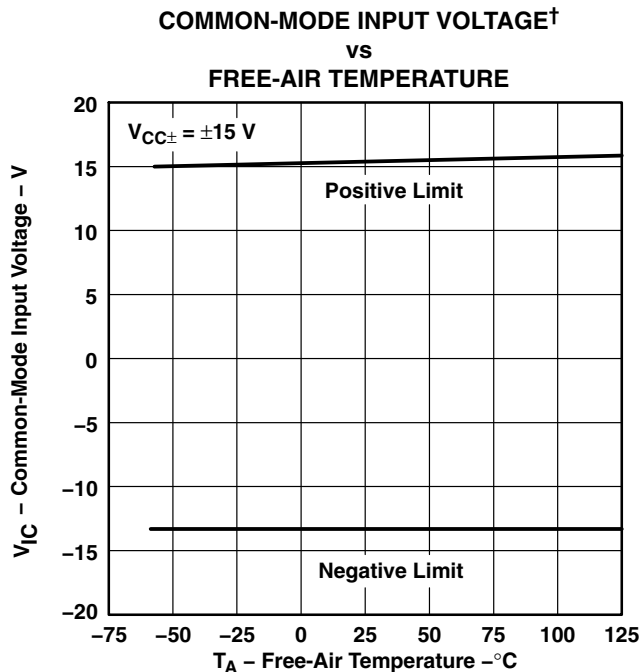
**Figure 17**

† Data at high and low temperatures are applicable only within the recommended operating free-air temperature ranges of the various devices.

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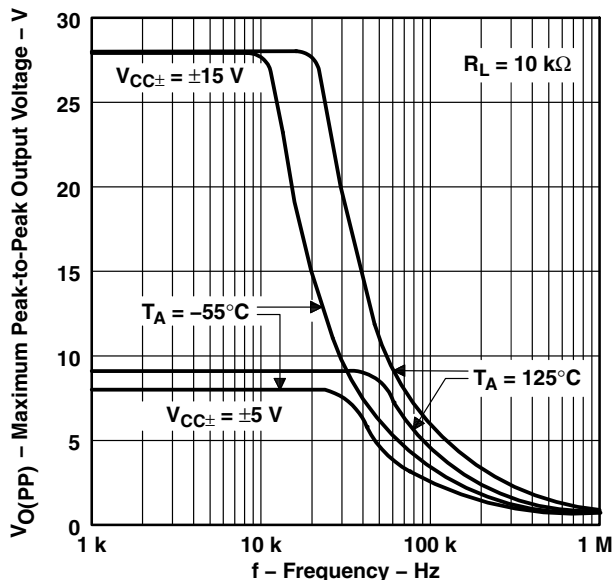
## TYPICAL CHARACTERISTICS



† Data at high and low temperatures are applicable only within the recommended operating free-air temperature ranges of the various devices.

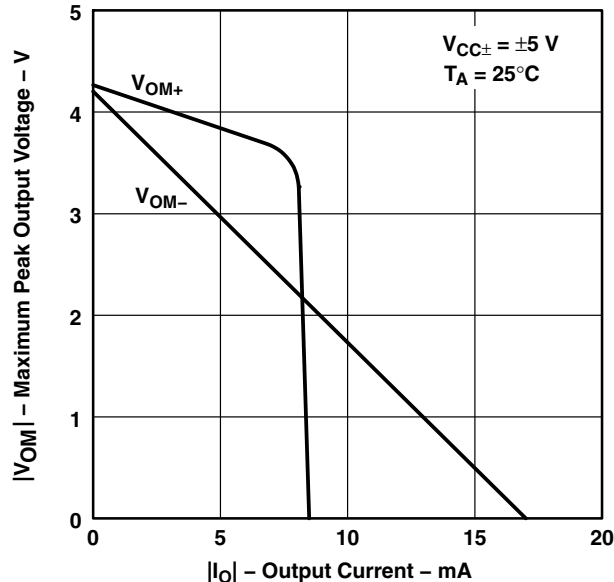
**TYPICAL CHARACTERISTICS**

**MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE†  
vs  
FREQUENCY**



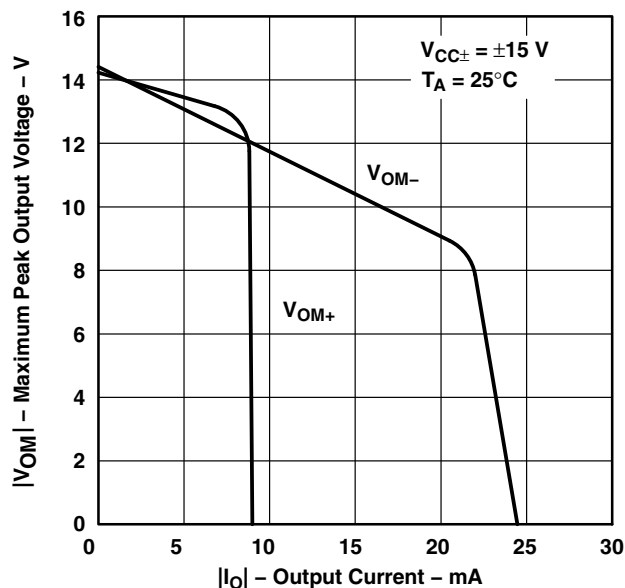
**Figure 22**

**MAXIMUM PEAK OUTPUT VOLTAGE  
vs  
OUTPUT CURRENT**



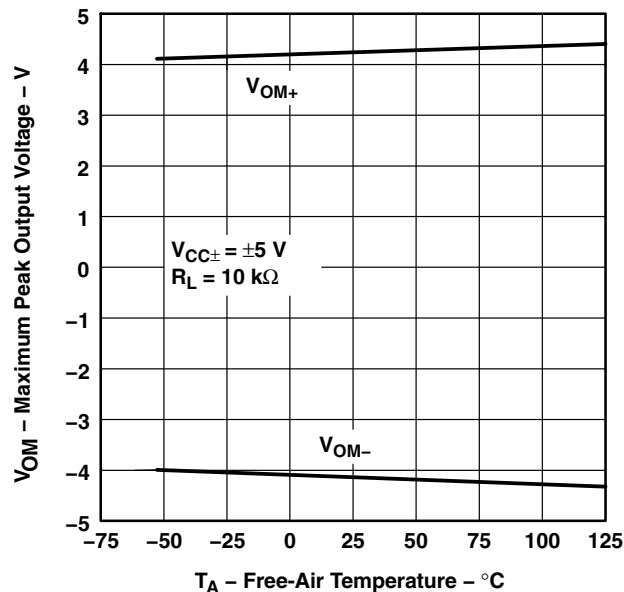
**Figure 23**

**MAXIMUM PEAK OUTPUT VOLTAGE  
vs  
OUTPUT CURRENT**



**Figure 24**

**MAXIMUM PEAK OUTPUT VOLTAGE†  
vs  
FREE-AIR TEMPERATURE**



**Figure 25**

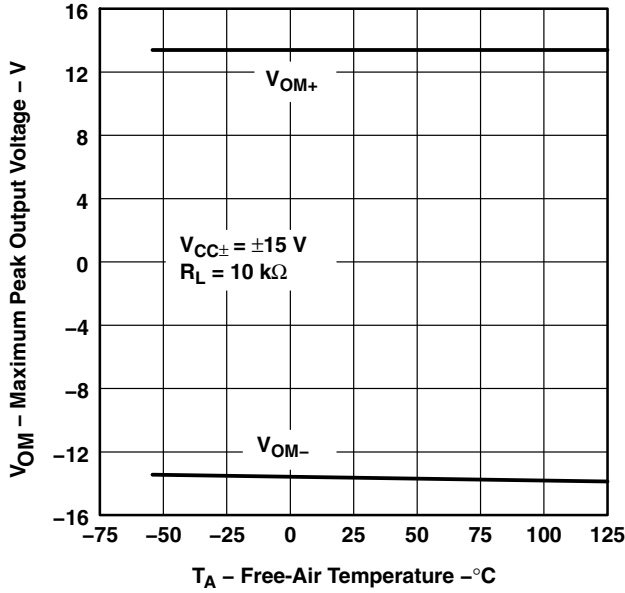
† Data at high and low temperatures are applicable only within the recommended operating free-air temperature ranges of the various devices.

**TL03x, TL03xA**  
**ENHANCED-JFET LOW-POWER LOW-OFFSET**  
**OPERATIONAL AMPLIFIERS**

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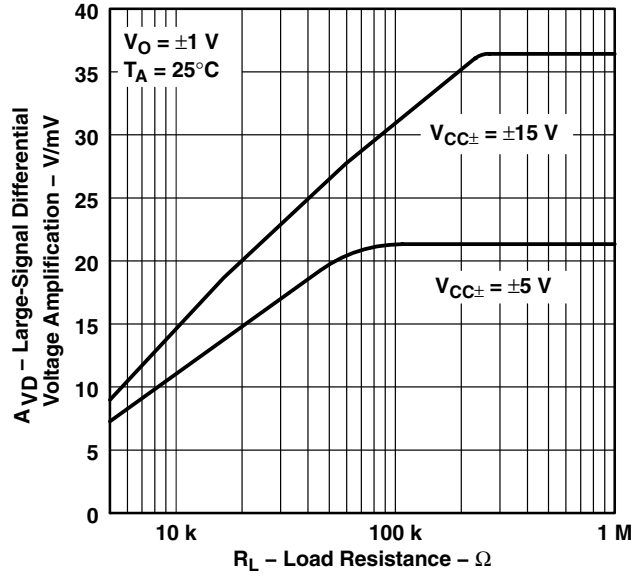
**TYPICAL CHARACTERISTICS**

**MAXIMUM PEAK OUTPUT VOLTAGE†**  
**vs**  
**FREE-AIR TEMPERATURE**



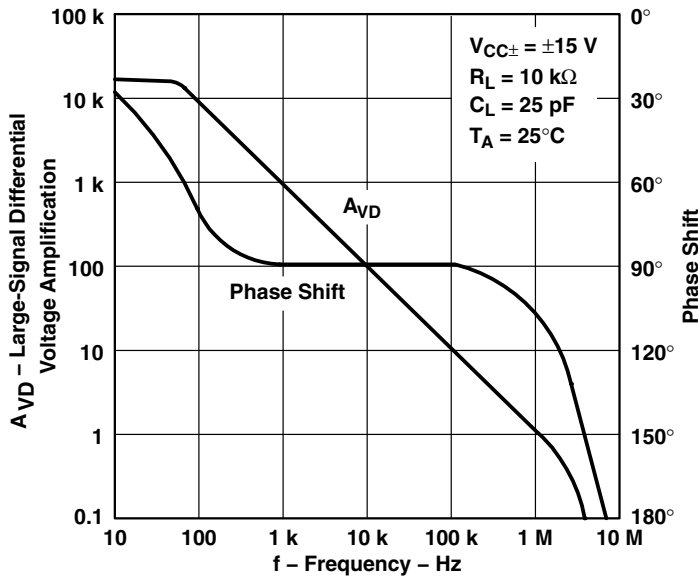
**Figure 26**

**LARGE-SIGNAL DIFFERENTIAL**  
**VOLTAGE AMPLIFICATION**  
**vs**  
**LOAD RESISTANCE**



**Figure 27**

**LARGE-SIGNAL DIFFERENTIAL VOLTAGE**  
**AMPLIFICATION AND PHASE SHIFT**  
**vs**  
**FREQUENCY**



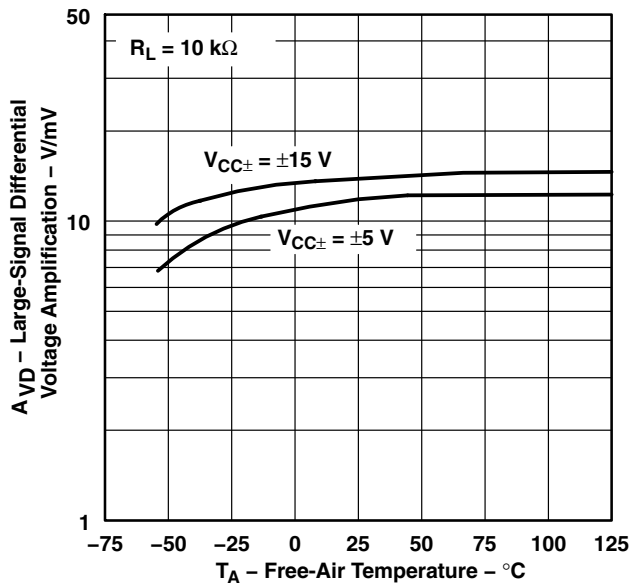
**Figure 28**

† Data at high and low temperatures are applicable only within the recommended operating free-air temperature ranges of the various devices.



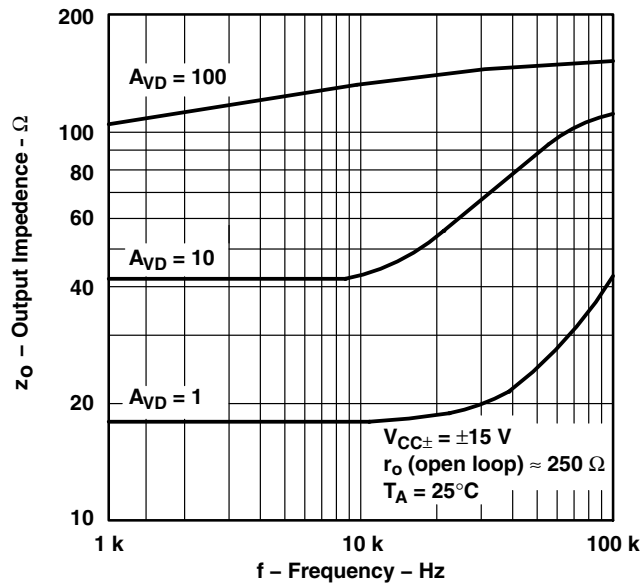
**TYPICAL CHARACTERISTICS**

**LARGE-SIGNAL DIFFERENTIAL  
 VOLTAGE AMPLIFICATION†  
 vs  
 FREE-AIR TEMPERATURE**



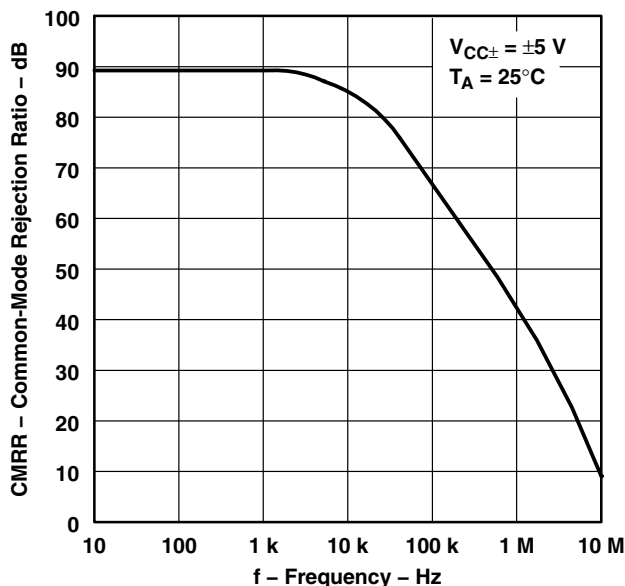
**Figure 29**

**OUTPUT IMPEDANCE  
 vs  
 FREQUENCY**



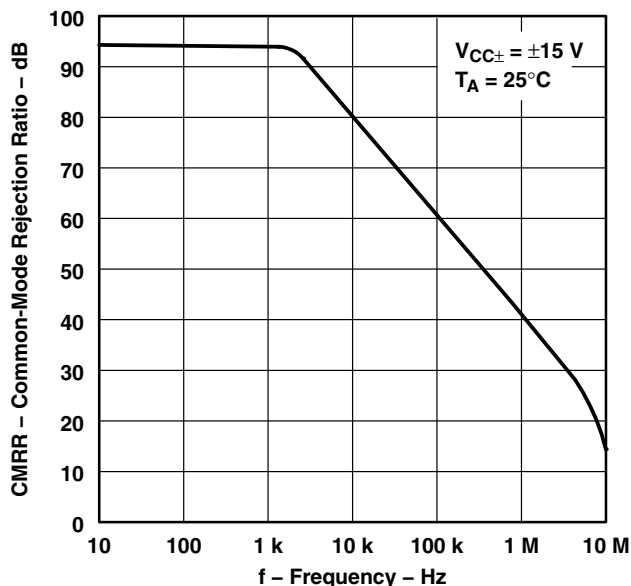
**Figure 30**

**COMMON-MODE REJECTION RATIO  
 vs  
 FREQUENCY**



**Figure 31**

**COMMON-MODE REJECTION RATIO  
 vs  
 FREQUENCY**



**Figure 32**

† Data at high and low temperatures are applicable only within the recommended operating free-air temperature ranges of the various devices.

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## TYPICAL CHARACTERISTICS

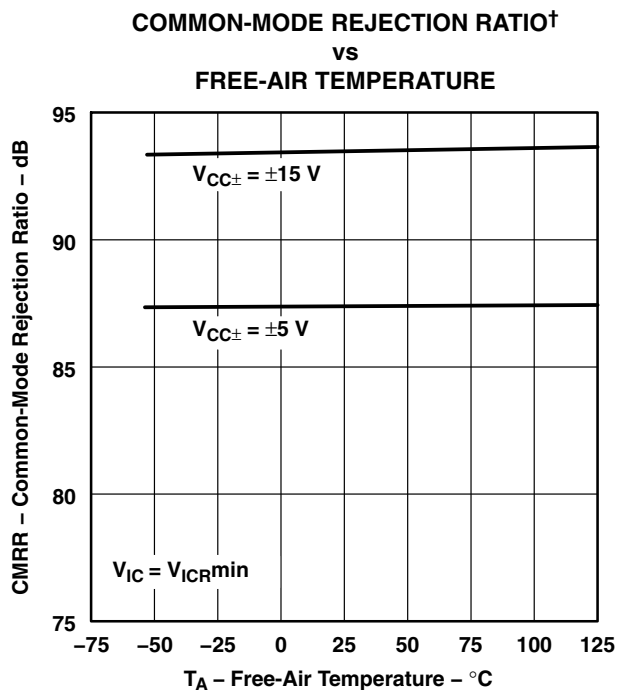


Figure 33

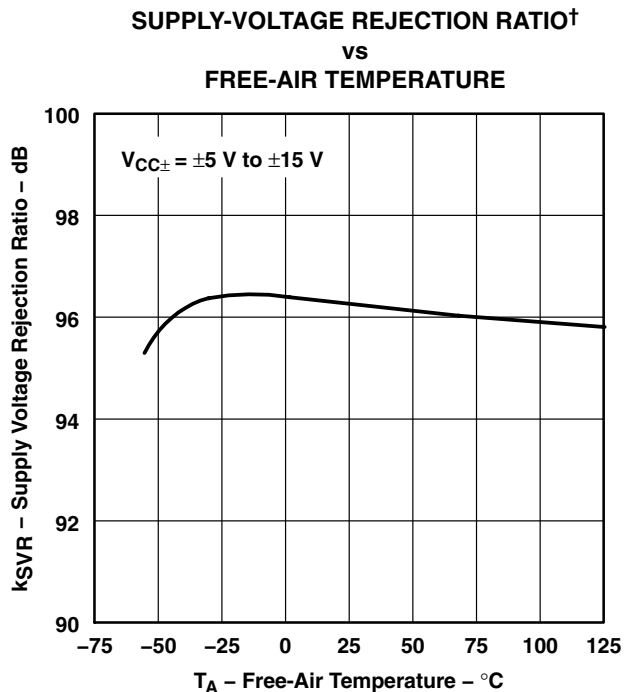


Figure 34

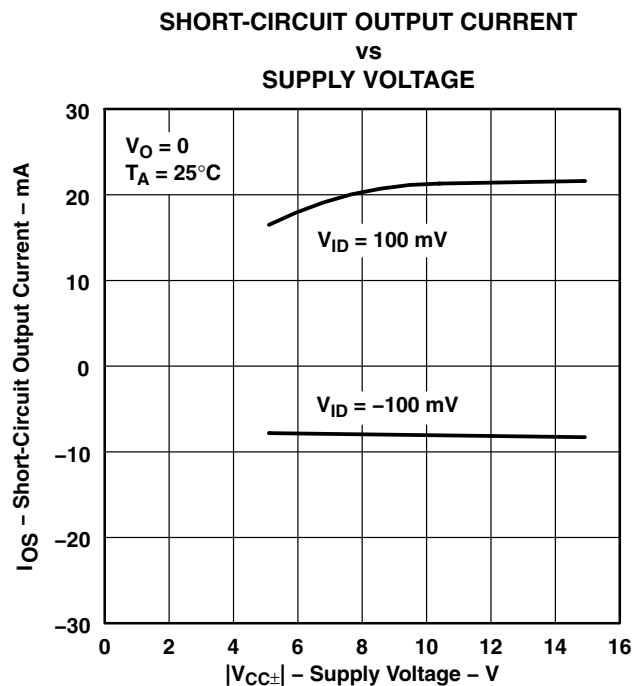


Figure 35

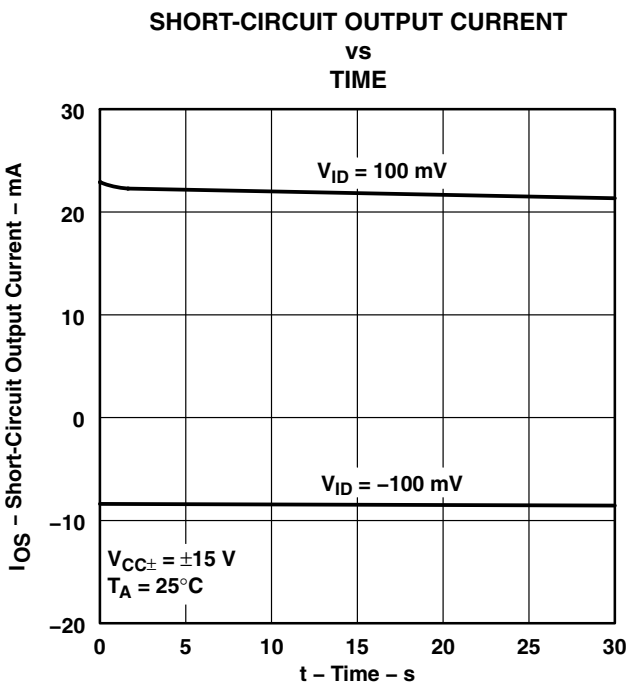
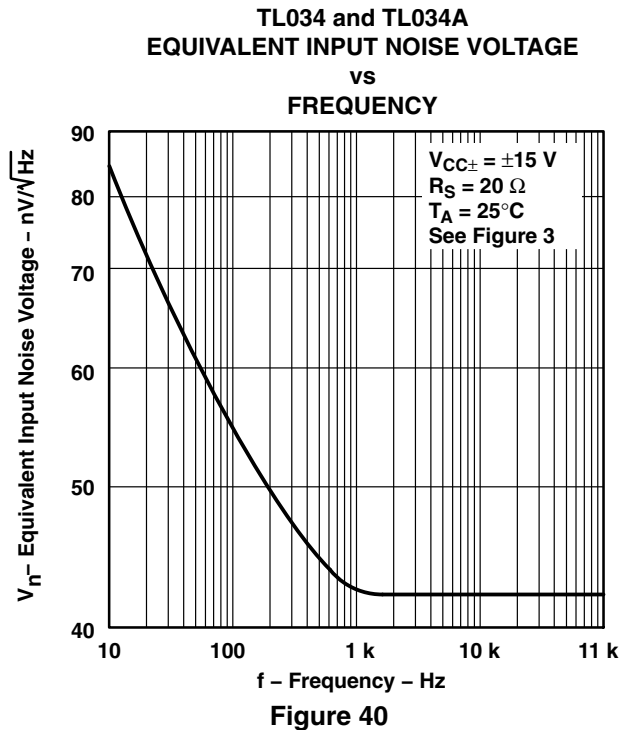
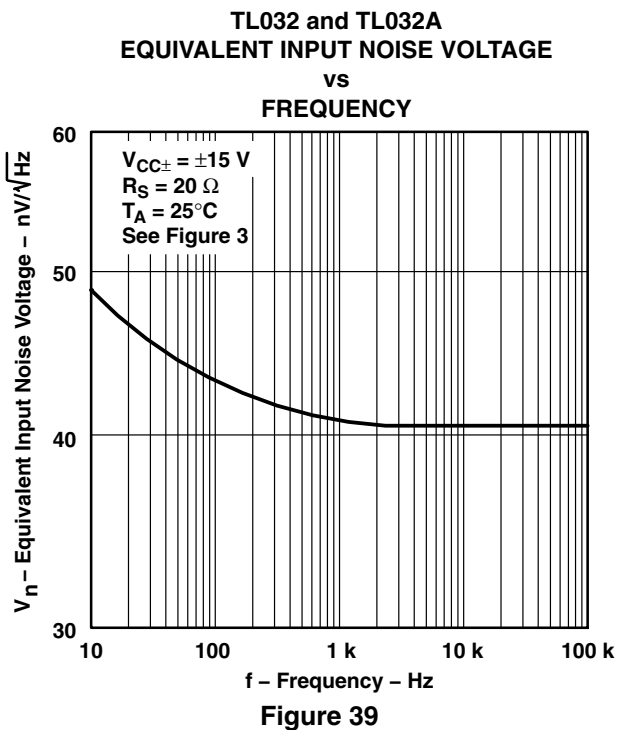
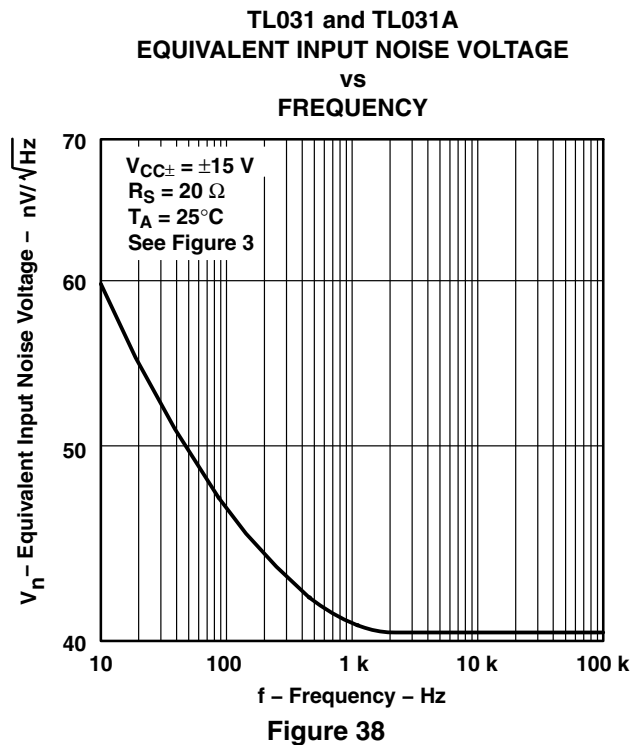
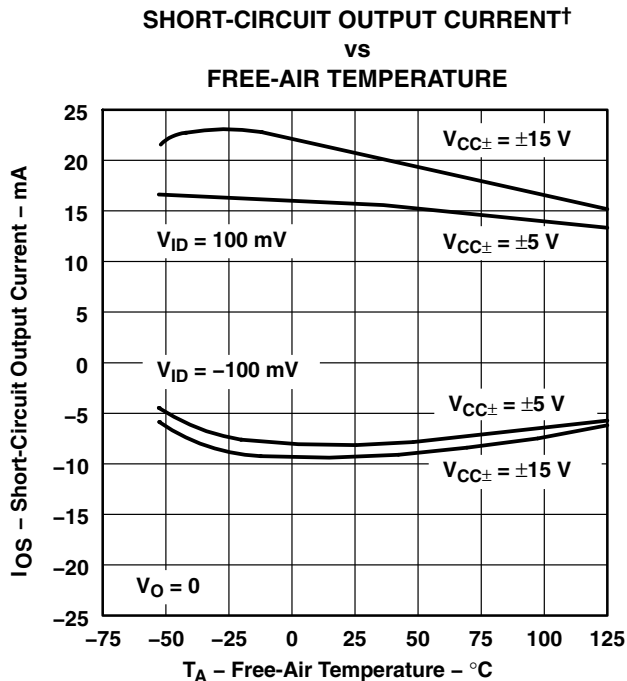


Figure 36

† Data at high and low temperatures are applicable only within the recommended operating free-air temperature ranges of the various devices.

**TYPICAL CHARACTERISTICS**



† Data at high and low temperatures are applicable only within the recommended operating free-air temperature ranges of the various devices.

# TL03x, TL03xA ENHANCED-JFET LOW-POWER LOW-OFFSET OPERATIONAL AMPLIFIERS

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## TYPICAL CHARACTERISTICS

TL031 and TL031A  
SUPPLY CURRENT†  
vs  
SUPPLY VOLTAGE

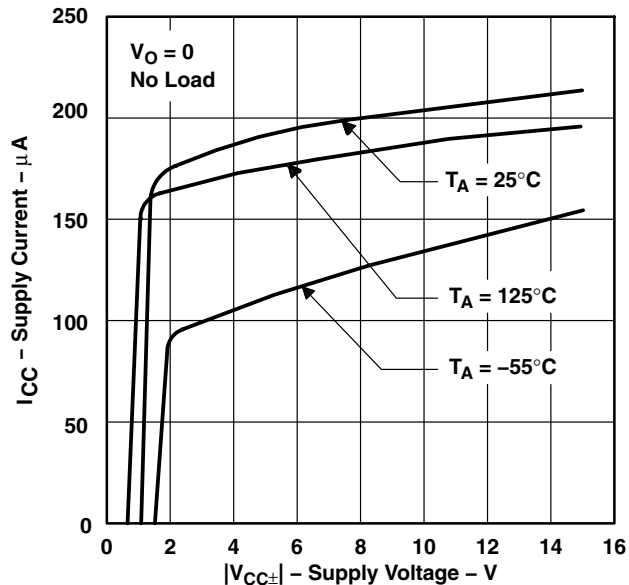


Figure 41

TL032 and TL032A  
SUPPLY CURRENT†  
vs  
SUPPLY VOLTAGE

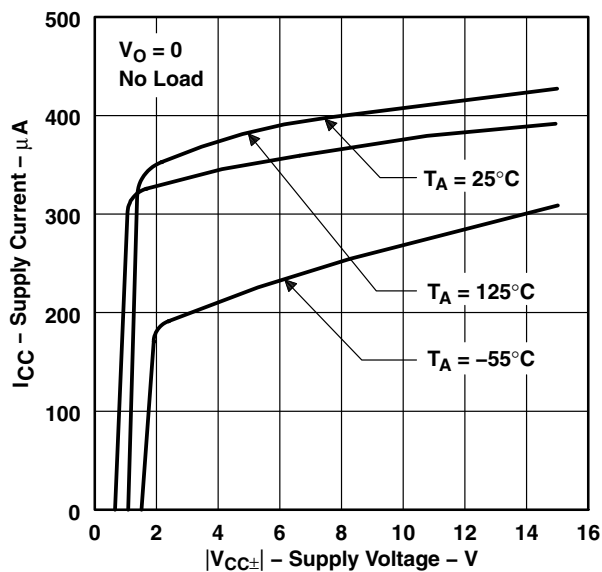


Figure 42

TL034 and TL034A  
SUPPLY CURRENT†  
vs  
SUPPLY VOLTAGE

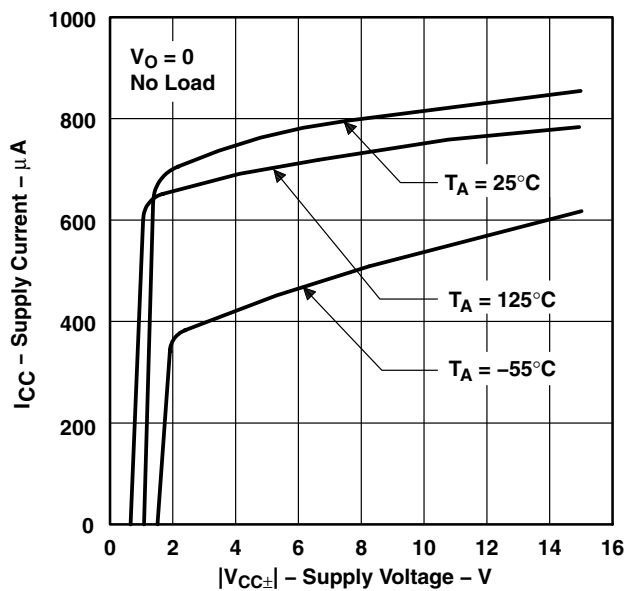


Figure 43

TL031 and TL031A  
SUPPLY CURRENT†  
vs  
FREE-AIR TEMPERATURE

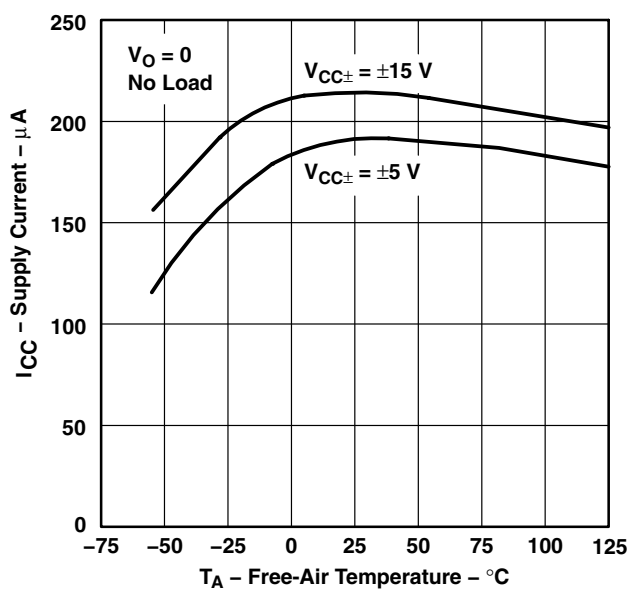
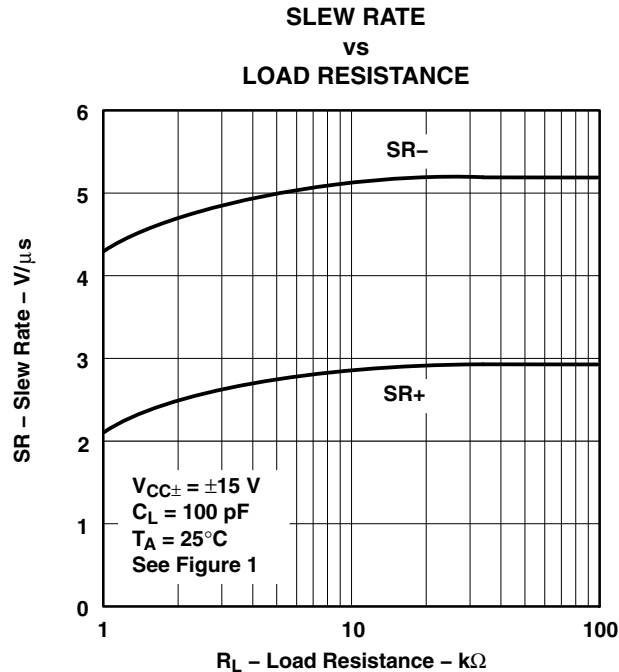
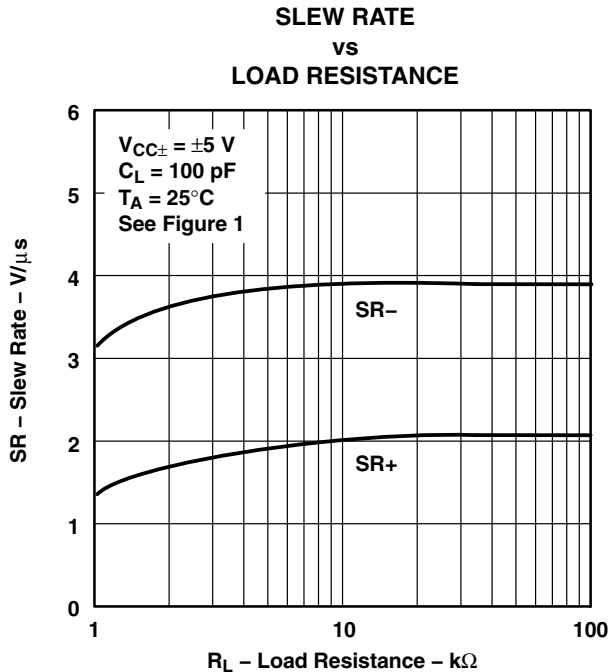
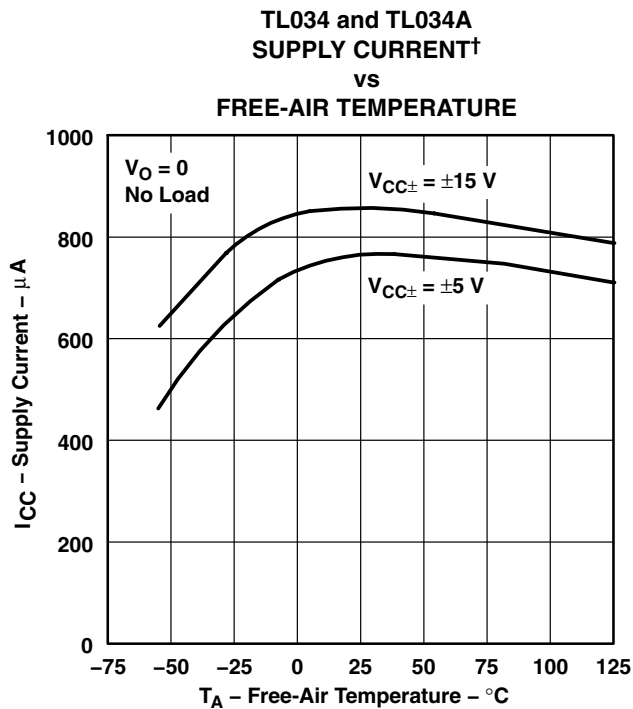
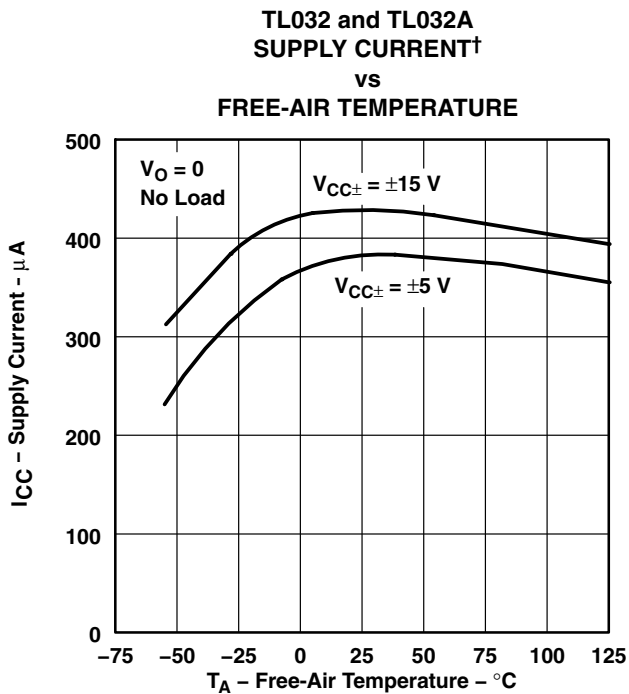


Figure 44

† Data at high and low temperatures are applicable only within the recommended operating free-air temperature ranges of the various devices.

**TYPICAL CHARACTERISTICS**



† Data at high and low temperatures are applicable only within the recommended operating free-air temperature ranges of the various devices.

# TL03x, TL03xA ENHANCED-JFET LOW-POWER LOW-OFFSET OPERATIONAL AMPLIFIERS

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## TYPICAL CHARACTERISTICS

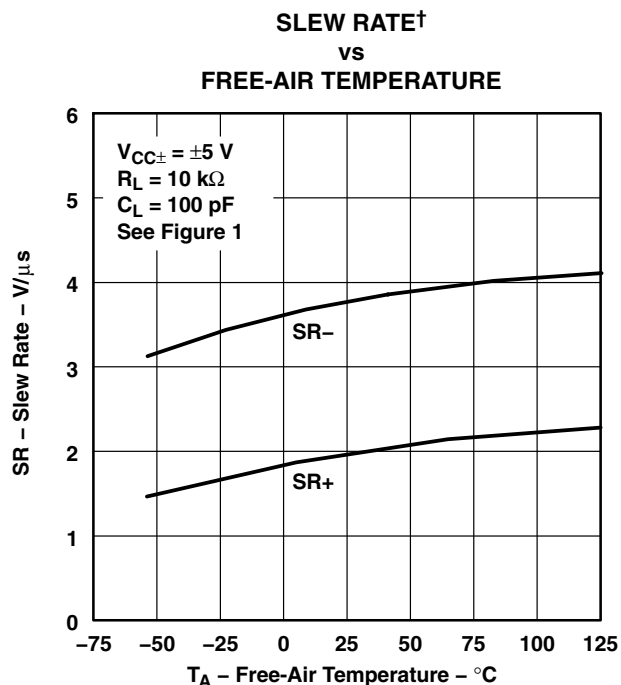


Figure 49

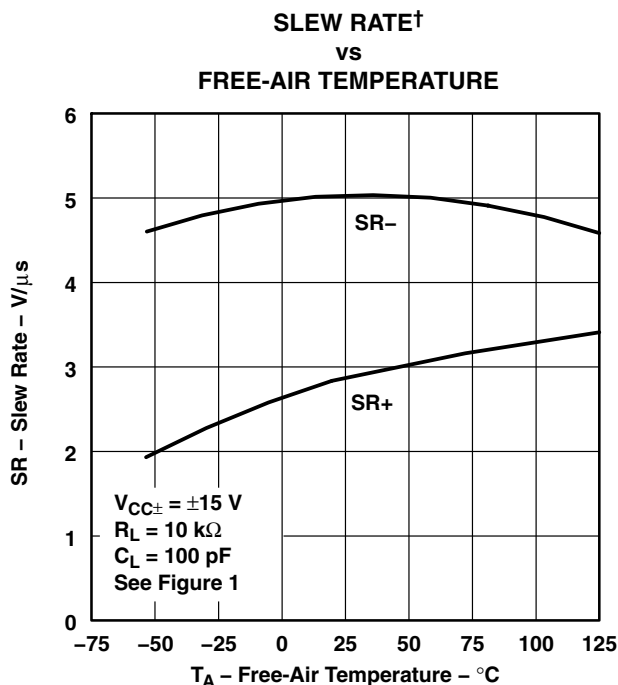


Figure 50

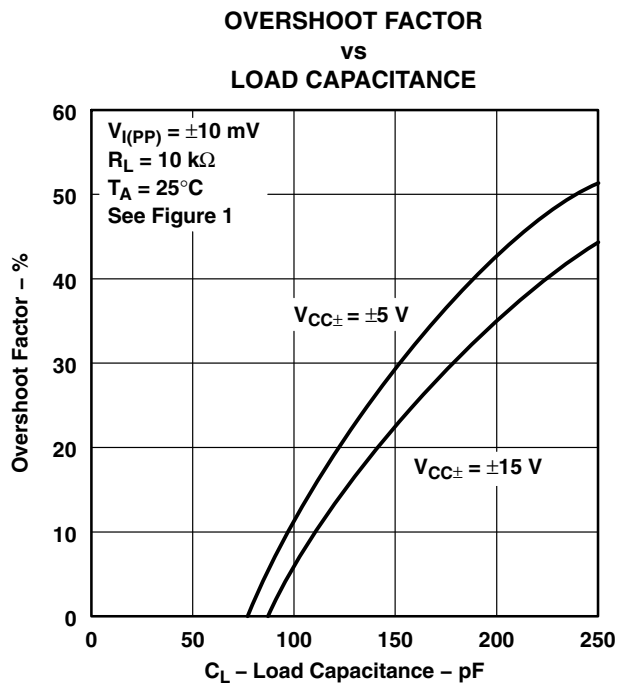


Figure 51

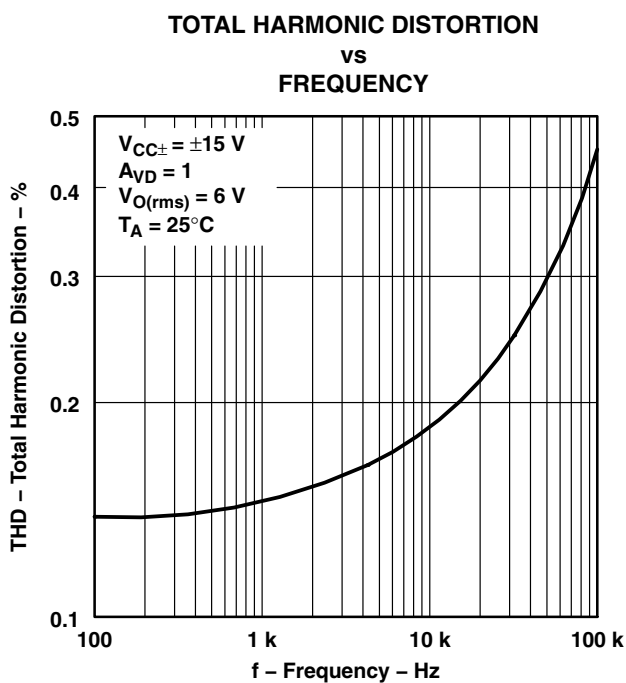
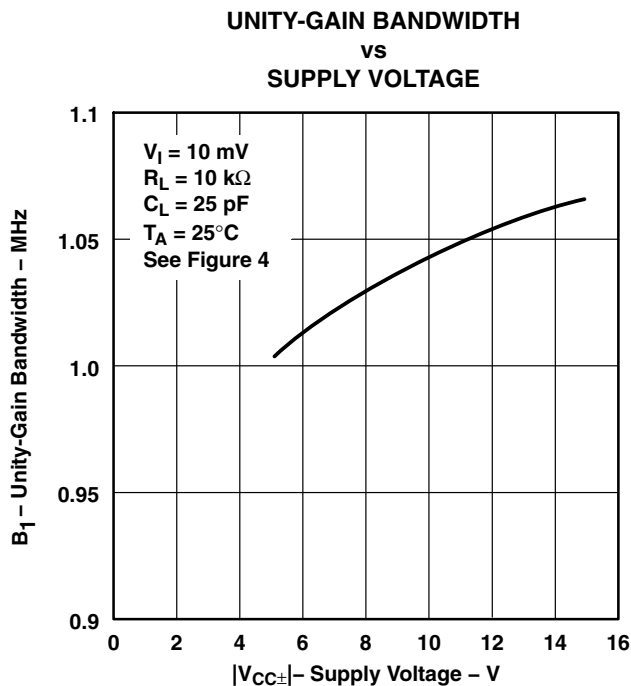


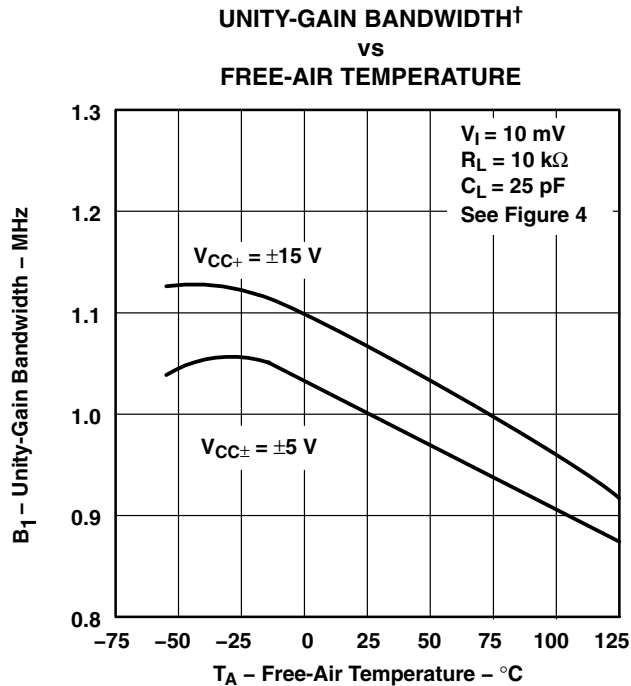
Figure 52

† Data at high and low temperatures are applicable only within the recommended operating free-air temperature ranges of the various devices.

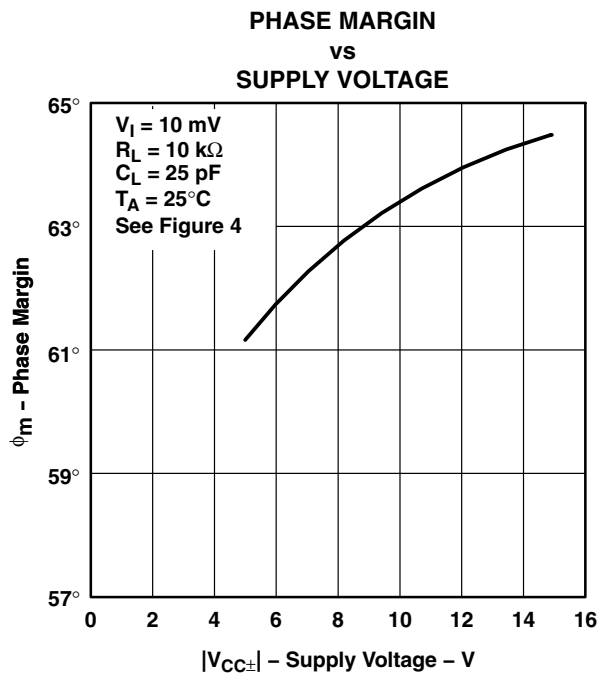
**TYPICAL CHARACTERISTICS**



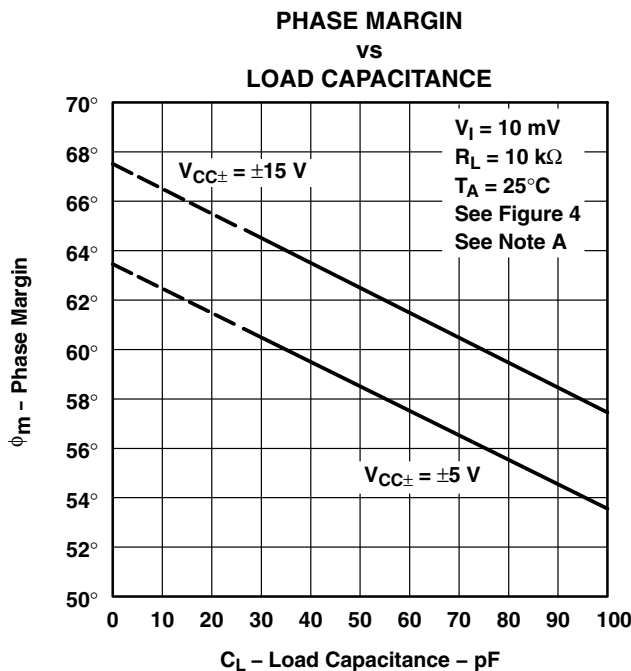
**Figure 53**



**Figure 54**



**Figure 55**



NOTE A: Values of phase margin below a load capacitance of 25 pF were estimated.

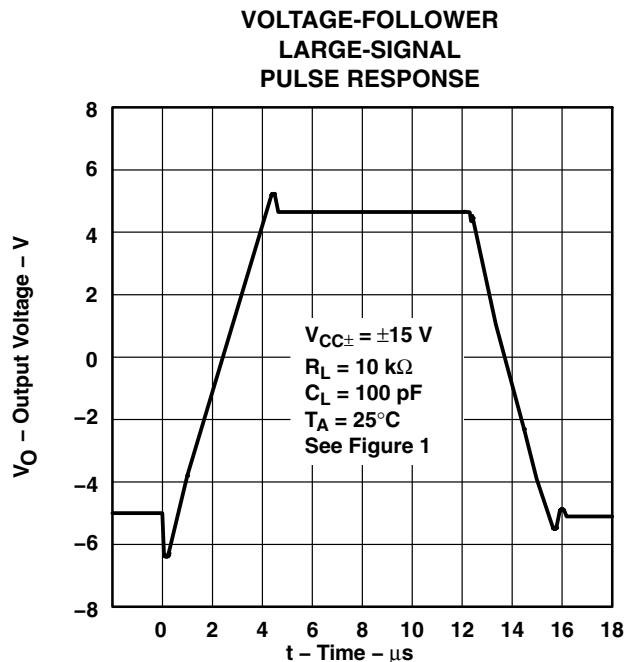
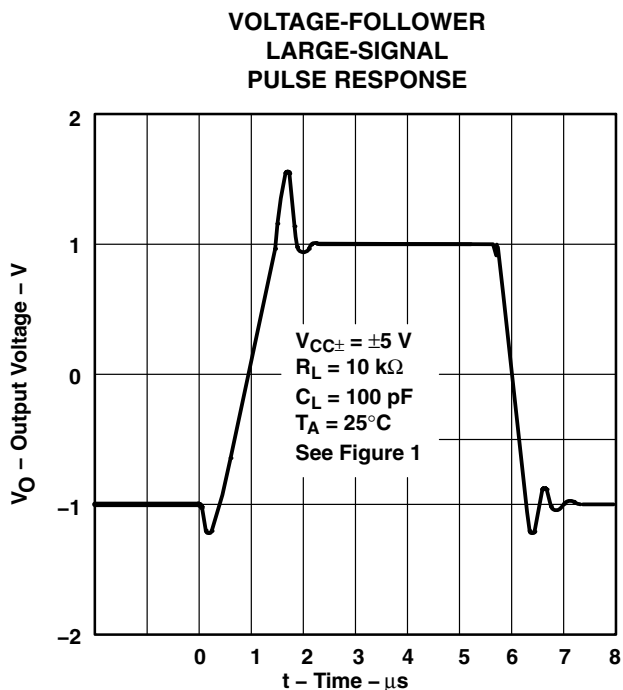
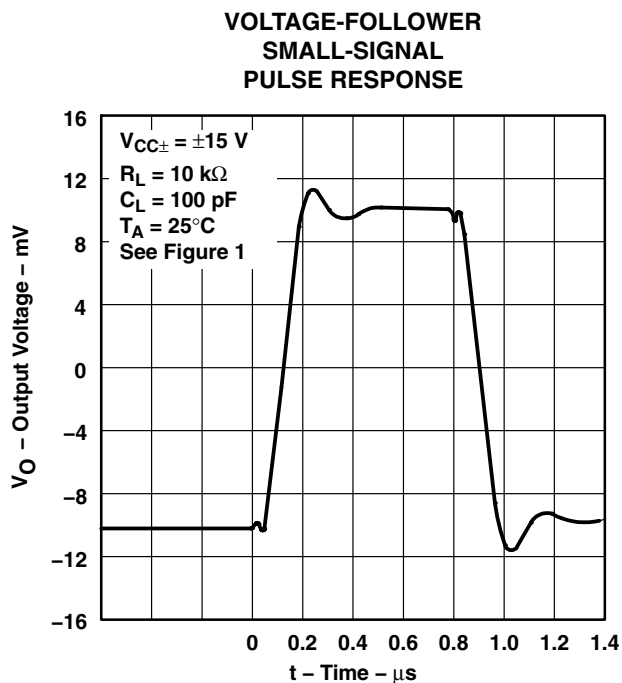
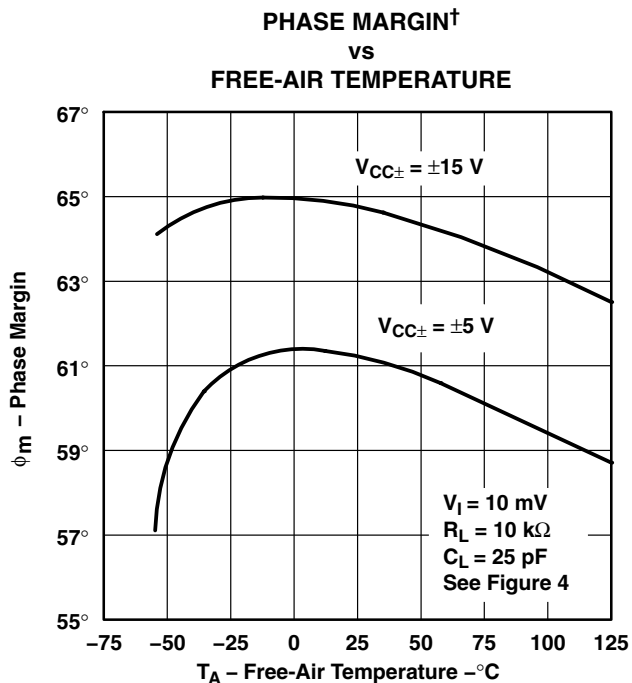
**Figure 56**

† Data at high and low temperatures are applicable only within the recommended operating free-air temperature ranges of the various devices.

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## TYPICAL CHARACTERISTICS



† Data at high and low temperatures are applicable only within the recommended operating free-air temperature ranges of the various devices.



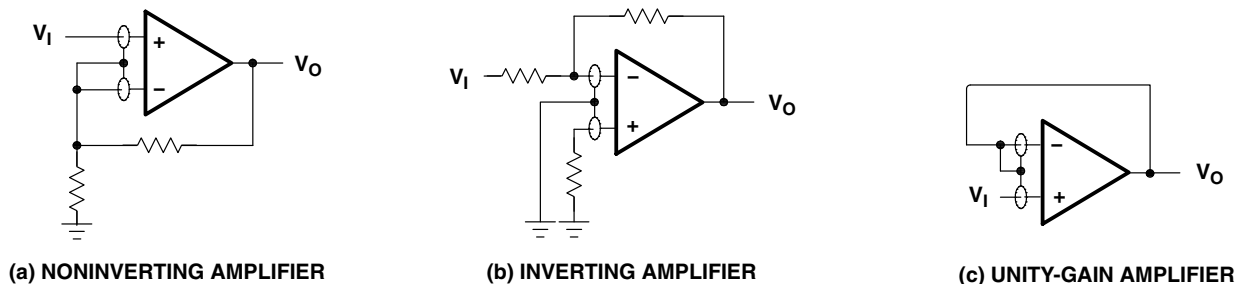
## APPLICATION INFORMATION

### input characteristics

The TL03x and TL03xA are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction.

Due to the extremely high input impedance and resulting low bias-current requirements, the TL03x and TL03xA are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets easily can exceed bias-current requirements and cause degradation in system performance. It is a good practice to include guard rings around inputs (see Figure 61). These guard rings should be driven from a low-impedance source at the same voltage level as the common-mode input.

Unused amplifiers should be connected as grounded unity-gain followers to avoid oscillation.



**Figure 61. Use of Guard Rings**

# TL03x, TL03xA ENHANCED-JFET LOW-POWER LOW-OFFSET OPERATIONAL AMPLIFIERS

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## APPLICATION INFORMATION

### output characteristics

All operating characteristics (except bandwidth and phase margin) are specified with 100-pF load capacitance. The TL03x and TL03xA drive higher capacitive loads; however, as the load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation. The value of the load capacitance at which oscillation occurs varies with production lots. If an application appears to be sensitive to oscillation due to load capacitance, adding a small resistance in series with the load should alleviate the problem (see Figure 63). Capacitive loads of 1000 pF and larger can be driven if enough resistance is added in series with the output (see Figure 62).

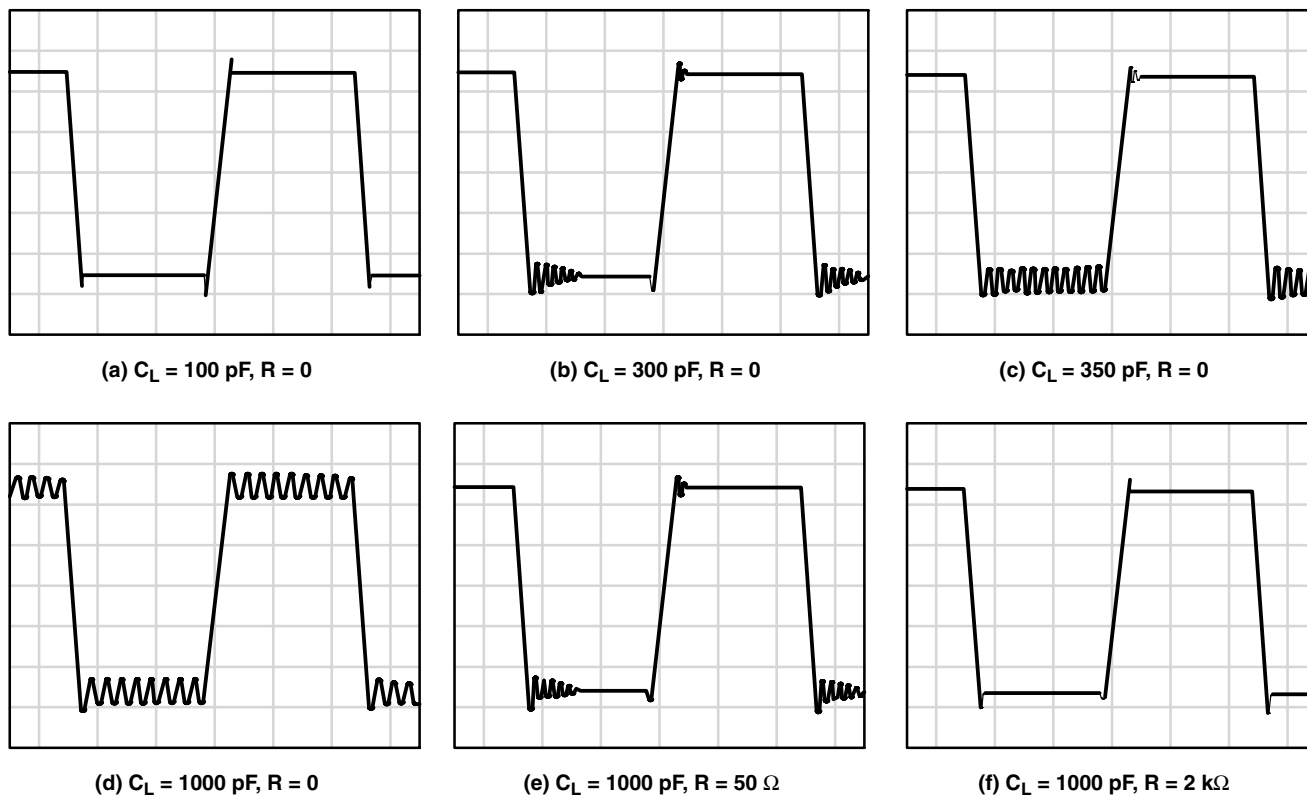


Figure 62. Effect of Capacitive Loads

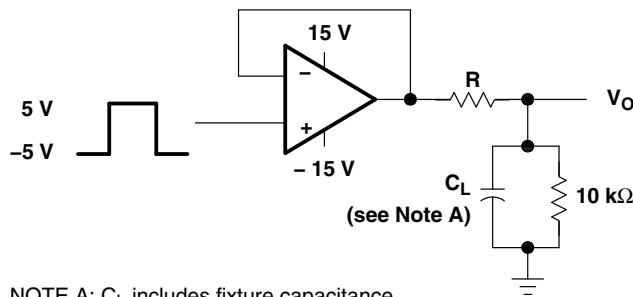


Figure 63. Test Circuit for Output Characteristics

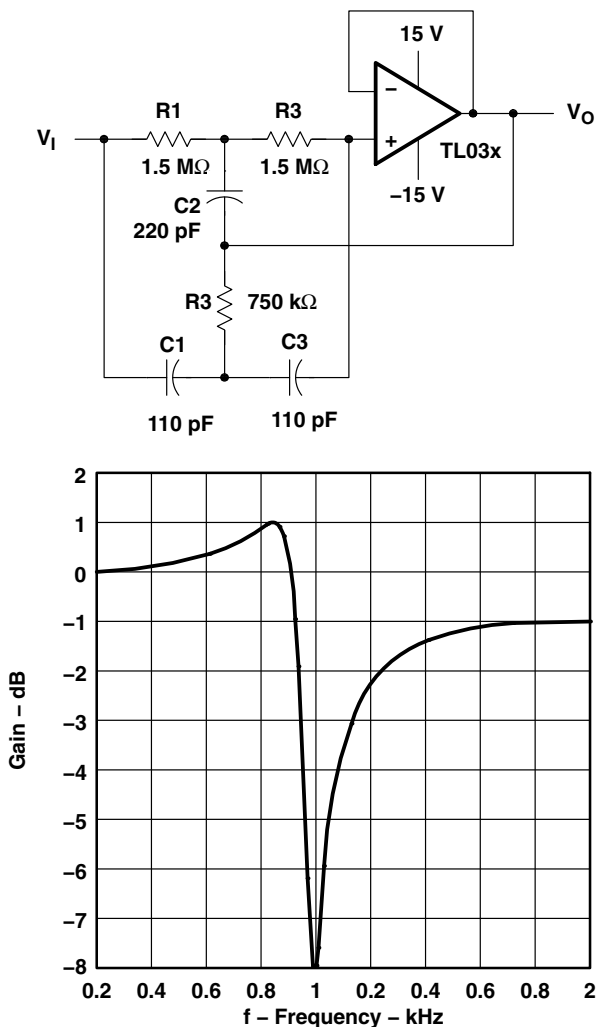
**APPLICATION INFORMATION**

**high-Q notch filter**

In general, Texas Instruments enhanced-JFET operational amplifiers serve as excellent filters. The circuit in Figure 64 provides a narrow notch at a specific frequency. Notch filters are designed to eliminate frequencies that are interfering with the operation of an application. For this filter, the center frequency can be calculated as:

$$f_0 = \frac{1}{2\pi \times R1 \times C1}$$

With the resistors and capacitors shown in Figure 64, the center frequency is 1 kHz.  $C1 = C3 = C2 + 2$  and  $R1 = R3 = 2 \times R2$ . The center frequency can be modified by varying these values. When adjusting the center frequency, ensure that the operational amplifier has sufficient gain at the frequency required.



**Figure 64. High-Q Notch Filter**

# TL03x, TL03xA ENHANCED-JFET LOW-POWER LOW-OFFSET OPERATIONAL AMPLIFIERS

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## APPLICATION INFORMATION

### transimpedance amplifier

The low-power precision TL03x allows accurate measurement of low currents. The high input impedance and low offset voltage of the TL03xA greatly simplify the design of a transimpedance amplifier. At room temperature, this design achieves 10-bit accuracy with an error of less than 1/2 LSB.

Assuming that R2 is much less than R1 and ignoring error terms, the output voltage can be expressed as:

$$V_O = -I_{IN} \times R_F \left( \frac{R_1 + R_2}{R_2} \right)$$

Using the resistor values shown in the schematic for a 1-nA input current, the output voltage equals -0.1 V. If the  $V_O$  limit for the TL03xA is measured at  $\pm 12$  V, the maximum input current for these resistor values is  $\pm 120$  nA. Similarly, one LSB on a 10-bit scale corresponds to 12 mV of output voltage, or 120 pA of input current.

The following equation shows the effect of input offset voltage and input bias current on the output voltage:

$$V_O = - \left[ V_{IO} + R_F (I_{IO} + I_{IB}) \right] \left( \frac{R_1 + R_2}{R_2} \right)$$

If the application requires input protection for the transimpedance amplifier, do not use standard PN diodes. Instead, use low-leakage Siliconix SN4117 JFETs (or equivalent) connected as diodes across the TL03xA inputs (see Figure 65).

As with all precision applications, special care must be taken to eliminate external sources of leakage and interference. Other precautions include using high-quality insulation, cleaning insulating surfaces to remove fluxes and other residue, and enclosing the application within a protective box.

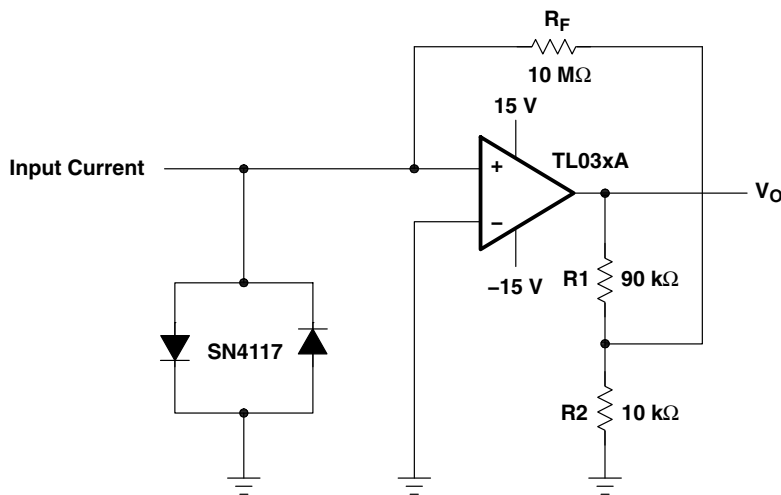


Figure 65. Transimpedance Amplifier

## APPLICATION INFORMATION

### 4-mA to 20-mA current loops

Often, information from an analog sensor must be sent over a distance to the receiving circuitry. For many applications, the most feasible method involves converting voltage information to a current before transmission. The following circuits give two variations of low-power current loops. The circuit in Figure 66 requires three wires from the transmitting to receiving circuitry, while the second variation in Figure 67 requires only two wires, but includes an extra integrated circuit. Both circuits benefit from the high input impedance of the TL03xA because many inexpensive sensors do not have low output impedance.

Assuming that the voltage at the noninverting input of the TL03xA is zero, the following equation determines the output current:

$$I_O = V_I \left( \frac{R_3}{R_1 \times R_S} \right) + 5V \left( \frac{R_3}{R_2 \times R_S} \right) = 0.16 \times V_I + 4\text{mA}$$

The circuits presently provide 4-mA to 20-mA output current for an input voltage of 0 to 100 mV. By modifying R1, R2, and R3, the input voltage range or the output current range can be adjusted.

Including the offset voltage of the operational amplifier in the above equation clearly illustrates why the low offset TL03xA was chosen:

$$\begin{aligned} I_O &= V_I \left( \frac{R_3}{R_1 \times R_S} \right) + 5V \left( \frac{R_3}{R_2 \times R_S} \right) - V_I \left( \frac{R_3}{R_1 \times R_S} + \frac{R_3}{R_2 \times R_S} + \frac{R_1}{R_S} \right) \\ &= 0.16 \times V_I + 4\text{mA} - 0.17 \times V_I \end{aligned}$$

For example, an offset voltage of 1 mV decreases the output current by 0.17 mA.

Due to the low power consumption of the TL03xA, both circuits have at least 2 mA available to drive the actual sensor from the 5-V reference node.

# TL03x, TL03xA ENHANCED-JFET LOW-POWER LOW-OFFSET OPERATIONAL AMPLIFIERS

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## APPLICATION INFORMATION

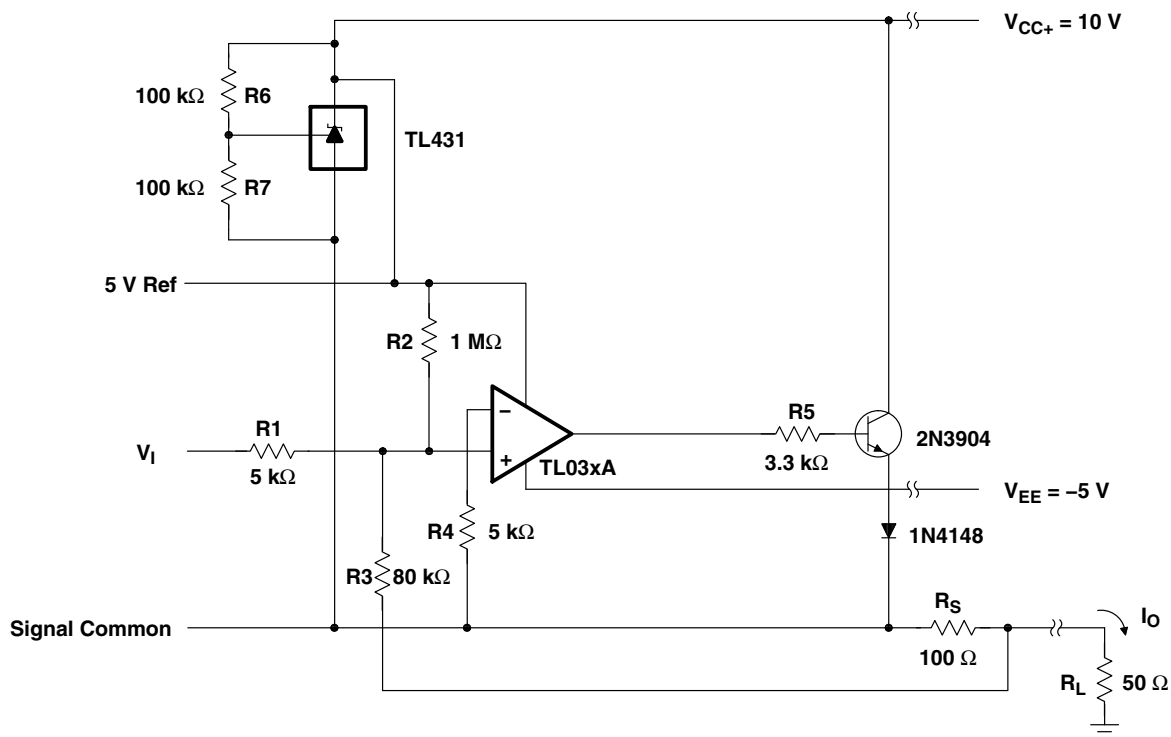


Figure 66. Three-Wire 4-mA to 20-mA Current Loop

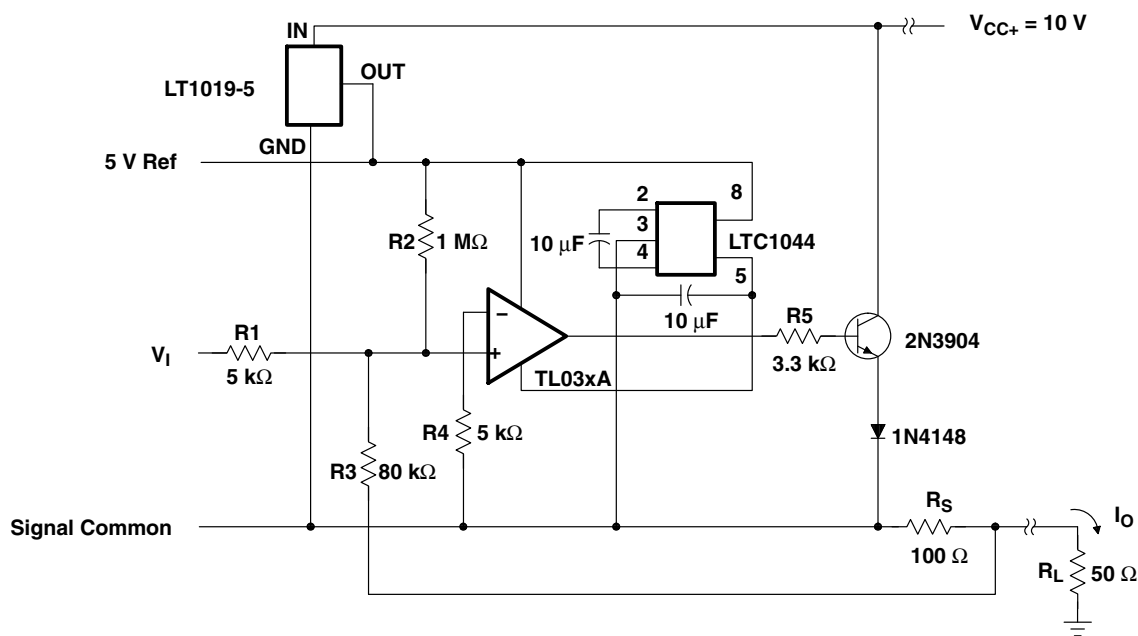


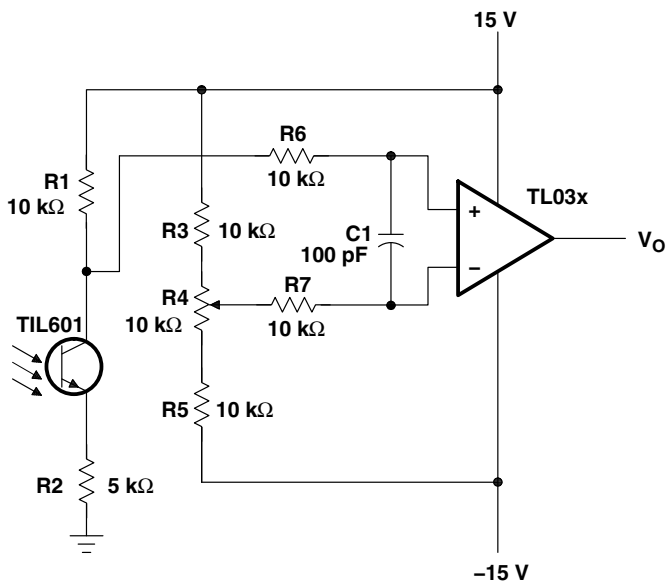
Figure 67. Two-Wire 4-mA to 20-mA Current Loop

## APPLICATION INFORMATION

### low-level light-detector preamplifier

Applications that need to detect small currents require high input-impedance operational amplifiers; otherwise, the bias currents of the operational amplifier camouflage the current being monitored. Phototransistors provide a current that is proportional to the light reaching the transistor. The TL03x allows even the small currents resulting from low-level light to be detected.

In Figure 68, if there is no light, the phototransistor is off and the output is high. As light is detected, the operational amplifier output begins pulling low. Adjusting R4 both compensates for offset voltage of the amplifier and adjusts the point of light detection by the amplifier.



**Figure 68. Low-Level Light-Detector Preamplifier**

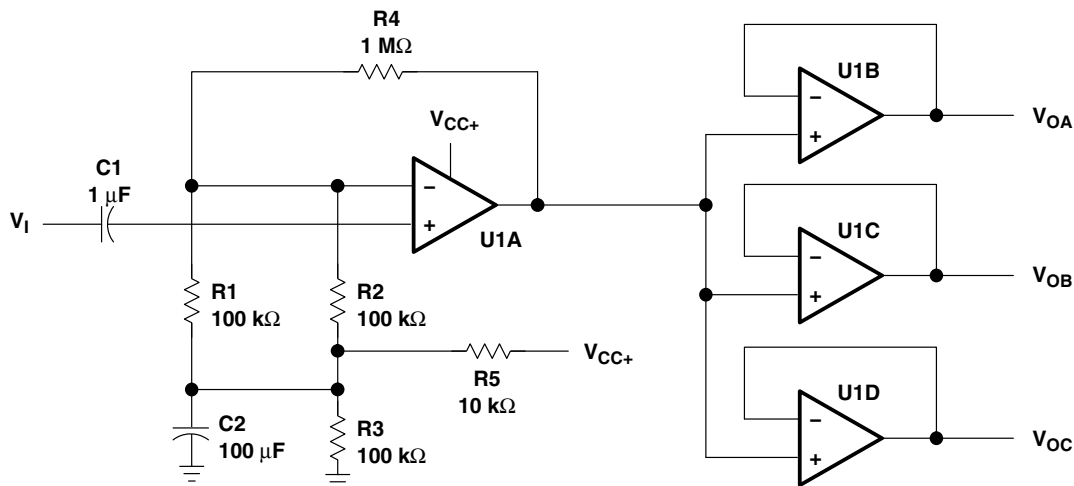
# TL03x, TL03xA ENHANCED-JFET LOW-POWER LOW-OFFSET OPERATIONAL AMPLIFIERS

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## APPLICATION INFORMATION

### audio-distribution amplifier

This audio-distribution amplifier (see Figure 69) feeds the input signal to three separate output channels. U1A amplifies the input signal with a gain of 10, while U1B, U1C, and U1D serve as buffers to the output channels. The gain response of this circuit is very flat from 20 Hz to 20 kHz. The TL03x allows quick response to the input signal while maintaining low power consumption.



NOTE A: U1A through U1D = TL03x;  $V_{CC+} = 5\text{ V}$

Figure 69. Audio-Distribution Amplifier Circuit



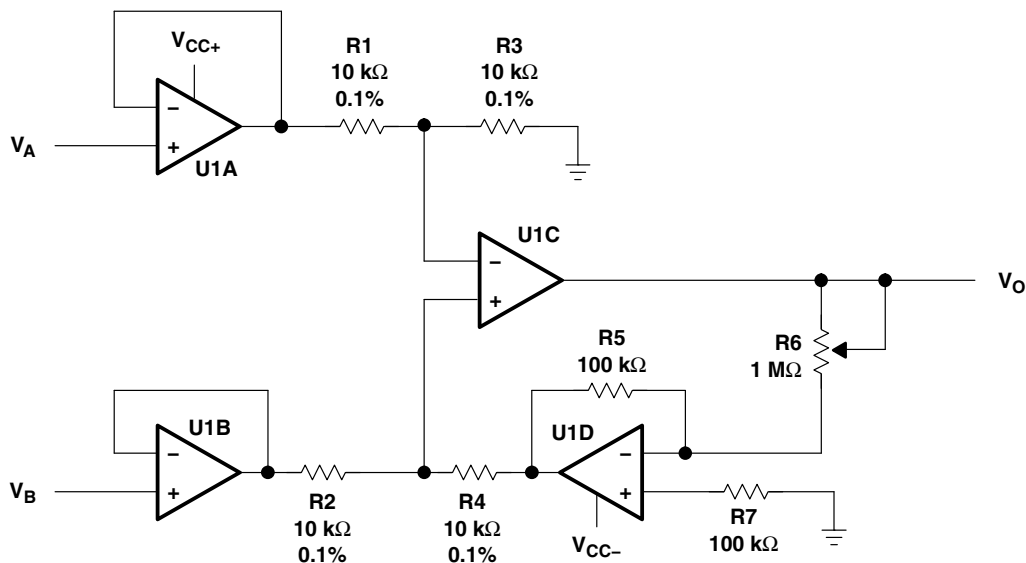
**APPLICATION INFORMATION**

**instrumentation amplifier with linear gain adjust**

The low offset voltage and low power consumption of the TL03x provide an accurate but inexpensive instrumentation amplifier (see Figure 70). This particular configuration offers the advantage that the gain can be linearly set by one resistor:

$$V_O = \frac{R_6}{R_5} \times (V_B - V_A)$$

Adjusting R6 varies the gain. The value of R6 always should be greater than, or equal to, the value of R5 to ensure stability. The disadvantage of this instrumentation amplifier topology is the high degree of CMRR degradation resulting from mismatches between R1, R2, R3, and R4. For this reason, these four resistors should be 0.1%-tolerance resistors.



NOTE A: U1A through U1D = TL03x;  $V_{CC\pm} = \pm 15$  V

**Figure 70. Instrumentation Amplifier With Linear Gain-Adjust Circuit**

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL031CD	Obsolete	Production	SOIC (D)   8	-	-	Call TI	Call TI	0 to 70	TL031C
TL031CDR	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL031C
TL031CP	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL031CP
TL031ID	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL031I
TL031IP	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL031IP
TL032ACD	Obsolete	Production	SOIC (D)   8	-	-	Call TI	Call TI	0 to 70	032AC
TL032ACDR	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	032AC
TL032ACP	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL032ACP
TL032AID	Obsolete	Production	SOIC (D)   8	-	-	Call TI	Call TI	-40 to 85	032AI
TL032AIDR	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	032AI
TL032AIP	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL032AIP
TL032CD	Obsolete	Production	SOIC (D)   8	-	-	Call TI	Call TI	0 to 70	TL032C
TL032CDR	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL032C
TL032CP	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL032CP
TL032CPSR	Active	Production	SO (PS)   8	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T032
TL032ID	Obsolete	Production	SOIC (D)   8	-	-	Call TI	Call TI	-40 to 85	TL032I
TL032IDR	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL032I
TL032IP	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL032IP
TL034ACD	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	0 to 70	TL034AC
TL034ACDR	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU   NIPDAU	Level-1-260C-UNLIM	0 to 70	TL034AC
TL034ACN	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL034ACN
TL034AID	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	-40 to 85	TL034AI
TL034AIDR	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU   NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL034AI
TL034AIN	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL034AIN
TL034CDR	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU   NIPDAU	Level-1-260C-UNLIM	0 to 70	TL034C
TL034CN	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL034CN
TL034CNSR	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL034
TL034CPW	Obsolete	Production	TSSOP (PW)   14	-	-	Call TI	Call TI	0 to 70	T034
TL034CPWR	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T034

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TL034ID</a>	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	-40 to 85	TL034I
<a href="#">TL034IDR</a>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU   NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL034I
<a href="#">TL034IN</a>	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL034IN

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



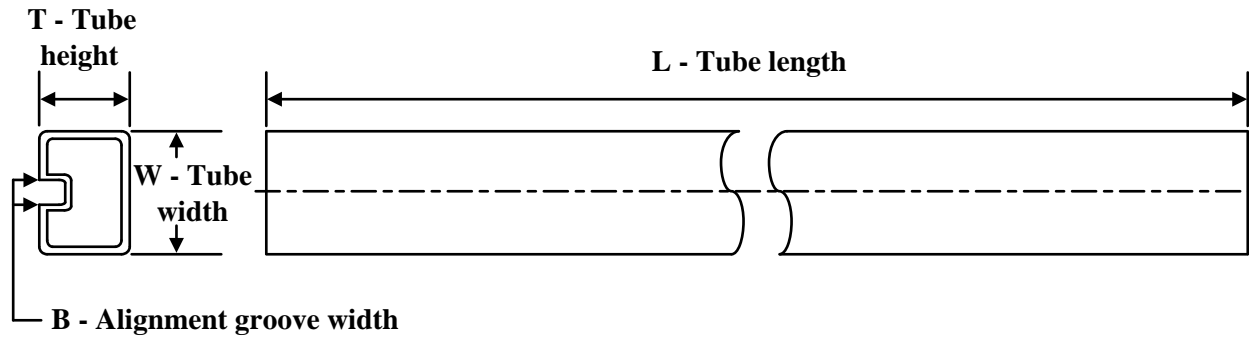
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL031CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL032ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL032AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL032CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL032CPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TL032IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL034ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL034ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL034AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL034CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL034CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL034CNSR	SOP	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TL034CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL034CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL034IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL034IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL031CDR	SOIC	D	8	2500	353.0	353.0	32.0
TL032ACDR	SOIC	D	8	2500	356.0	356.0	35.0
TL032AIDR	SOIC	D	8	2500	356.0	356.0	35.0
TL032CDR	SOIC	D	8	2500	356.0	356.0	35.0
TL032CPSR	SO	PS	8	2000	356.0	356.0	35.0
TL032IDR	SOIC	D	8	2500	353.0	353.0	32.0
TL034ACDR	SOIC	D	14	2500	356.0	356.0	35.0
TL034ACDR	SOIC	D	14	2500	353.0	353.0	32.0
TL034AIDR	SOIC	D	14	2500	356.0	356.0	35.0
TL034CDR	SOIC	D	14	2500	353.0	353.0	32.0
TL034CDR	SOIC	D	14	2500	356.0	356.0	35.0
TL034CNSR	SOP	NS	14	2000	356.0	356.0	35.0
TL034CPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TL034CPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TL034IDR	SOIC	D	14	2500	356.0	356.0	35.0
TL034IDR	SOIC	D	14	2500	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TL031CP	P	PDIP	8	50	506	13.97	11230	4.32
TL031ID	D	SOIC	8	75	507	8	3940	4.32
TL031IDG4	D	SOIC	8	75	507	8	3940	4.32
TL031IP	P	PDIP	8	50	506	13.97	11230	4.32
TL032ACP	P	PDIP	8	50	506	13.97	11230	4.32
TL032AIP	P	PDIP	8	50	506	13.97	11230	4.32
TL032CP	P	PDIP	8	50	506	13.97	11230	4.32
TL032IP	P	PDIP	8	50	506	13.97	11230	4.32
TL034ACN	N	PDIP	14	25	506	13.97	11230	4.32
TL034AIN	N	PDIP	14	25	506	13.97	11230	4.32
TL034CN	N	PDIP	14	25	506	13.97	11230	4.32
TL034IN	N	PDIP	14	25	506	13.97	11230	4.32

D0014A



# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



4040082/E 04/2010

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.



N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

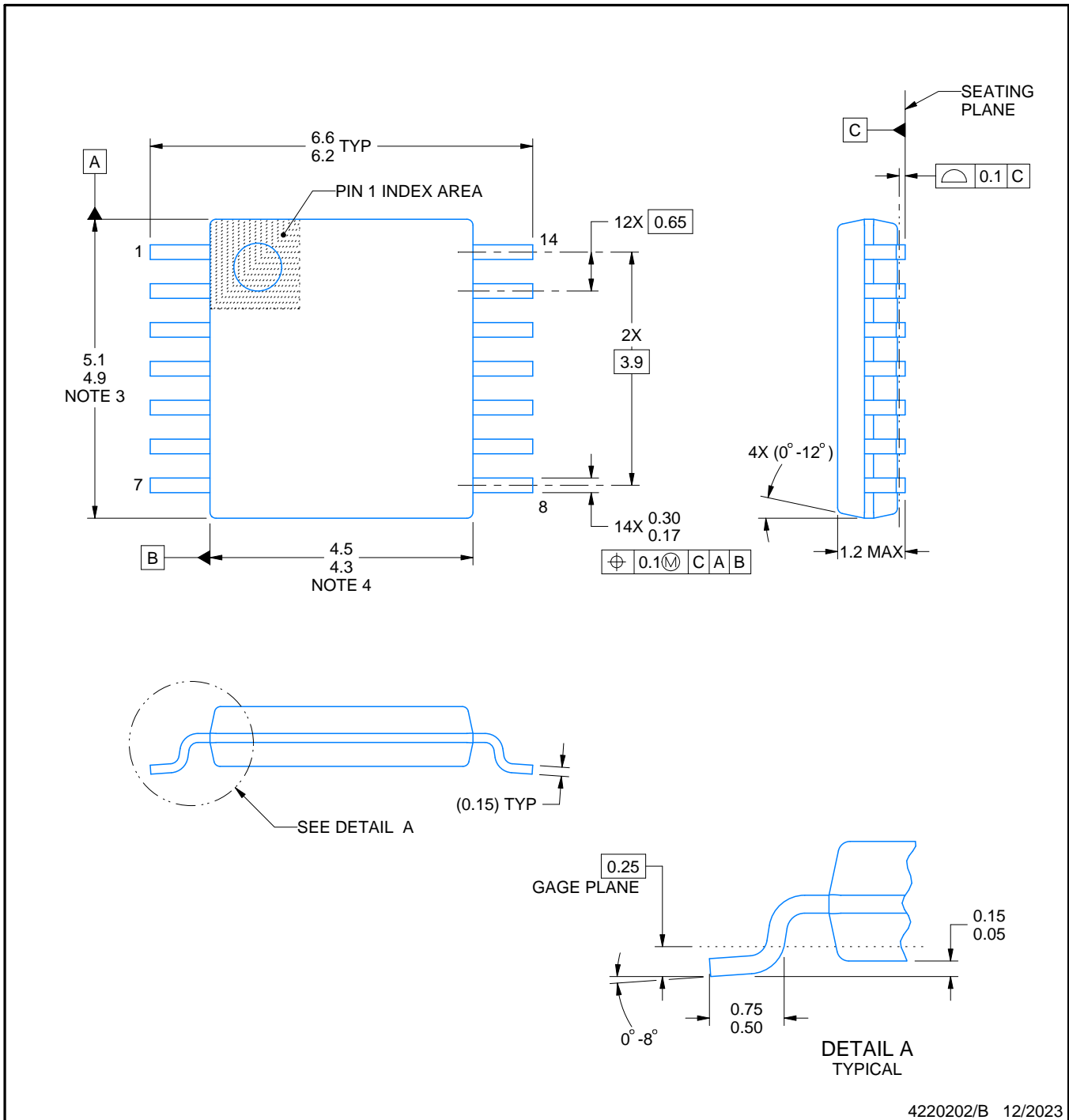
4040049/E 12/2002

PW0014A



**PACKAGE OUTLINE**  
**TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

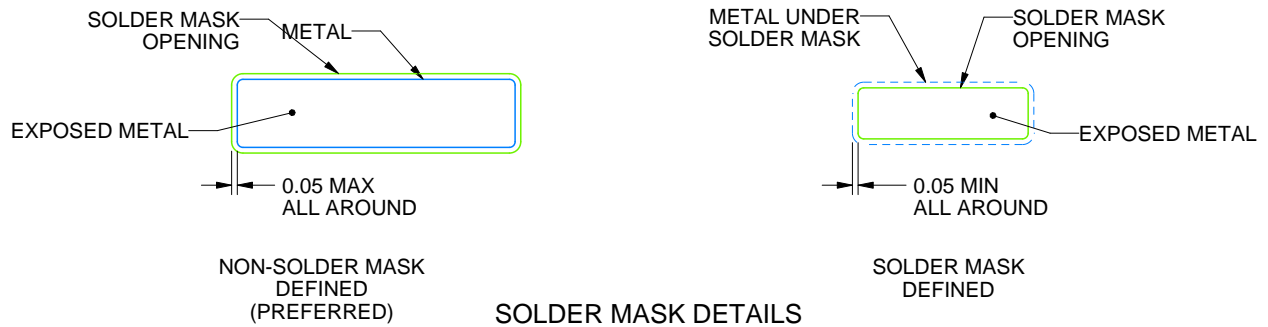
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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