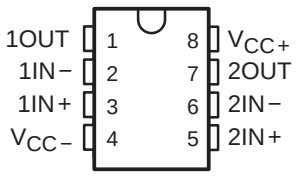
- **Wide Range of Supply Voltages; Single Supply . . . 3 V to 36 V, or Dual Supplies**
- **Class AB Output Stage**
- **High-Impedance N-Channel-JFET Input Stage . . . 10^{12} Ω Typ**
- **Internal Frequency Compensation**
- **Short-Circuit Protection**
- **Input Common Mode Includes V_{CC-}**
- **Low Input Offset Current . . . 50 pA**
- **Low Input Bias Current . . . 200 pA Typ**

PS PACKAGE
(TOP VIEW)



description

The TL092 JFET-input operational amplifier is similar in performance to the MC3403 family, but with much higher input impedance derived from a FET input stage. The N-channel-JFET input stage allows a common-mode input voltage range that includes the negative supply voltage and offers a typical input impedance of 10^{12} Ω, a typical input offset current of 50 pA, and a typical input bias current of 200 pA. This device is designed to operate from a single supply over a range of 3 V to 36 V. Operation from split supplies also is possible, provided the difference between the two supplies is 3 V to 36 V. Output voltage range is from V_{CC-} to V_{CC+} − 1.3 V, with a load resistor to V_{CC-}.

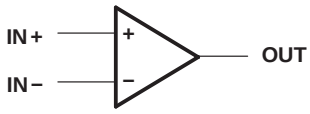
The TL092 is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

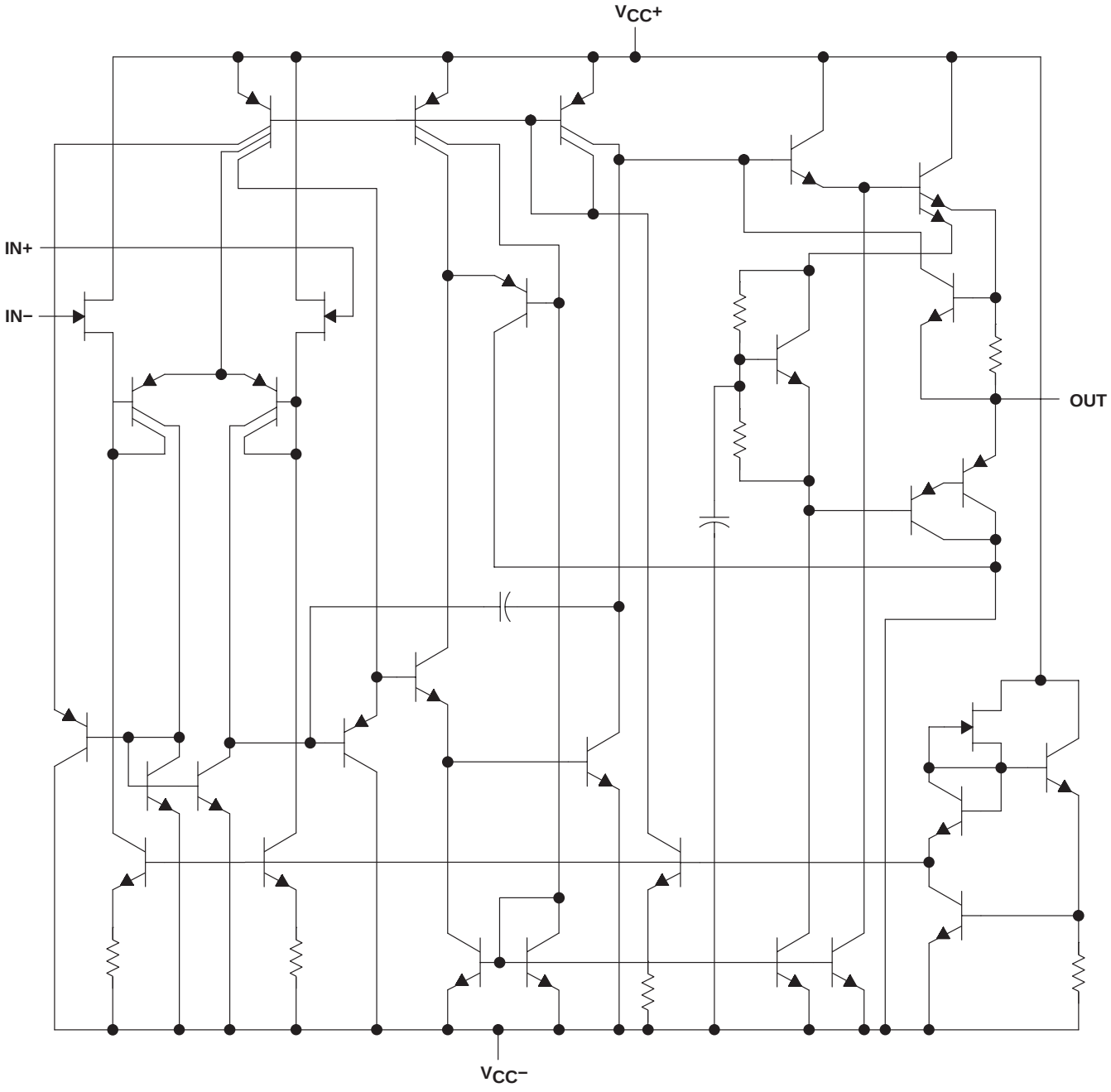
T_A	PACKAGED DEVICE
	PLASTIC SMALL OUTLINE (PS)
0°C to 70°C	TL092CPSR

The PS package is only available taped and reeled. Add the suffix R to device type for ordering (e.g., TL092CPSR).

symbol



schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage: V_{CC+} (see Note 1) . . . . . 18 V
V_{CC-} (see Note 1) . . . . . −18 V
V_{CC+} with respect to V_{CC-} . . . . . 36 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±36 V
Input voltage, V_I (see Notes 1 and 3) . . . . . ±18 V
Package thermal impedance, θ_{JA} (see Notes 4 and 5) . . . . . 95°C/W
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. Neither input must ever be more positive than V_{CC+} or more negative than V_{CC-} − 0.3 V.
4. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		MIN	MAX	UNIT
$V_{CC\pm}$	Supply voltage	3	36	V
T_A	Operating free-air temperature range	0	70	°C

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (all characteristics are specified under open-loop conditions, unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP†	MAX	UNIT
V_{IO}	Input offset voltage	R_S = 50 Ω		25°C		5	15	mV
				Full range			20	
αV_{IO}	Temperature coefficient of input offset voltage			25°C		10		µV/°C
I_{IO}‡	Input offset current			25°C		50	200	pA
				Full range			5	nA
I_{IB}‡	Input bias current			25°C		200	400	pA
				Full range			10	nA
V_{ICR}	Common-mode input voltage range			25°C	V_{CC-} to 12	V_{CC-} to 13		V
$V_{O(PP)}$	Peak output voltage swing	R_L = 2 kΩ		25°C	±10	±13		V
		R_L = 10 kΩ		25°C	±12	±13.5		
		R_L = 2 kΩ		Full range	±10			
A_{VD}	Large-signal differential voltage amplification	R_L = 2 kΩ,	V_O = ±10 V	25°C	20	200		V/mV
				Full range	15			
B_{OM}	Maximum output swing bandwidth	R_L = 2 kΩ, A_{VD} = 1,	$V_{O(PP)}$ = 20 V, THD < 5%	25°C		9		kHz
B_1	Unity gain bandwidth	R_L = 10 kΩ,	V_O = 50 mV	25°C		1		MHz
ϕ_m	Phase margin	R_L = 2 kΩ,	C_L = 200 pF	25°C		60°		
r_i	Input resistance	f = 20 Hz		25°C		10^{12}		Ω
r_o	Output resistance	f = 20 Hz		25°C		75		Ω
CMRR	Common-mode rejection ratio	R_S = 50 Ω,	V_{IC} = V_{ICR}	25°C	70	90		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	R_S = 50 Ω,	$V_{CC\pm}$ = ±3 V to ±15 V	25°C	75	90		dB
I_{OS}	Short-circuit output current			25°C		40		mA
I_{CC}	Supply current (per amplifier)	V_O = 0,	No load	25°C		1.5	2.5	mA

† All typical values are at T_A = 25°C.

‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques that maintain the junction temperature as close to the ambient temperature as possible must be used.

electrical characteristics at specified free-air temperature, V_{CC+} = 5 V, V_{CC-} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IO}	Input offset voltage	R_S = 50 Ω,	V_O = 2.5 V		5	15	mV
I_{IO}	Input offset current	V_O = 2.5 V			50	200	pA
I_{IB}	Input bias current	V_O = 2.5 V			200	400	pA
$V_{O(PP)}$	Peak output voltage swing	R_L = 10 kΩ		3.3	3.5		V
		R_L = 10 kΩ,	V_{CC+} = 5 V to 30 V	V_{CC+}−1.7			V
A_{VD}	Large-signal differential voltage amplification	R_L = 2 kΩ,	ΔV_O =1.6 V	20	200		V/mV
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	R_S = 50 Ω,	$V_{CC\pm}$ = ±3 V to ±15 V	75			dB
I_{CC}	Supply current (per amplifier)	V_O = 2.5 V,	No load		1.5	2.5	mA
V_{O1}/V_{O2}	Channel separation	f = 1 kHz to 20 kHz			120		dB

† All typical values are at T_A = 25°C.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_I = ±10 V (see Figure 1),	C_L = 100 pF,	R_L = 2 kΩ		0.6		V/μs
t_r	Rise time	ΔV_O = 50 mV (see Figure 1),	C_L = 100 pF,	R_L = 2 kΩ		0.2		μs
t_f	Fall time	ΔV_O = 50 mV (see Figure 1),	C_L = 100 pF,	R_L = 2 kΩ		0.2		μs
	Overshoot factor	ΔV_O = 50 mV (see Figure 1),	C_L = 100 pF,	R_L = 2 kΩ		20%		
	Crossover distortion	V_{IPP} = 30 mV, $V_{O(PP)}$ = 2 V,	f = 10 kHz			1%		
V_n	Equivalent input noise voltage	R_S = 100 Ω,	f = 1 kHz			34		nV/√Hz

PARAMETER MEASUREMENT INFORMATION

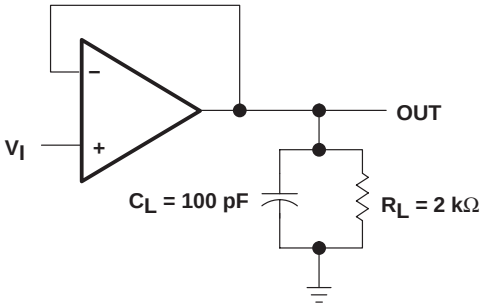


Figure 1. Unity-Gain Amplifier

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL092CPSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T092	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

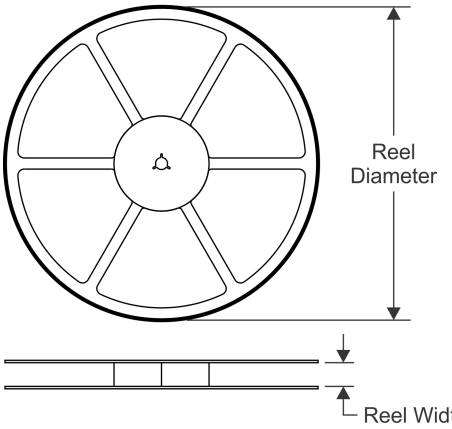
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

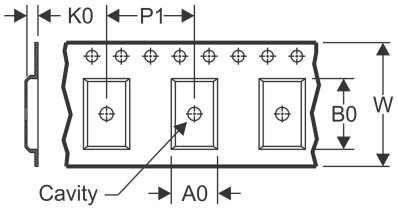
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

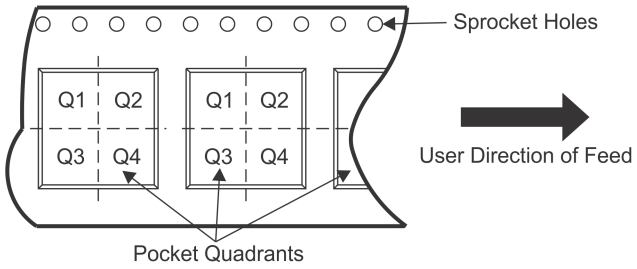


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

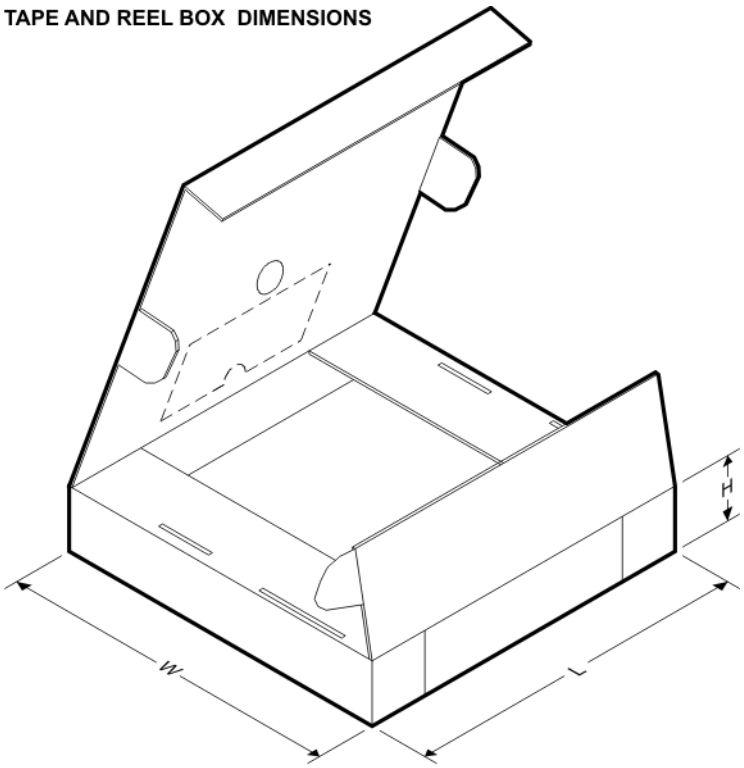
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL092CPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

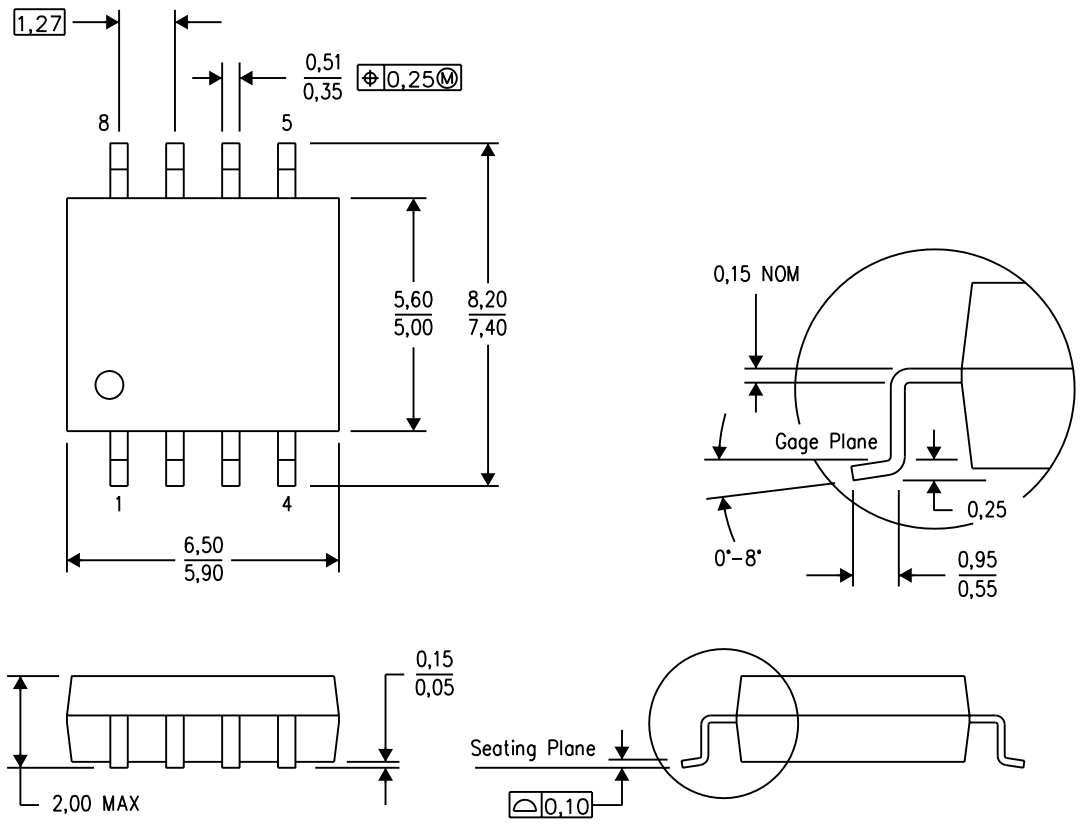


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL092CPSR	SO	PS	8	2000	853.0	449.0	35.0

MECHANICAL DATA

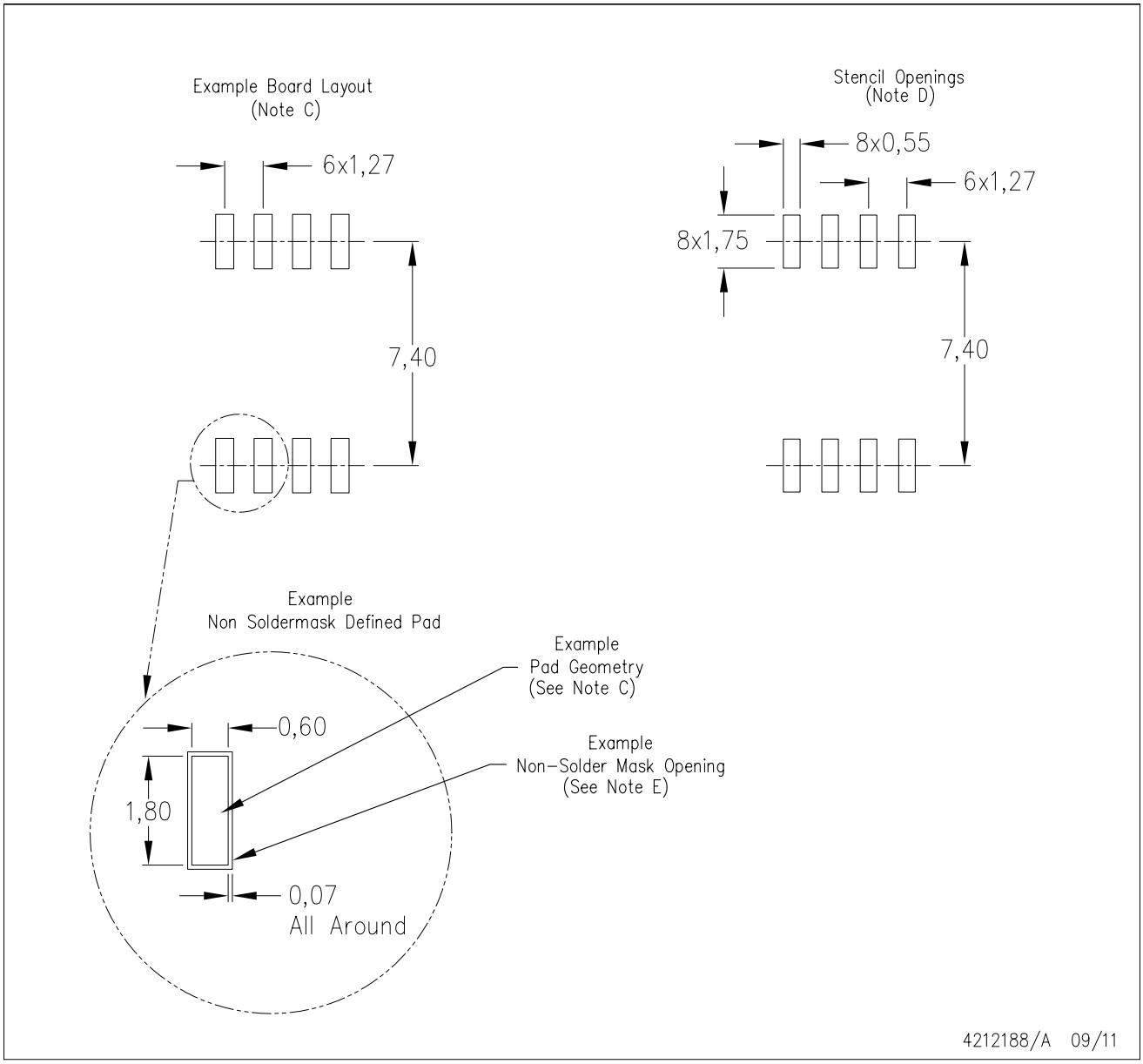
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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