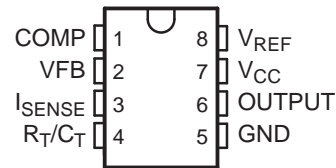


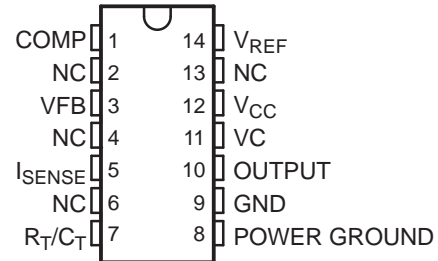
FEATURES

- **Low Start-Up Current (<0.5 mA)**
- **Trimmed Oscillator Discharge Current**
- **Current Mode Operation to 500 kHz**
- **Automatic Feed-Forward Compensation**
- **Latching PWM for Cycle-by-Cycle Current Limiting**
- **Internally Trimmed Reference With Undervoltage Lockout**
- **High-Current Totem-Pole Output Undervoltage Lockout With Hysteresis**
- **Double-Pulse Suppression**

**D (SOIC) OR P (PDIP) PACKAGE
(TOP VIEW)**



**D (SOIC) PACKAGE
(TOP VIEW)**



NC – No internal connection

DESCRIPTION/ORDERING INFORMATION

The TL284xB and TL384xB series of control integrated circuits provide the features that are necessary to implement off-line or dc-to-dc fixed-frequency current-mode control schemes, with a minimum number of external components. Internally implemented circuits include an undervoltage lockout (UVLO) and a precision reference that is trimmed for accuracy at the error amplifier input. Other internal circuits include logic to ensure latched operation, a pulse-width modulation (PWM) comparator that also provides current-limit control, and a totem-pole output stage designed to source or sink high-peak current. The output stage, suitable for driving N-channel MOSFETs, is low when it is in the off state.

The TL284xB and TL384xB series are pin compatible with the standard TL284x and TL384x with the following improvements. The start-up current is specified to be 0.5 mA (max), while the oscillator discharge current is trimmed to 8.3 mA (typ). In addition, during undervoltage lockout conditions, the output has a maximum saturation voltage of 1.2 V while sinking 10 mA ($V_{CC} = 5$ V).

Major differences between members of these series are the UVLO thresholds and maximum duty-cycle ranges. Typical UVLO thresholds of 16 V (on) and 10 V (off) on the TLx842B and TLx844B devices make them ideally suited to off-line applications. The corresponding typical thresholds for the TLx843B and TLx845B devices are 8.4 V (on) and 7.6 V (off). The TLx842B and TLx843B devices can operate to duty cycles approaching 100%. A duty-cycle range of 0% to 50% is obtained by the TLx844B and TLx845B by the addition of an internal toggle flip-flop, which blanks the output off every other clock cycle. The TL284xB-series devices are characterized for operation from -40°C to 85°C . The TL384xB-series devices are characterized for operation from 0°C to 70°C .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TL284xB, TL384xB HIGH-PERFORMANCE CURRENT-MODE PWM CONTROLLERS

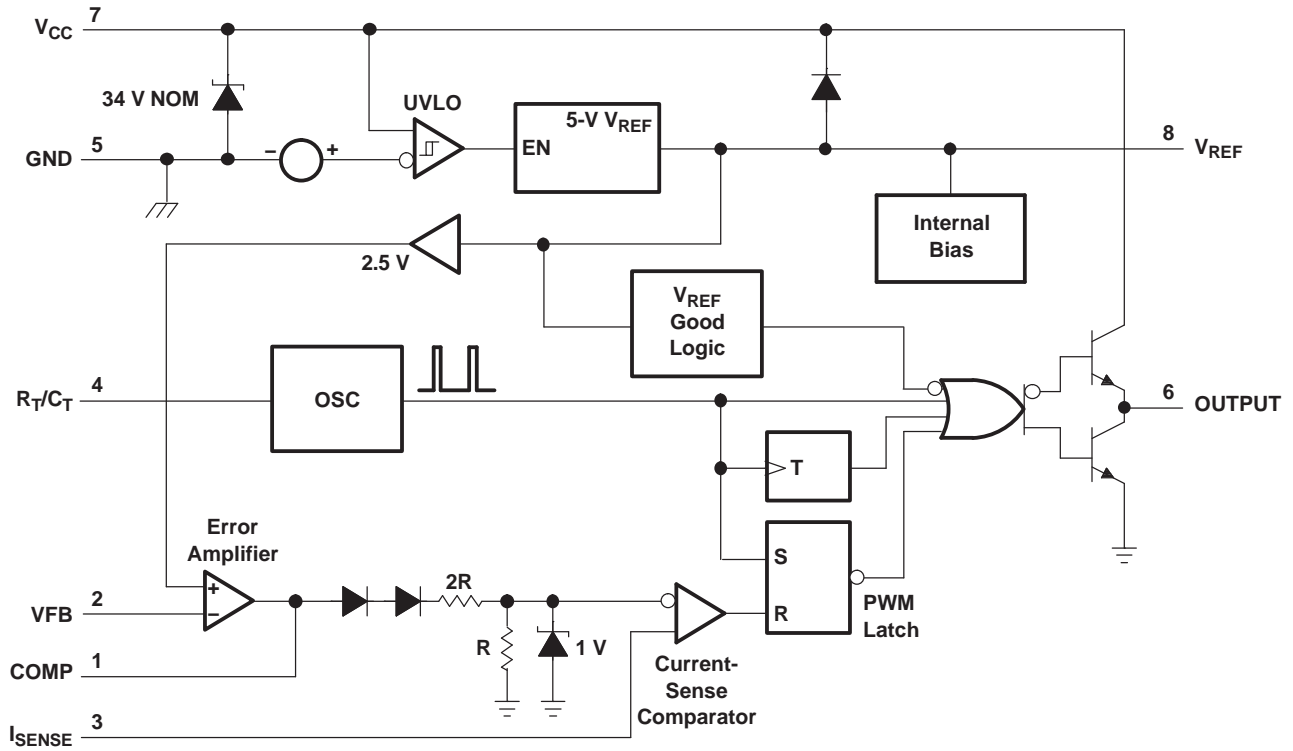
SLVS610B – AUGUST 2006 – REVISED JULY 2007

ORDERING INFORMATION

| T _A | PACKAGE ⁽¹⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------------------|--------------|-----------------------|------------------|
| -40°C to 85°C | PDIP – P | Tube of 50 | TL2842BP | TL2842BP |
| | | | TL2843BP | TL2843BP |
| | | | TL2844BP | TL2844BP |
| | | | TL2845BP | TL2845BP |
| | SOIC – D (8 pin) | Tube of 75 | TL2842BD-8 | 2842B |
| | | Reel of 2500 | TL2842BDR-8 | |
| | | Tube of 75 | TL2843BD-8 | 2843B |
| | | Reel of 2500 | TL2843BDR-8 | |
| | | Tube of 75 | TL2844BD-8 | 2844B |
| | | Reel of 2500 | TL2844BDR-8 | |
| | | Tube of 75 | TL2845BD-8 | 2845B |
| | | Reel of 2500 | TL2845BDR-8 | |
| | SOIC – D (14 pin) | Tube of 75 | TL2842BD | TL2842B |
| | | Reel of 2500 | TL2842BDR | |
| | | Tube of 75 | TL2843BD | TL2843B |
| | | Reel of 2500 | TL2843BDR | |
| Tube of 75 | | TL2844BD | TL2844B | |
| Reel of 2500 | | TL2844BDR | | |
| Tube of 75 | | TL2845BD | TL2845B | |
| Reel of 2500 | | TL2845BDR | | |
| 0°C to 70°C | PDIP – P | Tube of 50 | TL3842BP | TL3842BP |
| | | | TL3843BP | TL3843BP |
| | | | TL3844BP | TL3844BP |
| | | | TL3845BP | TL3845BP |
| | SOIC – D (8 pin) | Tube of 75 | TL3842BD-8 | 3842B |
| | | Reel of 2500 | TL3842BDR-8 | |
| | | Tube of 75 | TL3843BD-8 | 3843B |
| | | Reel of 2500 | TL3843BDR-8 | |
| | | Tube of 75 | TL3844BD-8 | 3844B |
| | | Reel of 2500 | TL3844BDR-8 | |
| | | Tube of 75 | TL3845BD-8 | 3845B |
| | | Reel of 2500 | TL3845BDR-8 | |
| | SOIC – D (14 pin) | Tube of 75 | TL3842BD | TL3842B |
| | | Reel of 2500 | TL3842BDR | |
| | | Tube of 75 | TL3843BD | TL3843B |
| | | Reel of 2500 | TL3843BDR | |
| Tube of 75 | | TL3844BD | TL3844B | |
| Reel of 2500 | | TL3844BDR | | |
| Tube of 75 | | TL3845BD | TL3845B | |
| Reel of 2500 | | TL3845BDR | | |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTIONAL BLOCK DIAGRAM



A. Pin numbers shown are for the 8-pin D package.

TL284xB, TL384xB HIGH-PERFORMANCE CURRENT-MODE PWM CONTROLLERS

SLVS610B – AUGUST 2006 – REVISED JULY 2007

Absolute Maximum Ratings⁽¹⁾⁽²⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT | |
|----------------------|---|----------------------------|---------------|------|------|
| V _{CC} | Supply voltage | Low impedance source | 30 | V | |
| | | I _{CC} < 30 mA | Self limiting | | |
| V _I | Analog input voltage range | VFB and I _{SENSE} | -0.3 | 6.3 | V |
| I _{CC} | Supply current | | 30 | mA | |
| I _O | Output current | | ±1 | A | |
| I _{O(sink)} | Error amplifier output sink current | | 10 | mA | |
| θ _{JA} | Package thermal impedance ⁽³⁾⁽⁴⁾ | D package | 8 pin | 97 | °C/W |
| | | | 14 pin | 86 | |
| | | P package | 85 | | |
| | Output energy | Capacitive load | 5 | μJ | |
| T _J | Virtual junction temperature | | 150 | °C | |
| T _{stg} | Storage temperature range | | -65 | 150 | °C |
| T _{lead} | Lead temperature | Soldering, 10 s | 300 | °C | |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to the device GND terminal.
- (3) Maximum power dissipation is a function of T_{J(max)}, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is P_D = (T_{J(max)} - T_A)/θ_{JA}. Operating at the absolute maximum T_J of 150°C can impact reliability.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|---------------------|------------------------------------|--------------------------------|------|-----|------|
| V _{CC} | Supply voltage | V _{CC} | | 30 | V |
| | | VC ⁽¹⁾ | | 30 | |
| V _I | Input voltage | R _T /C _T | 0 | 5.5 | V |
| | | VFB and I _{SENSE} | 0 | 5.5 | |
| V _O | Output voltage | OUTPUT | 0 | 30 | V |
| | | POWER GROUND ⁽¹⁾ | -0.1 | 1 | |
| I _{CC} | Supply current, externally limited | | | 25 | mA |
| I _O | Average output current | | | 200 | mA |
| I _{O(ref)} | Reference output current | | | -20 | mA |
| f _{osc} | Oscillator frequency | | 100 | 500 | kHz |
| T _J | Operating free-air temperature | TL284xB | -40 | 85 | °C |
| | | TL384xB | 0 | 70 | |

- (1) The recommended voltages for VC and POWER GROUND apply only to the 14-pin D package.

Reference Section Electrical Characteristics
 $V_{CC} = 15\text{ V}^{(1)}$, $R_T = 10\text{ k}\Omega$, $C_T = 3.3\text{ nF}$, over recommended operating free-air temperature range (unless otherwise specified)

| PARAMETER | TEST CONDITIONS | TL284xB | | | TL384xB | | | UNIT |
|---|--|---------|--------------------|------|---------|--------------------|------|----------------------|
| | | MIN | TYP ⁽²⁾ | MAX | MIN | TYP ⁽²⁾ | MAX | |
| Output voltage | $I_O = 1\text{ mA}$, $T_J = 25^\circ\text{C}$ | 4.95 | 5 | 5.05 | 4.9 | 5 | 5.1 | V |
| Line regulation | $V_{CC} = 12\text{ V}$ to 25 V | | 6 | 20 | | 6 | 20 | mV |
| Load regulation | $I_O = 1\text{ mA}$ to 20 mA | | 6 | 25 | | 6 | 25 | mV |
| Average temperature coefficient of output voltage | | | 0.2 | 0.4 | | 0.2 | 0.4 | mV/ $^\circ\text{C}$ |
| Output voltage, worst-case variation | $V_{CC} = 12\text{ V}$ to 25 V , $I_O = 1\text{ mA}$ to 20 mA | 4.9 | | 5.1 | 4.82 | | 5.18 | V |
| Output noise voltage | $f = 10\text{ Hz}$ to 10 kHz , $T_J = 25^\circ\text{C}$ | | 50 | | | 50 | | μV |
| Output-voltage long-term drift | After 1000 h at $T_J = 25^\circ\text{C}$ | | 5 | 25 | | 5 | 25 | mV |
| Short-circuit output current | | -30 | -100 | -180 | -30 | -100 | -180 | mA |

 (1) Adjust V_{CC} above the start threshold before setting it to 15 V.

 (2) All typical values are at $T_J = 25^\circ\text{C}$.

Oscillator Section⁽¹⁾ Electrical Characteristics
 $V_{CC} = 15\text{ V}^{(2)}$, $R_T = 10\text{ k}\Omega$, $C_T = 3.3\text{ nF}$, over recommended operating free-air temperature range (unless otherwise specified)

| PARAMETER | TEST CONDITIONS | TL284xB | | | TL384xB | | | UNIT |
|-----------------------|--|---------|--------------------|-----|---------|--------------------|-----|------|
| | | MIN | TYP ⁽³⁾ | MAX | MIN | TYP ⁽³⁾ | MAX | |
| Initial accuracy | $T_J = 25^\circ\text{C}$ | 49 | 52 | 55 | 49 | 52 | 55 | kHz |
| | $T_A = T_{low}$ to T_{high} | | 48 | 56 | | 48 | 56 | |
| | $T_J = 25^\circ\text{C}$, $R_T = 6.2\text{ k}\Omega$, $C_T = 1\text{ nF}$ | 225 | 250 | 275 | 225 | 250 | 275 | |
| Voltage stability | $V_{CC} = 12\text{ V}$ to 25 V | | 0.2 | 1 | | 0.2 | 1 | % |
| Temperature stability | | | 5 | | | 5 | | % |
| Amplitude | Peak to peak | | 1.7 | | | 1.7 | | V |
| Discharge current | $T_J = 25^\circ\text{C}$, $R_T/C_T = 2\text{ V}$ | 7.8 | 8.3 | 8.8 | 7.8 | 8.3 | 8.8 | mA |
| | $R_T/C_T = 2\text{ V}$ | | 7.5 | 8.8 | | 7.6 | 8.8 | |

(1) Output frequency equals oscillator frequency for the TL3842B and TL3843B. Output frequency is one-half the oscillator frequency for the TL3844B and TL3845B.

 (2) Adjust V_{CC} above the start threshold before setting it to 15 V.

 (3) All typical values are at $T_J = 25^\circ\text{C}$.

Error-Amplifier Section Electrical Characteristics

$V_{CC} = 15\text{ V}^{(1)}$, $R_T = 10\text{ k}\Omega$, $C_T = 3.3\text{ nF}$, over recommended operating free-air temperature range (unless otherwise specified)

| PARAMETER | TEST CONDITIONS | TL284xB | | | TL384xB | | | UNIT |
|---------------------------------|--|---------|--------------------|------|---------|--------------------|------|---------------|
| | | MIN | TYP ⁽²⁾ | MAX | MIN | TYP ⁽²⁾ | MAX | |
| Feedback input voltage | COMP = 2.5 V | 2.45 | 2.5 | 2.55 | 2.42 | 2.5 | 2.58 | V |
| Input bias current | | | -0.3 | -1 | | -0.3 | -2 | μA |
| Open-loop voltage amplification | $V_O = 2\text{ V to }4\text{ V}$ | 65 | 90 | | 65 | 90 | | dB |
| Gain-bandwidth product | | 0.7 | 1 | | 0.7 | 1 | | MHz |
| Supply-voltage rejection ratio | $V_{CC} = 12\text{ V to }25\text{ V}$ | 60 | 70 | | 60 | 70 | | dB |
| Output sink current | VFB = 2.7 V, COMP = 1.1 V | 2 | 6 | | 2 | 6 | | mA |
| Output source current | VFB = 2.3 V, COMP = 5 V | -0.5 | -0.8 | | -0.5 | -0.8 | | mA |
| High-level output voltage | VFB = 2.3 V, $R_L = 15\text{ k}\Omega$ to GND | 5 | 6 | | 5 | 6 | | V |
| Low-level output voltage | VFB = 2.7 V, $R_L = 15\text{ k}\Omega$ to GND | | 0.7 | 1.1 | | 0.7 | 1.1 | V |

(1) Adjust V_{CC} above the start threshold before setting it to 15 V.

(2) All typical values are at $T_J = 25^\circ\text{C}$.

Current-Sense Section Electrical Characteristics

$V_{CC} = 15\text{ V}^{(1)}$, $R_T = 10\text{ k}\Omega$, $C_T = 3.3\text{ nF}$, over recommended operating free-air temperature range (unless otherwise specified)

| PARAMETER | TEST CONDITIONS | TL284xB | | | TL384xB | | | UNIT |
|---|---------------------------------------|---------|--------------------|------|---------|--------------------|------|---------------|
| | | MIN | TYP ⁽²⁾ | MAX | MIN | TYP ⁽²⁾ | MAX | |
| Voltage amplification ⁽³⁾⁽⁴⁾ | | 2.85 | 3 | 3.15 | 2.85 | 3 | 3.15 | V/V |
| Current-sense comparator threshold ⁽³⁾ | COMP = 5 V | 0.9 | 1 | 1.1 | 0.9 | 1 | 1.1 | V |
| Supply-voltage rejection ratio ⁽³⁾ | $V_{CC} = 12\text{ V to }25\text{ V}$ | | 70 | | | 70 | | dB |
| Input bias current | | | -2 | -10 | | -2 | -10 | μA |
| Delay time to output | VFB = 0 V to 2 V | | 150 | 300 | | 150 | 300 | ns |

(1) Adjust V_{CC} above the start threshold before setting it to 15 V.

(2) All typical values are at $T_J = 25^\circ\text{C}$.

(3) Measured at the trip point of the latch, with VFB at 0 V.

(4) Measured between I_{SENSE} and COMP, with the input changing from 0 V to 0.8 V.

Output Section Electrical Characteristics

$V_{CC} = 15\text{ V}^{(1)}$, $R_T = 10\text{ k}\Omega$, $C_T = 3.3\text{ nF}$, over recommended operating free-air temperature range (unless otherwise specified)

| PARAMETER | TEST CONDITIONS | TL284xB | | | TL384xB | | | UNIT |
|---------------------------|--|---------|--------------------|-----|---------|--------------------|-----|------|
| | | MIN | TYP ⁽²⁾ | MAX | MIN | TYP ⁽²⁾ | MAX | |
| High-level output voltage | $I_{OH} = -20\text{ mA}$ | 13 | 13.5 | | 13 | 13.5 | | V |
| | $I_{OH} = -200\text{ mA}$ | 12 | 13.5 | | 12 | 13.5 | | |
| Low-level output voltage | $I_{OL} = 20\text{ mA}$ | | 0.1 | 0.4 | | 0.1 | 0.4 | V |
| | $I_{OL} = 200\text{ mA}$ | | 1.5 | 2.2 | | 1.5 | 2.2 | |
| Rise time | $C_L = 1\text{ nF}$, $T_J = 25^\circ\text{C}$ | | 50 | 150 | | 50 | 150 | ns |
| Fall time | $C_L = 1\text{ nF}$, $T_J = 25^\circ\text{C}$ | | 50 | 150 | | 50 | 150 | ns |
| UVLO saturation | $V_{CC} = 5\text{ V}$, $I_{OL} = 1\text{ mA}$ | | 0.7 | 1.2 | | 0.7 | 1.2 | V |

- (1) Adjust V_{CC} above the start threshold before setting it to 15 V.
 (2) All typical values are at $T_J = 25^\circ\text{C}$.

Undervoltage-Lockout Section Electrical Characteristics

$V_{CC} = 15\text{ V}^{(1)}$, $R_T = 10\text{ k}\Omega$, $C_T = 3.3\text{ nF}$, over recommended operating free-air temperature range (unless otherwise specified)

| PARAMETER | TEST CONDITIONS | TL284xB | | | TL384xB | | | UNIT |
|--|------------------|---------|--------------------|-----|---------|--------------------|------|------|
| | | MIN | TYP ⁽²⁾ | MAX | MIN | TYP ⁽²⁾ | MAX | |
| Start threshold voltage | TLx842B, TLx844B | 15 | 16 | 17 | 14.5 | 16 | 17.5 | V |
| | TLx843B, TLx845B | 7.8 | 8.4 | 9 | 7.8 | 8.4 | 9 | |
| Minimum operating voltage after start-up | TLx842B, TLx844B | 9 | 10 | 11 | 8.5 | 10 | 11.5 | V |
| | TLx843B, TLx845B | 7 | 7.6 | 8.2 | 7 | 7.6 | 8.2 | |

- (1) Adjust V_{CC} above the start threshold before setting it to 15 V.
 (2) All typical values are at $T_J = 25^\circ\text{C}$.

Pulse-Width Modulator Section Electrical Characteristics

$V_{CC} = 15\text{ V}^{(1)}$, $R_T = 10\text{ k}\Omega$, $C_T = 3.3\text{ nF}$, over recommended operating free-air temperature range (unless otherwise specified)

| PARAMETER | TEST CONDITIONS | TL284xB | | | TL384xB | | | UNIT |
|--------------------|------------------|---------|--------------------|-----|---------|--------------------|-----|------|
| | | MIN | TYP ⁽²⁾ | MAX | MIN | TYP ⁽²⁾ | MAX | |
| Maximum duty cycle | TL3842B, TL3843B | 94 | 96 | 100 | 94 | 96 | 100 | % |
| | TL3844B, TL3845B | 47 | 48 | 50 | 47 | 48 | 50 | |
| Minimum duty cycle | | | | 0 | | | 0 | % |

- (1) Adjust V_{CC} above the start threshold before setting it to 15 V.
 (2) All typical values are at $T_J = 25^\circ\text{C}$.

Supply Voltage Electrical Characteristics

$V_{CC} = 15\text{ V}^{(1)}$, $R_T = 10\text{ k}\Omega$, $C_T = 3.3\text{ nF}$, over recommended operating free-air temperature range (unless otherwise specified)

| PARAMETER | TEST CONDITIONS | TL284xB | | | TL384xB | | | UNIT |
|--------------------------|----------------------------|---------|--------------------|-----|---------|--------------------|-----|------|
| | | MIN | TYP ⁽²⁾ | MAX | MIN | TYP ⁽²⁾ | MAX | |
| Start-up current | | | 0.3 | 0.5 | | 0.3 | 0.5 | mA |
| Operating supply current | VFB and I_{SENSE} at 0 V | | 11 | 17 | | 11 | 17 | mA |
| Limiting voltage | $I_{CC} = 25\text{ mA}$ | | 30 | 34 | | 30 | 34 | V |

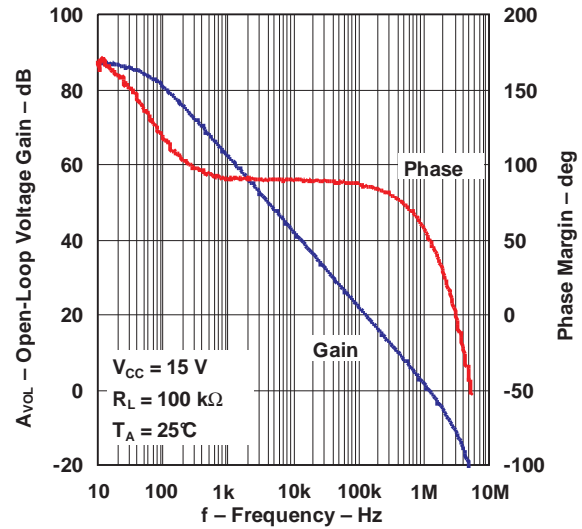
- (1) Adjust V_{CC} above the start threshold before setting it to 15 V.
 (2) All typical values are at $T_J = 25^\circ\text{C}$.

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
 VS
 SUPPLY VOLTAGE



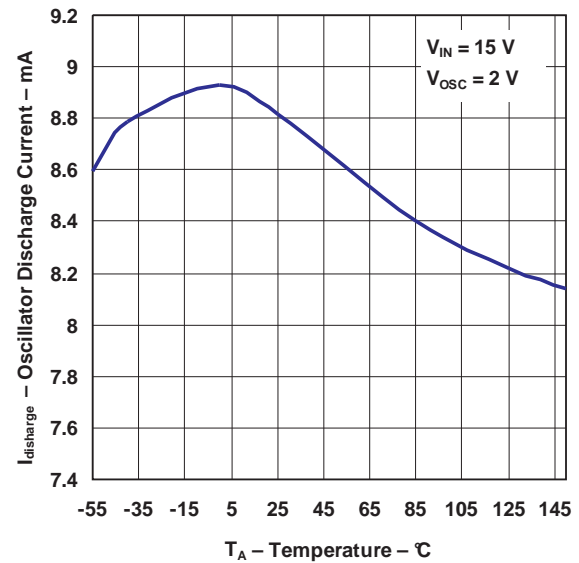
ERROR AMPLIFIER OPEN-LOOP
 GAIN AND PHASE
 VS
 FREQUENCY



CURRENT-SENSE INPUT THRESHOLD
 VS
 ERROR AMPLIFIER OUTPUT VOLTAGE

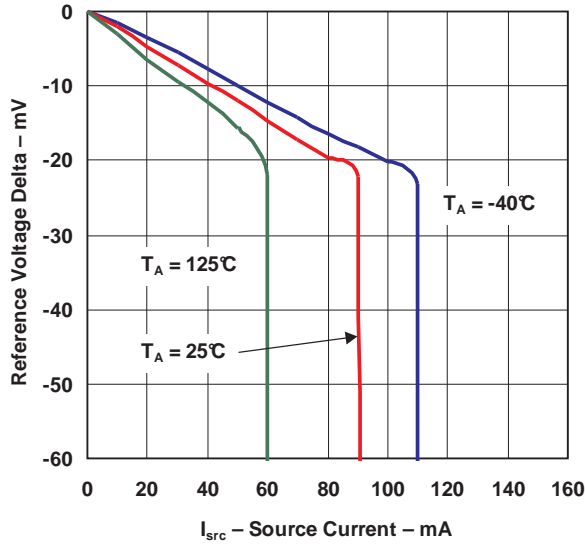


OSCILLATOR DISCHARGE CURRENT
 VS
 TEMPERATURE

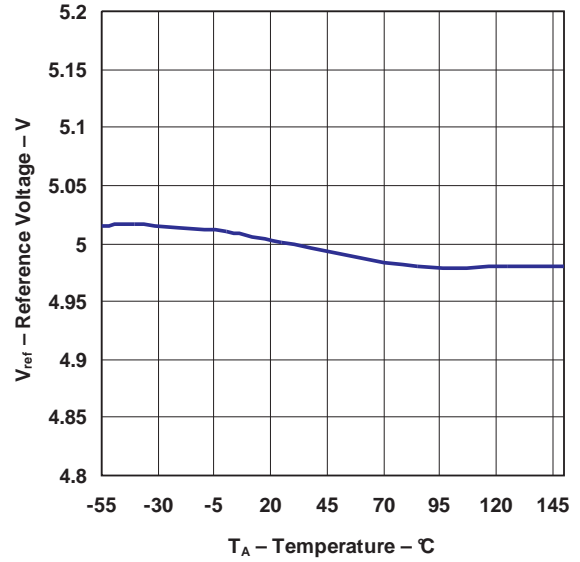


TYPICAL CHARACTERISTICS (continued)

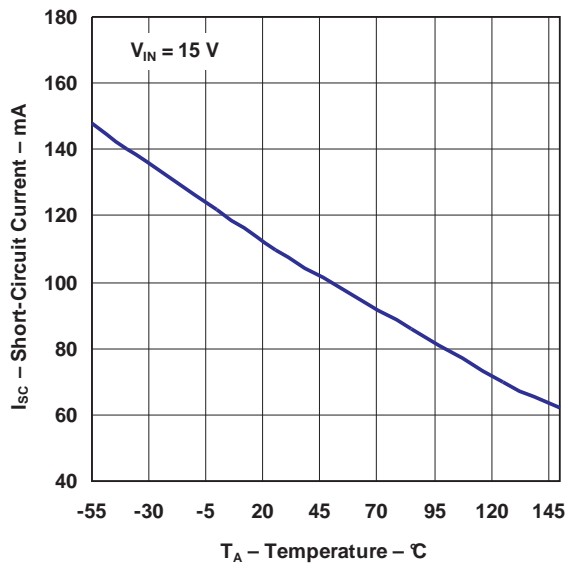
REFERENCE VOLTAGE
VS
SOURCE CURRENT



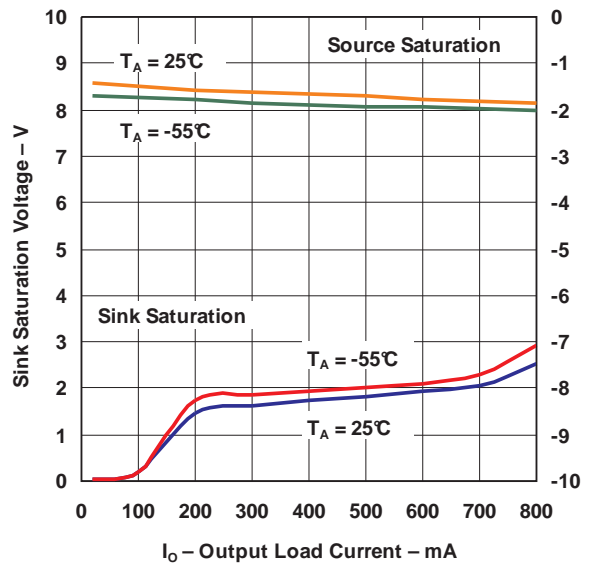
REFERENCE VOLTAGE
VS
TEMPERATURE



REFERENCE SHORT-CIRCUIT CURRENT
VS
TEMPERATURE

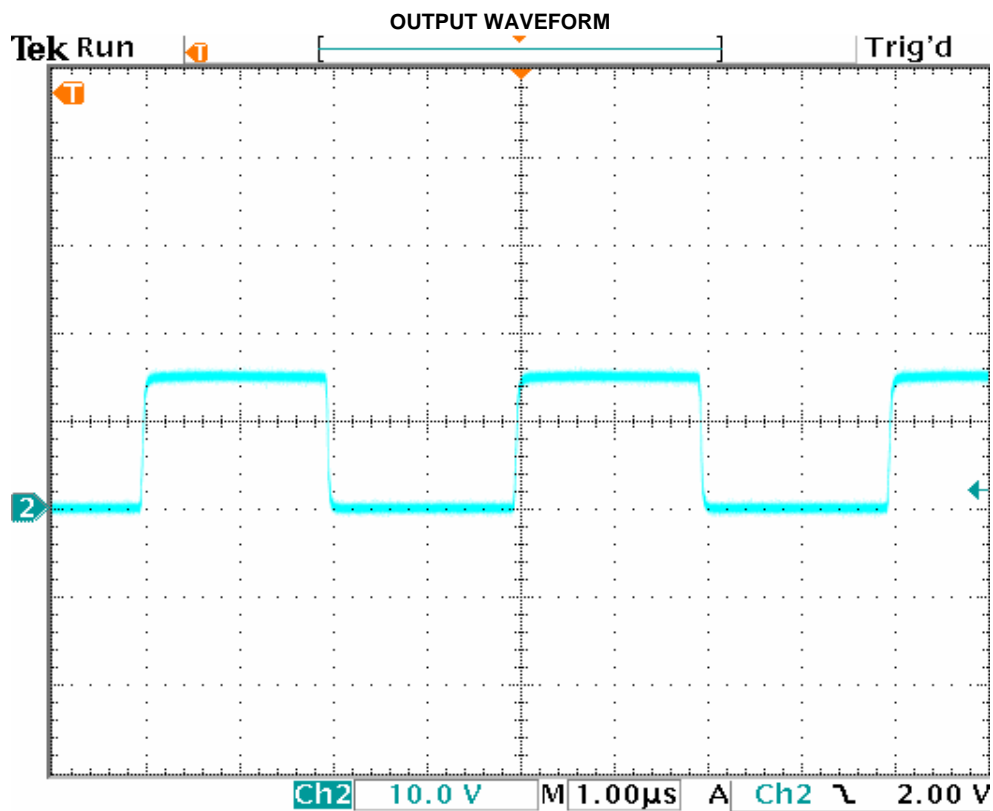
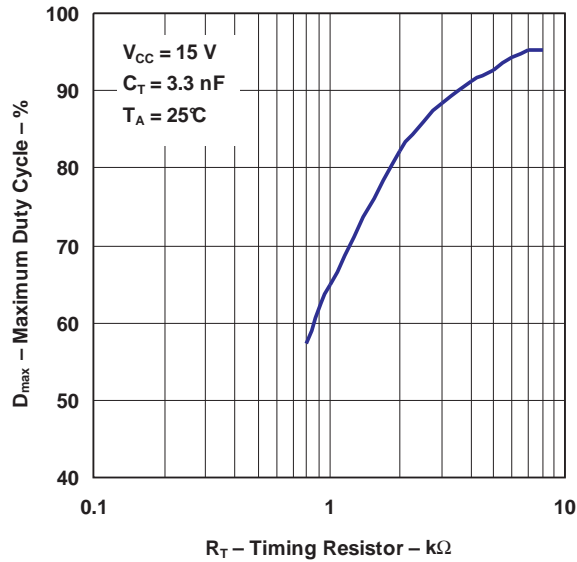


OUTPUT SATURATION VOLTAGE
VS
LOAD CURRENT



TYPICAL CHARACTERISTICS (continued)

MAXIMUM OUTPUT DUTY CYCLE
 VS
 TIMING RESISTOR



APPLICATION INFORMATION

The error-amplifier configuration circuit is shown in Figure 1.



- A. Error amplifier can source or sink up to 0.5 mA.

Figure 1. Error-Amplifier Configuration

The current-sense circuit is shown in Figure 2.



- A. Peak current (I_S) is determined by the formula: $I_{S(max)} = 1 / V/R_S$
- B. A small RC filter formed by resistor R_f and capacitor C_f may be required to suppress switch transients.

Figure 2. Current-Sense Circuit

The oscillator frequency is set using the circuit shown in Figure 3. The frequency is calculated as:

$$f = 1 / R_T C_T$$

For $R_T > 5 \text{ k}\Omega$:

$$f \approx 1.72 / R_T C_T$$

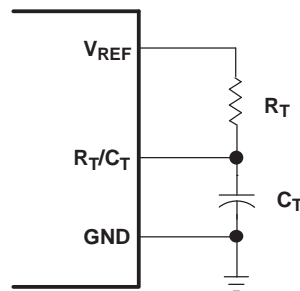
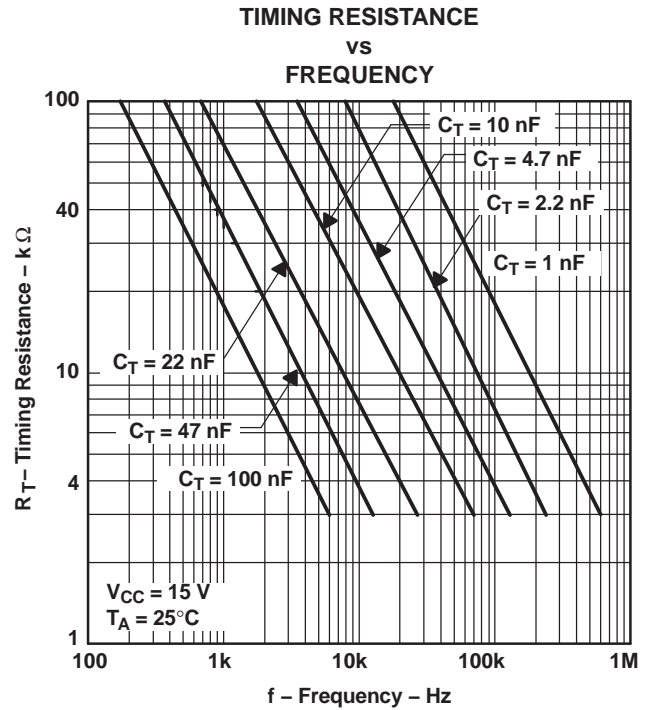
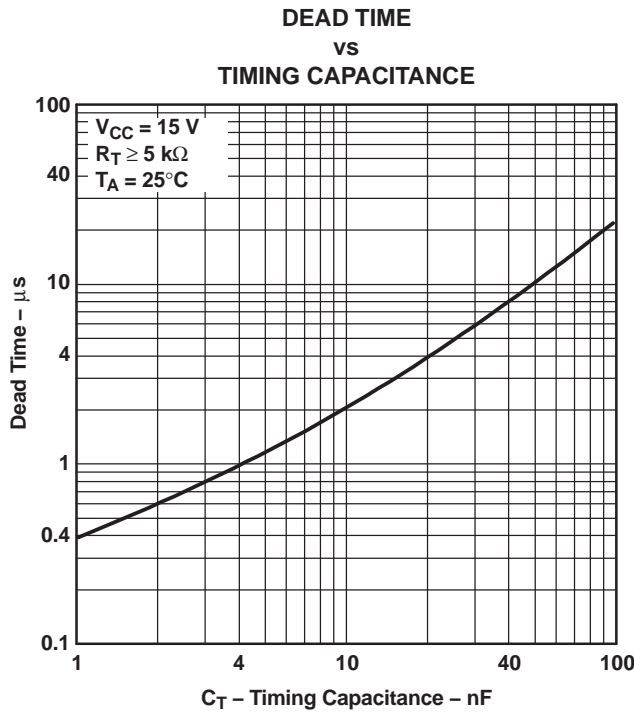


Figure 3. Oscillator Section

APPLICATION INFORMATION (continued)



Open-Loop Laboratory Test Fixture

In the open-loop laboratory test fixture (see Figure 4), high peak currents associated with loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to the GND terminal in a single-point ground. The transistor and 5-k Ω potentiometer sample the oscillator waveform and apply an adjustable ramp to the I_{SENSE} terminal.



Figure 4. Open-Loop Laboratory Test Fixture

APPLICATION INFORMATION (continued)

Shutdown Technique

The PWM controller (see Figure 5) can be shut down by two methods: either raise the voltage at I_{SENSE} above 1 V or pull the COMP terminal below a voltage two diode drops above ground. Either method causes the output of the PWM comparator to be high (refer to block diagram). The PWM latch is reset dominant so that the output remains low until the next clock cycle after the shutdown condition at the COMP or I_{SENSE} terminal is removed. In one example, an externally latched shutdown can be accomplished by adding an SCR that resets by cycling V_{CC} below the lower UVLO threshold. At this point, the reference turns off, allowing the SCR to reset.

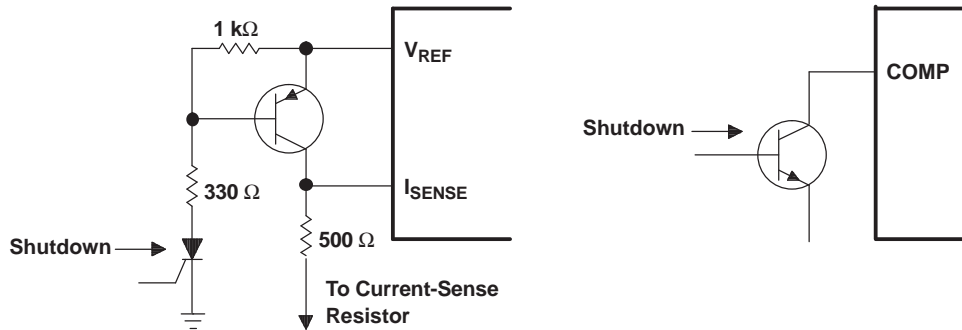


Figure 5. Shutdown Techniques

A fraction of the oscillator ramp can be summed resistively with the current-sense signal to provide slope compensation for converters requiring duty cycles over 50% (see Figure 6). Note that capacitor C forms a filter with R2 to suppress the leading-edge switch spikes.



Figure 6. Slope Compensation

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TL2842BD | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL2842B | Samples |
| TL2842BD-8 | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 2842B | Samples |
| TL2842BDR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL2842B | Samples |
| TL2842BDR-8 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 2842B | Samples |
| TL2842BP | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | TL2842BP | Samples |
| TL2843BD | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL2843B | Samples |
| TL2843BD-8 | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 2843B | Samples |
| TL2843BDR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL2843B | Samples |
| TL2843BDR-8 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 2843B | Samples |
| TL2843BDRG4-8 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 2843B | Samples |
| TL2843BP | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | TL2843BP | Samples |
| TL2844BD-8 | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 2844B | Samples |
| TL2844BDR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL2844B | Samples |
| TL2844BDR-8 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 2844B | Samples |
| TL2844BDRG4-8 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 2844B | Samples |
| TL2845BD | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL2845B | Samples |
| TL2845BD-8 | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 2845B | Samples |
| TL2845BDR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL2845B | Samples |
| TL2845BDR-8 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 2845B | Samples |
| TL2845BDRG4-8 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 2845B | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TL3842BD | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL3842B | Samples |
| TL3842BD-8 | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 3842B | Samples |
| TL3842BDR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL3842B | Samples |
| TL3842BDR-8 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 3842B | Samples |
| TL3842BP | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | TL3842BP | Samples |
| TL3843BD | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL3843B | Samples |
| TL3843BD-8 | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 3843B | Samples |
| TL3843BDR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL3843B | Samples |
| TL3843BDR-8 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 3843B | Samples |
| TL3843BDRG4 | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL3843B | Samples |
| TL3843BP | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | TL3843BP | Samples |
| TL3844BD-8 | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 3844B | Samples |
| TL3844BDR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL3844B | Samples |
| TL3844BDR-8 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 3844B | Samples |
| TL3844BP | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | TL3844BP | Samples |
| TL3845BD | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL3845B | Samples |
| TL3845BD-8 | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 3845B | Samples |
| TL3845BDR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL3845B | Samples |
| TL3845BDR-8 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 3845B | Samples |
| TL3845BP | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | TL3845BP | Samples |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TL2843B :

- Automotive : [TL2843B-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TL2842BDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL2842BDR-8 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL2843BDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL2843BDR-8 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL2844BDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL2844BDR-8 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL2845BDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL2845BDR-8 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL3842BDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL3842BDR-8 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL3843BDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL3843BDR-8 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL3844BDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL3844BDR-8 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL3845BDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL3845BDR-8 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TL2842BDR | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |
| TL2842BDR-8 | SOIC | D | 8 | 2500 | 340.5 | 336.1 | 25.0 |
| TL2843BDR | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |
| TL2843BDR-8 | SOIC | D | 8 | 2500 | 340.5 | 336.1 | 25.0 |
| TL2844BDR | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |
| TL2844BDR-8 | SOIC | D | 8 | 2500 | 340.5 | 336.1 | 25.0 |
| TL2845BDR | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |
| TL2845BDR-8 | SOIC | D | 8 | 2500 | 340.5 | 336.1 | 25.0 |
| TL3842BDR | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |
| TL3842BDR-8 | SOIC | D | 8 | 2500 | 340.5 | 336.1 | 25.0 |
| TL3843BDR | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |
| TL3843BDR-8 | SOIC | D | 8 | 2500 | 340.5 | 336.1 | 25.0 |
| TL3844BDR | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |
| TL3844BDR-8 | SOIC | D | 8 | 2500 | 340.5 | 336.1 | 25.0 |
| TL3845BDR | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |
| TL3845BDR-8 | SOIC | D | 8 | 2500 | 340.5 | 336.1 | 25.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| TL2842BD | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| TL2842BD-8 | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TL2842BP | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TL2843BD | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| TL2843BD-8 | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TL2843BP | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TL2844BD-8 | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TL2845BD | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| TL2845BD-8 | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TL3842BD | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| TL3842BD-8 | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TL3842BP | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TL3843BD | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| TL3843BD-8 | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TL3843BP | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TL3844BD-8 | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TL3844BP | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TL3845BD | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| TL3845BD-8 | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TL3845BP | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211283-3/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
 EXPOSED METAL SHOWN
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

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