The TL714C is a high-speed differential comparator fabricated with bipolar Schottky process technology. The circuit has differential inputs and a TTL-compatible logic output with symmetrical switching characteristics. The device operates from a single 5-V supply and is useful as a disk-memory read-chain data comparator.

**ORDERING INFORMATION**

<table>
<thead>
<tr>
<th>$T_A$</th>
<th>PACKAGE†</th>
<th>ORDERABLE PART NUMBER</th>
<th>TOP-SIDE MARKING</th>
</tr>
</thead>
<tbody>
<tr>
<td>0°C to 70°C</td>
<td>PDIP (P)</td>
<td>Tube of 50</td>
<td>TL714CP</td>
</tr>
<tr>
<td></td>
<td>SOIC (D)</td>
<td>Tube of 75</td>
<td>TL714CD</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Reel of 2500</td>
<td>TL714CDR</td>
</tr>
</tbody>
</table>

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
schematic of inputs and outputs

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, \( V_{CC} \) (see Note 1) 7 V
Differential input voltage, \( V_{ID} \) (see Note 2) ±5 V
Input voltage range, \( V_{I} \) \( V_{CC} \) to GND
Low-level output current, \( I_{OL} \) 40 mA
Package thermal impedance, \( \theta_{JA} \) (see Notes 3 and 4): D package 97°C/W
P package 85°C/W
Operating virtual junction temperature, \( T_{J} \) 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds 260°C
Storage temperature range, \( T_{stg} \) –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltage, are with respect to the network ground.
2. Differential voltage values are at \( \text{IN}+ \) with respect to \( \text{IN}− \).
3. Maximum power dissipation is a function of \( T_{J}(\text{max}) \), \( \theta_{JA} \), and \( T_{A} \). The maximum allowable power dissipation at any allowable ambient temperature is \( P_{D} = (T_{J}(\text{max})−T_{A})/\theta_{JA} \). Operating at the absolute maximum \( T_{J} \) of 150°C can affect reliability.
4. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

| \( V_{CC} \) | 4.75 | 5.25 | V |
| \( V_{IC} \) | Common-mode input voltage | 1.4 | to | \( V_{CC}−1.4 \) | V |
| \( I_{OH} \) | High-level output current | –1 | mA |
| \( I_{OL} \) | Low-level output current | 16 | mA |
| \( T_{A} \) | Operating free-air temperature | 0 | 70 | °C |
**Electrical Characteristics**

Over free-air operating temperature range, $V_{CC} = 5\, \text{V}$ (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP†</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_T$ Threshold voltage ($V_{T+}$ and $V_{T-}$)</td>
<td>$V_{IC} = 1.4, \text{V}$ to $3.6, \text{V}$</td>
<td>$-75\ddagger$</td>
<td>75</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>$V_{\text{hys}}$ Hysteresis ($V_{T+} - V_{T-}$)</td>
<td></td>
<td>2</td>
<td>10</td>
<td>30</td>
<td>mV</td>
</tr>
<tr>
<td>$V_{OH}$ High-level output voltage</td>
<td>$V_{ID} = 100, \text{mV}, \quad I_{OH} = -1, \text{mA}$</td>
<td>2.7</td>
<td>3.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{OL}$ Low-level output voltage</td>
<td>$V_{ID} = -100, \text{mV}, \quad I_{OL} = 16, \text{mA}$</td>
<td>0.4</td>
<td>0.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{OS}$ Short-circuit output current</td>
<td></td>
<td>$-30$</td>
<td>$-110$</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$r_i$ Differential input resistance</td>
<td></td>
<td>2.9</td>
<td>kΩ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{CC}$ Supply current</td>
<td>$V_{ID} = -100, \text{mV}, \quad I_O = 0$</td>
<td>7</td>
<td>12</td>
<td>mA</td>
<td></td>
</tr>
</tbody>
</table>

† All typical values are at $T_A = 25\, \text{°C}$.

‡ The algebraic convention, where the more-negative limit is designated as minimum, is used in this data sheet for input threshold voltage levels only.

**Switching Characteristics**

$V_{CC} = 5\, \text{V}, \quad T_A = 25\, \text{°C}$

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP†</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{\text{max}}$ Maximum operating frequency</td>
<td>$V_{ID} = \pm250, \text{mV}, \quad C_L = 25, \text{pF}, \quad t_r = t_f = 4, \text{ns}, \quad \text{Input duty cycle} = 50%$</td>
<td>50</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{\text{PLH}}$ Propagation delay time, low-to-high-level output</td>
<td>$V_{ID} = \pm100, \text{mV}, \quad C_L = 25, \text{pF}, \quad \text{See Figures 1 and 2}$</td>
<td>6</td>
<td>12</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_{\text{PHL}}$ Propagation delay time, high-to-low-level output</td>
<td>$V_{ID} = \pm100, \text{mV}, \quad C_L = 25, \text{pF}, \quad \text{See Figure 3}$</td>
<td>4</td>
<td>8</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

† All typical values are at $T_A = 25\, \text{°C}$.

**Parameter Measurement Information**

![Figure 1. Propagation Delay Time, Low to High ($t_{\text{PLH}}$)](image)

![Figure 2. Propagation Delay Time, High to Low ($t_{\text{PHL}}$)](image)
Figure 3. Rise and Fall Times (tr, tf)
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TL714CD</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>75</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>TL714C</td>
</tr>
<tr>
<td>TL714CDR</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>TL714C</td>
</tr>
<tr>
<td>TL714CP</td>
<td>ACTIVE</td>
<td>PDIP</td>
<td>P</td>
<td>8</td>
<td>50</td>
<td>RoHS &amp; Green</td>
<td>N / A for Pkg Type</td>
<td>0 to 70</td>
<td>TL714CP</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
- **RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
- **Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead finish/Ball material** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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### TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

![Reel Dimensions Diagram](image1)

**TAPE DIMENSIONS**

![Tape Dimensions Diagram](image2)

*Dimension designed to accommodate the component width*

*Dimension designed to accommodate the component length*

*Dimension designed to accommodate the component thickness*

*Overall width of the carrier tape*

*Pitch between successive cavity centers*

#### PACKAGE MATERIALS INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin 1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>TL714CDR</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>330.0</td>
<td>12.4</td>
<td>6.4</td>
<td>5.2</td>
<td>2.1</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>

*All dimensions are nominal.*
**TAPE AND REEL BOX DIMENSIONS**

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TL714CDR</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>340.5</td>
<td>338.1</td>
<td>20.6</td>
</tr>
</tbody>
</table>
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE: 8X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 variation BA.
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