







TLC69600-Q1, TLC69610-Q1, TLC69650-Q1, TLC69660-Q1

# SNVSCK9 - JUNE 2023

# TLC696x0-Q1 Automotive Scan MOSFET Controller for TLC696x2/4/8-Q1

#### 1 Features

- AEC-Q100 qualified for automotive applications:
  - Device temperature grade 1: -40°C to +125°C,  $\mathsf{T}_\mathsf{A}$
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C4B
- Functional Safety-Capable:
  - Documentation available to aid functional safety system design
- Full array local dimming topology:
  - Support up to 1024 devices cascaded
- Operating voltage V<sub>CC</sub> range: 3V to 5.5V
- Flexible P-MOSFET driving options:
  - Maximum channel current / voltage:
    - 30mA / 20V: TLC69600-Q1
    - 60mA / 20V: TLC69610-Q1
    - 30mA / 50V: TLC69650-Q1
    - 60mA / 50V: TLC69660-Q1
  - Global 8-bit Maximum Current (MC) setting
  - Individual 8-bit Channel Current (CC) setting
- High speed daisy chain interface:
  - I/O voltage compatible with: 1.8V / 3.3V
  - Data transfer rate: up to 20MHz
- EMI enhancement:
  - Programmable interface driving capability
- Diagnostics:
  - Device thermal shutdown detection
  - Report interface option:
    - UART and interrupt pin (INT)
    - Two-wire output: CLK\_O and SOUT

# 2 Applications

- · LCD local dimming backlight:
  - Automotive central information display
  - Automotive cluster display
  - Automotive head-up display

# 3 Description

TLC696x0-Q1 is a scan MOSFET controller compatible with current-sink driver TLC696x2/4/8-Q1 to achieve 2/4/8 time-multiplexing control. Each device integrates with 16 constant current sinks for up to 8 scan MOSFETs control. The device equips with ghost-cancellation function to eliminate upside ghosting.

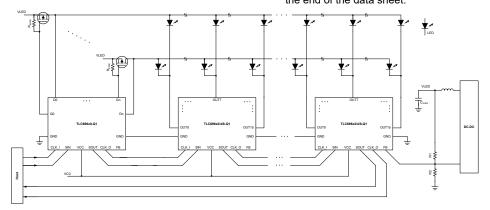
To optimize system efficiency, the device is equipped with adaptive headroom voltage control scheme to directly control DC/DC. Only the FB pin from last device in serial chain should be connected to DC/DC to achieve simplified system layout. The device also integrates minimum brightness update latency, black insertion and VRR features to improve display quality.

TLC696x0-Q1 has three error flags: LED open detection (LOD), LED short detection (LSD) and thermal shutdown detection (TSD) for diagnostic. The device implements two options for readback including UART/INT and SOUT/CLK\_O which is programmable by register.

#### **Device Information**

PART NUMBER	PACKAGE <sup>(1)</sup>	BODY SIZE (NOM)			
TLC696x0-Q1	WQFN (24) Wettable flank	4mm × 4mm			
	HTSSOP (28)	9.7mm × 4.4mm			

For all available packages, see the orderable addendum at (1) the end of the data sheet.



Simplified Schematic



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# **4 Device and Documentation Support**

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

#### 4.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 4.2 Support Resources

TI E2E<sup>™</sup> support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

#### 4.3 Trademarks

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# 4.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 4.5 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

#### 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES				
June 2023	*	Initial Release				



# 6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



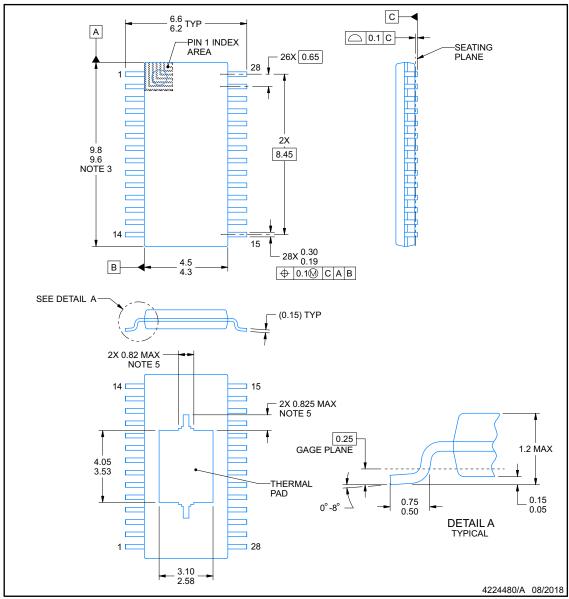
**PWP0028M** 



#### PACKAGE OUTLINE

# PowerPAD<sup>™</sup> TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



#### NOTES:

PowerPAD is a trademark of Texas Instruments.

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

  4. Reference JEDEC registration MO-153.
- 5. Features may differ or may not be present.



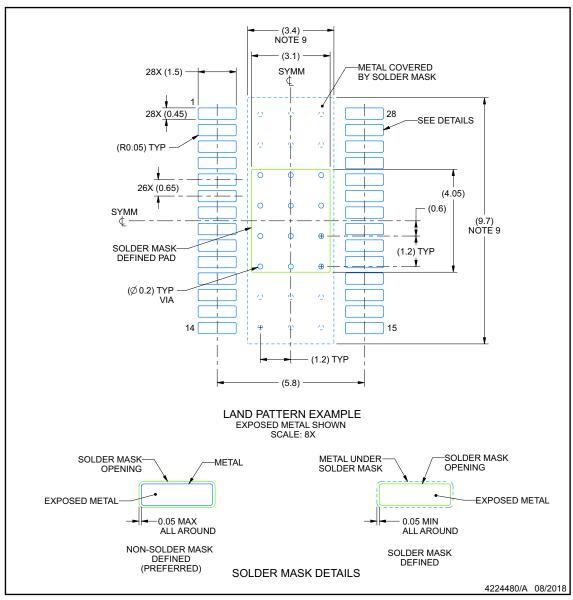


#### **EXAMPLE BOARD LAYOUT**

# **PWP0028M**

# PowerPAD<sup>™</sup> TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
- 8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
- 9. Size of metal pad may vary due to creepage requirement.
- 10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



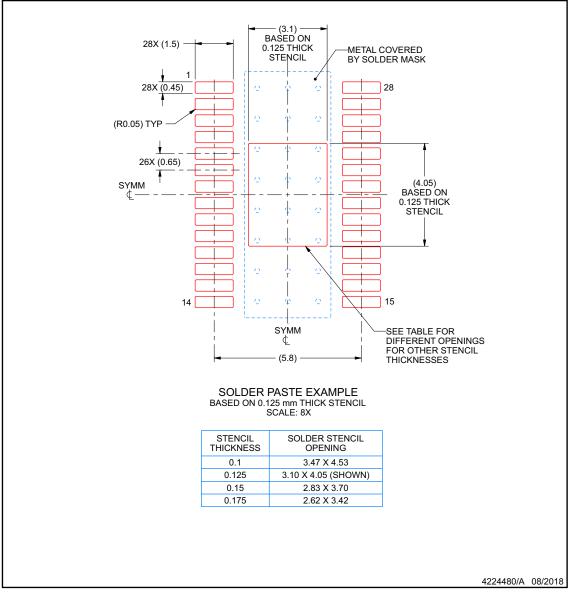


#### **EXAMPLE STENCIL DESIGN**

# **PWP0028M**

# PowerPAD<sup>™</sup> TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



- 11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

  12. Board assembly site may have different recommendations for stencil design.



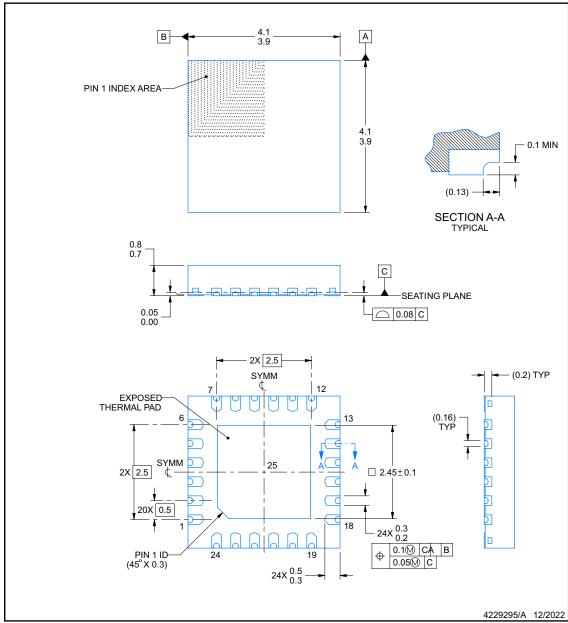
RTW0024N



# PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



#### NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
   This drawing is subject to change without notice.
   The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



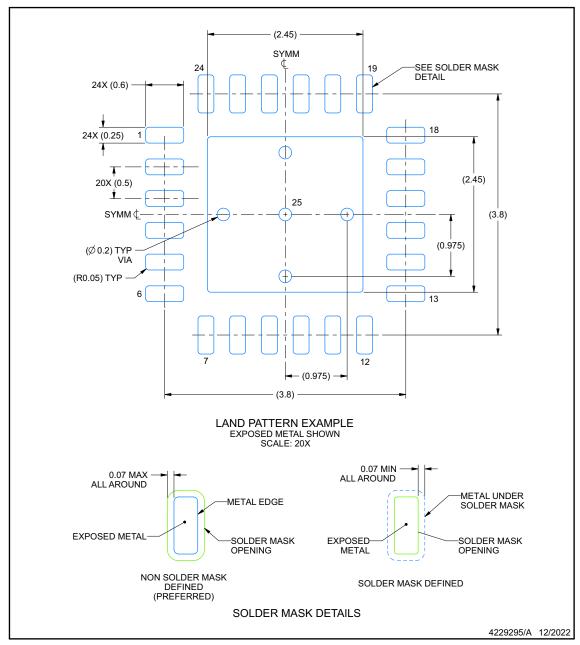


#### **EXAMPLE BOARD LAYOUT**

# RTW0024N

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



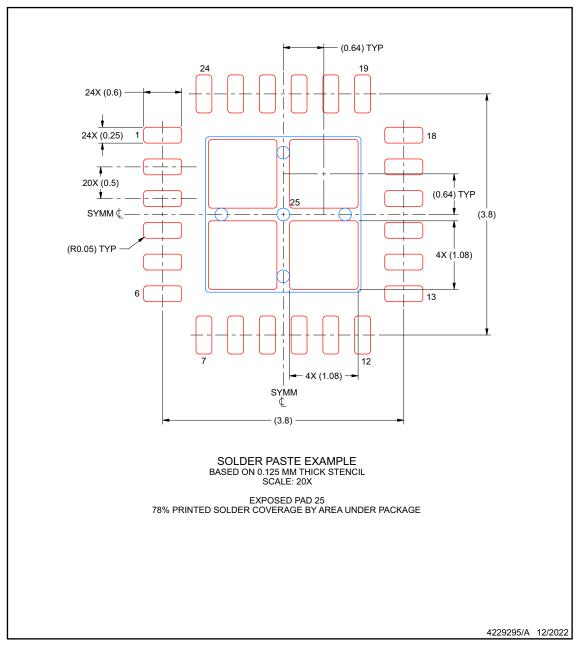


# **EXAMPLE STENCIL DESIGN**

# RTW0024N

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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#### PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead finish/ Ball material	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
							(6)				
TLC69600QPWPRQ1	ACTIVE	HTSSOP	PWP	28	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	69600Q	Samples
TLC69600QRTWRQ1	ACTIVE	WQFN	RTW	24	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	69600Q	Samples
TLC69610QPWPRQ1	ACTIVE	HTSSOP	PWP	28	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	69610Q	Samples
TLC69610QRTWRQ1	ACTIVE	WQFN	RTW	24	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	69610Q	Samples
TLC69650QPWPRQ1	ACTIVE	HTSSOP	PWP	28	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	69650Q	Samples
TLC69650QRTWRQ1	ACTIVE	WQFN	RTW	24	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	69650Q	Samples
TLC69660QPWPRQ1	ACTIVE	HTSSOP	PWP	28	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	69660Q	Samples
TLC69660QRTWRQ1	ACTIVE	WQFN	RTW	24	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	69660Q	Samples

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

# **PACKAGE OPTION ADDENDUM**

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(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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#### OTHER QUALIFIED VERSIONS OF TLC69600-Q1, TLC69610-Q1, TLC69650-Q1, TLC69660-Q1:

• Catalog: TLC69600, TLC69610, TLC69650, TLC69660

NOTE: Qualified Version Definitions:

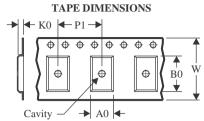
Catalog - TI's standard catalog product



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# TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC69600QPWPRQ1	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
TLC69600QRTWRQ1	WQFN	RTW	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLC69610QPWPRQ1	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
TLC69610QRTWRQ1	WQFN	RTW	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLC69650QPWPRQ1	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
TLC69650QRTWRQ1	WQFN	RTW	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLC69660QPWPRQ1	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
TLC69660QRTWRQ1	WQFN	RTW	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2



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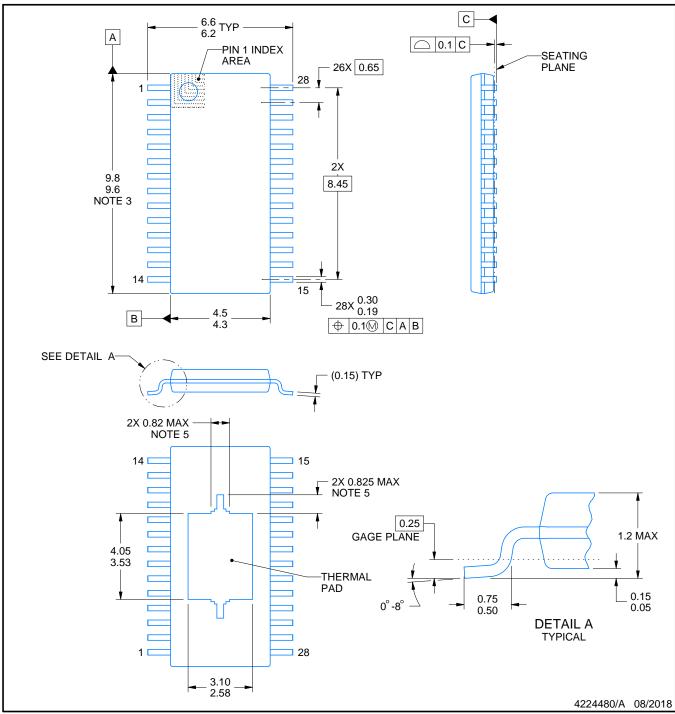


# \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC69600QPWPRQ1	HTSSOP	PWP	28	2000	356.0	356.0	35.0
TLC69600QRTWRQ1	WQFN	RTW	24	3000	367.0	367.0	35.0
TLC69610QPWPRQ1	HTSSOP	PWP	28	2000	356.0	356.0	35.0
TLC69610QRTWRQ1	WQFN	RTW	24	3000	367.0	367.0	35.0
TLC69650QPWPRQ1	HTSSOP	PWP	28	2000	356.0	356.0	35.0
TLC69650QRTWRQ1	WQFN	RTW	24	3000	367.0	367.0	35.0
TLC69660QPWPRQ1	HTSSOP	PWP	28	2000	356.0	356.0	35.0
TLC69660QRTWRQ1	WQFN	RTW	24	3000	367.0	367.0	35.0

# PowerPAD<sup>™</sup> TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



#### NOTES:

PowerPAD is a trademark of Texas Instruments.

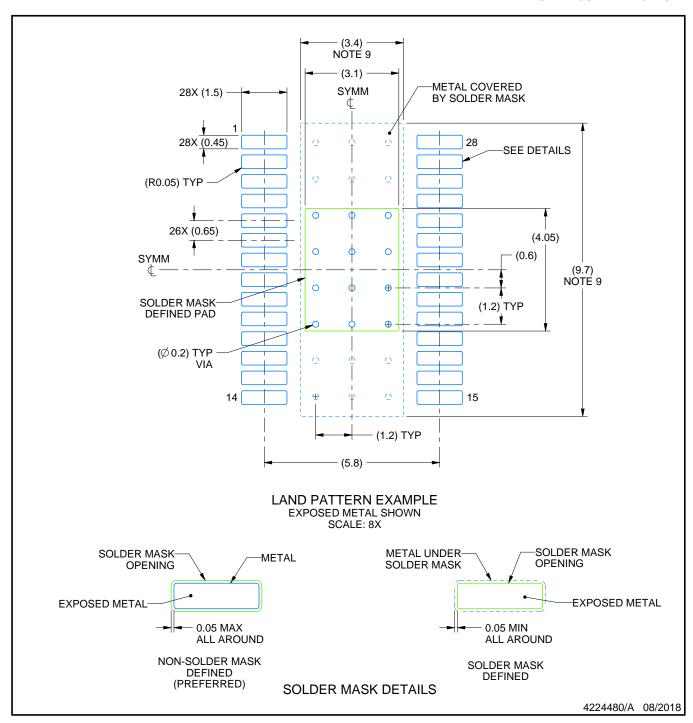
- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
  4. Reference JEDEC registration MO-153.
- 5. Features may differ or may not be present.



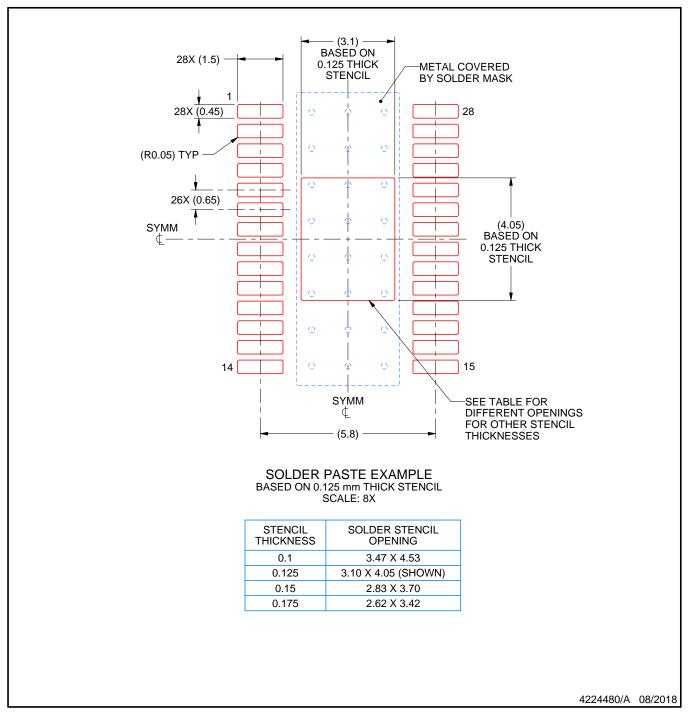
SMALL OUTLINE PACKAGE



- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
- 8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
- 9. Size of metal pad may vary due to creepage requirement.
- 10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SMALL OUTLINE PACKAGE

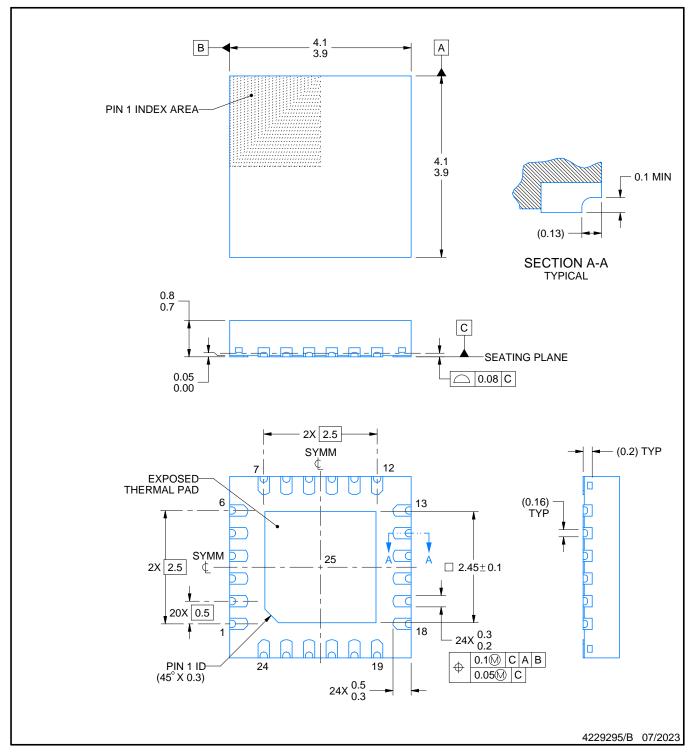


- 11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 12. Board assembly site may have different recommendations for stencil design.





PLASTIC QUAD FLATPACK - NO LEAD

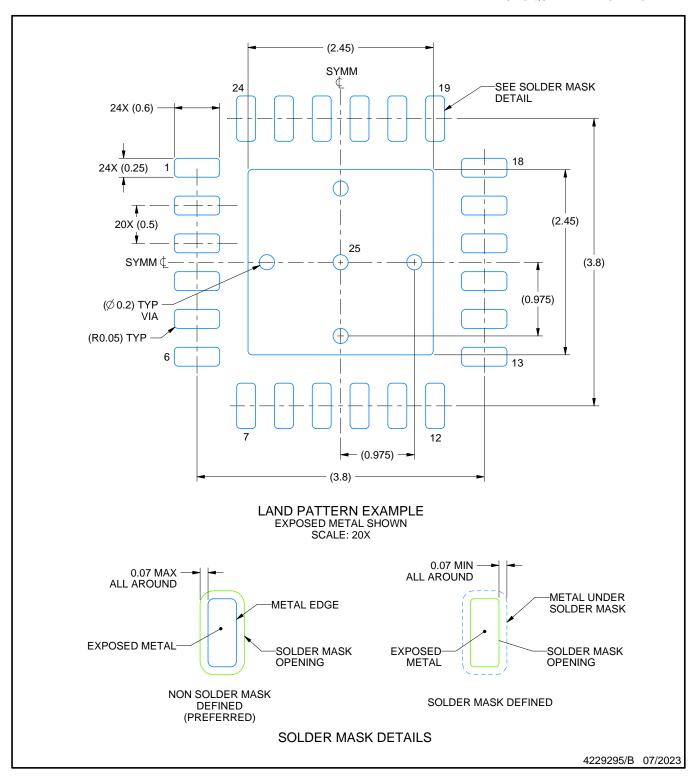


#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
  2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
- 4. Reference JEDEC registration MO-220. For wetable flank, reference IPC document IPC-7093.



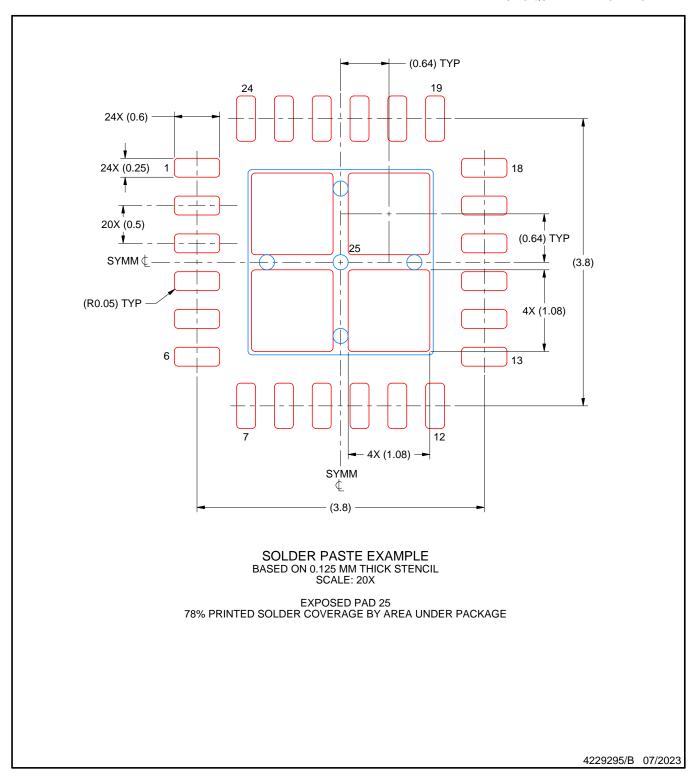
PLASTIC QUAD FLATPACK - NO LEAD



- 5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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