

# Excalibur™ LOW-NOISE HIGH-SPEED PRECISION OPERATIONAL AMPLIFIERS

Check for Samples: [TLE2141-Q1](#)

## FEATURES

- **Qualified for Automotive Applications**
- **Low Noise**
  - 10 Hz ... 15 nV/√Hz
  - 1 kHz ... 10.5 nV/√Hz
- **10000-pF Load Capability**
- **20-mA Min Short-Circuit Output Current**
- **27-V/μs Slew Rate (Min)**
- **High Gain-Bandwidth Product ... 5.9 MHz**
- **Low  $V_{IO}$  ... 500 μV (Max) at 25°C**
- **Single or Split Supply ... 4 V to 44 V**
- **Fast Settling Time**
  - 340 ns to 0.1%
  - 400 ns to 0.01%
- **Saturation Recovery ... 150 ns**
- **Large Output Swing ...  $V_{CC-} + 0.1 V$  to  $V_{CC+} - 1 V$**

## DESCRIPTION

The TLE2141-Q1 device is a high-performance, internally compensated operational amplifier built using the Texas Instruments complementary bipolar Excalibur™ process. It is a pin-compatible upgrade to standard industry products.

The design incorporates an input stage that simultaneously achieves low audio-band noise of 10.5 nV/√Hz with a 10-Hz 1/f corner and symmetrical 40-V/μs slew rate typically with loads up to 800 pF. The resulting low distortion and high power bandwidth are important in high-fidelity audio applications. A fast settling time of 340 ns to 0.1% of a 10-V step with a 2-kΩ/100-pF load is useful in fast actuator/positioning drivers. Under similar test conditions, settling time to 0.01% is 400 ns.

The device is stable with capacitive loads up to 10 nF, although the 6-MHz bandwidth decreases to 1.8 MHz at this high loading level. As such, the TLE2141-Q1 is useful for low-droop sample-and-holds and direct buffering of long cables, including 4-mA to 20-mA current loops.

The special design also exhibits an improved insensitivity to inherent integrated circuit component mismatches as is evidenced by a 500-μV maximum offset voltage and 1.7-μV/°C typical drift. Minimum common-mode rejection ratio and supply-voltage rejection ratio are 85 dB and 90 dB, respectively.

Device performance is relatively independent of supply voltage over the ±2-V to ±22-V range. Inputs can operate between  $V_{CC-} - 0.3 V$  to  $V_{CC+} - 1.8 V$  without inducing phase reversal, although excessive input current may flow out of each input exceeding the lower common-mode input range. The all-npn output stage provides a nearly rail-to-rail output swing of  $V_{CC-} - 0.1 V$  to  $V_{CC+} - 1 V$  under light current-loading conditions. The device can sustain shorts to either supply since output current is internally limited, but care must be taken to ensure that maximum package power dissipation is not exceeded.

The TLE2141-Q1 device can also be used as a comparator. Differential inputs of  $V_{CC±}$  can be maintained without damage to the device. Open-loop propagation delay with TTL supply levels is typically 200 ns. This gives a good indication as to output stage saturation recovery when the device is driven beyond the limits of recommended output swing.

The TLE2141-Q1 device is available in industry-standard 8-pin package. The device is characterized for operation from –40°C to 125°C.

## ORDERING INFORMATION<sup>(1)</sup>

T <sub>A</sub>	PACKAGE	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC – D (8 pin) Reel of 2500	TLE2141QDRQ1	2141Q

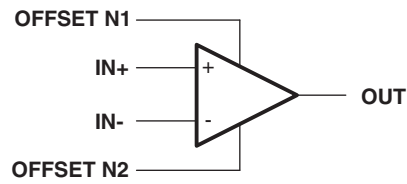
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).



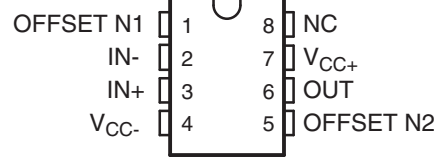
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Excalibur is a trademark of Texas Instruments.

**SYMBOL**

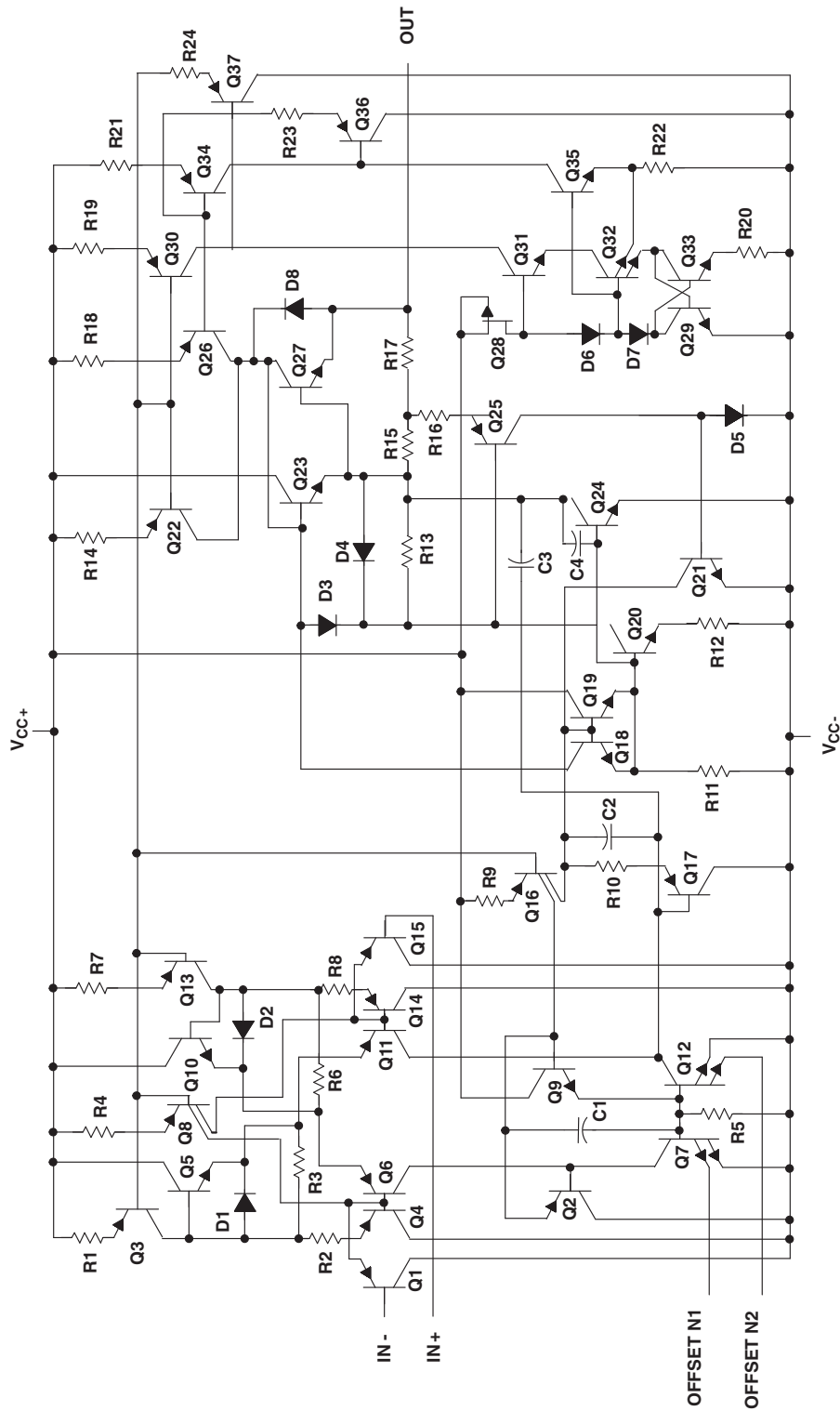


**D PACKAGE  
(TOP VIEW)**



NC – No internal connection

Figure 1. EQUIVALENT SCHEMATIC



DEVICE COMPONENT COUNT

COMPONENT	TLE2141-Q1
Transistors	46
Resistors	24
Diodes	8
Capacitors	4
Epi-FET	1

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
V <sub>CC+</sub>	Supply voltage <sup>(2)</sup>	22	V
V <sub>CC-</sub>	Supply voltage	-22	V
V <sub>ID</sub>	Differential input voltage <sup>(3)</sup>	±44	V
V <sub>I</sub>	Input voltage range (any input)	V <sub>CC+</sub> to (V <sub>CC-</sub> - 0.3)	V
I <sub>I</sub>	Input current (each input)	±1	mA
I <sub>O</sub>	Output current	±80	mA
	Total current into V <sub>CC+</sub>	80	mA
	Total current out of V <sub>CC-</sub>	80	mA
	Duration of short-circuit current at (or below) 25°C <sup>(4)</sup>	Unlimited	
θ <sub>JA</sub>	Package thermal impedance <sup>(5) (6)</sup>	D package (8 pin)	97.1 °C/W
T <sub>A</sub>	Operating free-air temperature range	-40 to 125	°C
T <sub>stg</sub>	Storage temperature range	-65 to 150	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to the midpoint between V<sub>CC+</sub> and V<sub>CC-</sub>.
- (3) Differential voltages are at IN+ with respect to IN-. Excessive current flows, if input, are brought below V<sub>CC-</sub> - 0.3 V.
- (4) The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.
- (5) Maximum power dissipation is a function of T<sub>J(max)</sub>, θ<sub>JA</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any allowable ambient temperature is P<sub>D</sub> = (T<sub>J(max)</sub> - T<sub>A</sub>)/θ<sub>JA</sub>. Operating at the absolute maximum T<sub>J</sub> of 150°C can affect reliability.
- (6) The package thermal impedance is calculated in accordance with JESD 51-7.

## RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT	
V <sub>CC±</sub>	Supply voltage	±2	±22	V	
V <sub>IC</sub>	Common-mode input voltage	V <sub>CC</sub> = 5 V	0	2.7	V
		V <sub>CC±</sub> = ±15 V	-15	12.7	
T <sub>A</sub>	Operating free-air temperature	-40	125	°C	

**ELECTRICAL CHARACTERISTICS**
 $V_{CC} = 5\text{ V}$ , at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A$ <sup>(1)</sup>	MIN	TYP	MAX	UNIT	
$V_{IO}$	Input offset voltage	$V_O = 2.5\text{ V}$ , $R_S = 50\ \Omega$ , $V_{IC} = 2.5\text{ V}$	25°C		225	1400	$\mu\text{V}$	
			Full range			2100		
$\alpha_{VIO}$	Temperature coefficient of input offset voltage	$V_O = 2.5\text{ V}$ , $R_S = 50\ \Omega$ , $V_{IC} = 2.5\text{ V}$	Full range		1.7		$\mu\text{V}/^\circ\text{C}$	
$I_{IO}$	Input offset current	$V_O = 2.5\text{ V}$ , $R_S = 50\ \Omega$ , $V_{IC} = 2.5\text{ V}$	25°C		8	100	nA	
			Full range			250		
$I_{IB}$	Input bias current	$V_O = 2.5\text{ V}$ , $R_S = 50\ \Omega$ , $V_{IC} = 2.5\text{ V}$	25°C		-0.8	-2	$\mu\text{A}$	
			Full range			-2.3		
$V_{ICR}$	Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	0 to 3	-0.3 to 3.2		V	
			Full range	0 to 2.7	-0.3 to 2.9			
$V_{OH}$	High-level output voltage		25°C	$I_{OH} = -150\ \mu\text{A}$	3.9	4.1	V	
				$I_{OH} = -1.5\text{ mA}$	3.8	4		
				$I_{OH} = -15\text{ mA}$	3.2	3.7		
			Full range	$I_{OH} = -100\ \mu\text{A}$	3.75			
				$I_{OH} = -1\text{ mA}$	3.65			
				$I_{OH} = -10\text{ mA}$	3.25			
$V_{OL}$	Low-level output voltage		25°C	$I_{OL} = 150\ \mu\text{A}$		75	125	mV
				$I_{OL} = 1.5\text{ mA}$		150	225	
				$I_{OL} = 15\text{ mA}$		1.2	1.4	V
			Full range	$I_{OL} = 100\ \mu\text{A}$		200		
				$I_{OL} = 1\text{ mA}$		250		
				$I_{OL} = 10\text{ mA}$		1.25		V
$A_{VD}$	Large-signal differential voltage amplification	$V_{IC} = \pm 2.5\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $V_O = 1\text{ V to }1.5\text{ V}$	25°C	50	220		V/mV	
			Full range	5				
$r_i$	Input resistance		25°C		70		M $\Omega$	
$c_i$	Input capacitance		25°C		2.5		pF	
$z_o$	Open-loop output impedance	$f = 1\text{ MHz}$	25°C		30		$\Omega$	
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}(\text{min})$ , $R_S = 50\ \Omega$	25°C	85	118		dB	
			Full range	80				
$k_{SVR}$	Supply-voltage rejection ratio ( $\Delta V_{CC\pm}/\Delta V_{IO}$ )	$V_{CC\pm} = \pm 2.5\text{ V to } \pm 15\text{ V}$ , $R_S = 50\ \Omega$	25°C	90	106		dB	
			Full range	85				
$I_{CC}$	Supply current	$V_O = 2.5\text{ V}$ , No load, $V_{IC} = 2.5\text{ V}$	25°C		3.4	4.4	mA	
			Full range			4.6		

(1) Full range is  $-40^\circ\text{C}$  to  $125^\circ\text{C}$ .

## OPERATING CHARACTERISTICS

$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR+	Positive slew rate	$A_{VD} = -1$ , $R_L = 2\text{ k}\Omega^{(1)}$ , $C_L = 500\text{ pF}$		45		V/ $\mu\text{s}$
SR–	Negative slew rate	$A_{VD} = -1$ , $R_L = 2\text{ k}\Omega^{(1)}$ , $C_L = 500\text{ pF}$		42		V/ $\mu\text{s}$
$t_s$	Settling time	$A_{VD} = -1$ , 2.5-V step	To 0.1%	0.16		$\mu\text{s}$
			To 0.01%	0.22		
$V_n$	Equivalent input noise voltage	$R_S = 20\ \Omega$	$f = 10\text{ Hz}$	15		$\text{nV}/\sqrt{\text{Hz}}$
			$f = 1\text{ kHz}$	10.5		
$V_{n(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$		0.48		$\mu\text{V}$
		$f = 0.1\text{ Hz to }10\text{ Hz}$		0.51		
$I_n$	Equivalent input noise current	$f = 10\text{ Hz}$		1.92		$\text{pA}/\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$		0.5		
THD+N	Total harmonic distortion plus noise	$V_O = 1\text{ V to }3\text{ V}$ , $R_L = 2\text{ k}\Omega^{(1)}$ , $A_{VD} = 2$ , $f = 10\text{ kHz}$		0.0052		%
$B_1$	Unity-gain bandwidth	$R_L = 2\text{ k}\Omega^{(1)}$ , $C_L = 100\text{ pF}^{(1)}$		5.9		MHz
	Gain-bandwidth product	$R_L = 2\text{ k}\Omega^{(1)}$ , $C_L = 100\text{ pF}^{(1)}$ , $f = 100\text{ kHz}$		5.8		MHz
BOM	Maximum output-swing bandwidth	$V_{O(PP)} = 2\text{ V}$ , $R_L = 2\text{ k}\Omega^{(1)}$ , $A_{VD} = 1$		660		kHz
$\Phi_m$	Phase margin at unity gain	$R_L = 2\text{ k}\Omega^{(1)}$ , $C_L = 100\text{ pF}^{(1)}$		57		$^\circ$

(1)  $R_L$  and  $C_L$  terminated to 2.5 V.

**ELECTRICAL CHARACTERISTICS**
 $V_{CC} = \pm 15\text{ V}$ , at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A$ <sup>(1)</sup>	MIN	TYP	MAX	UNIT
$V_{IO}$	Input offset voltage	$V_{IC} = 0, R_S = 50\ \Omega$	25°C		200	900	$\mu\text{V}$
			Full range			1700	
$\alpha_{VIO}$	Temperature coefficient of input offset voltage	$V_{IC} = 0, R_S = 50\ \Omega$	Full range		1.7		$\mu\text{V}/^\circ\text{C}$
$I_{IO}$	Input offset current	$V_{IC} = 0, R_S = 50\ \Omega$	25°C		7	100	nA
			Full range			250	
$I_{IB}$	Input bias current	$V_{IC} = 0, R_S = 50\ \Omega$	25°C		-0.7	-1.5	$\mu\text{A}$
			Full range			-1.8	
$V_{ICR}$	Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	-15 to 13	-15.3 to 13.2		V
			Full range		-15 to 12.7	-15.3 to 12.9	
$V_{OM+}$	Maximum positive peak output voltage swing		25°C	$I_O = -150\ \mu\text{A}$	13.8	14.1	V
				$I_O = -1.5\ \text{mA}$	13.7	14	
				$I_O = -15\ \text{mA}$	13.1	13.7	
			Full range	$I_O = -100\ \mu\text{A}$	13.7		
				$I_O = -1\ \text{mA}$	13.6		
				$I_O = -10\ \text{mA}$	13.1		
$V_{OM-}$	Maximum negative peak output voltage swing		25°C	$I_O = 150\ \mu\text{A}$	-14.7	-14.9	V
				$I_O = 1.5\ \text{mA}$	-14.5	-14.8	
				$I_O = 15\ \text{mA}$	-13.4	-13.8	
			Full range	$I_O = 100\ \mu\text{A}$	-14.6		
				$I_O = 1\ \text{mA}$	-14.5		
				$I_O = 10\ \text{mA}$	-13.4		
$A_{VD}$	Large-signal differential voltage amplification	$V_O = \pm 10\ \text{V}, R_L = 2\ \text{k}\Omega$	25°C	100	450		V/mV
			Full range		20		
$r_i$	Input resistance		25°C		65		M $\Omega$
$c_i$	Input capacitance		25°C		2.5		pF
$z_o$	Open-loop output impedance	$f = 1\ \text{MHz}$	25°C		30		$\Omega$
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}(\text{min}), R_S = 50\ \Omega$	25°C	85	108		dB
			Full range		80		
$k_{SVR}$	Supply-voltage rejection ratio ( $\Delta V_{CC\pm}/\Delta V_{IO}$ )	$V_{CC\pm} = \pm 2.5\ \text{V to } \pm 15\ \text{V}, R_S = 50\ \Omega$	25°C	90	106		dB
			Full range		85		
$I_{OS}$	Short-circuit output current	$V_O = 0$	25°C	$V_{ID} = 1\ \text{V}$	-25	-50	mA
				$V_{ID} = -1\ \text{V}$	20	31	
$I_{CC}$	Supply current	$V_O = 0, \text{No load}, V_{IC} = 2.5\ \text{V}$	25°C		3.5	4.5	mA
			Full range			4.7	

(1) Full range is  $-40^\circ\text{C}$  to  $125^\circ\text{C}$ .

## OPERATING CHARACTERISTICS

$V_{CC} = \pm 15\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR+	Positive slew rate	$A_{VD} = -1$ , $R_L = 2\text{ k}\Omega$ , $C_L = 100\text{ pF}$	27	45		V/ $\mu\text{s}$
SR-	Negative slew rate	$A_{VD} = -1$ , $R_L = 2\text{ k}\Omega$ , $C_L = 100\text{ pF}$	27	42		V/ $\mu\text{s}$
$t_s$	Settling time	$A_{VD} = -1$ , 10-V step	To 0.1%	0.34		$\mu\text{s}$
			To 0.01%	0.4		
$V_n$	Equivalent input noise voltage	$R_S = 20\ \Omega$	$f = 10\text{ Hz}$	15		$\text{nV}/\sqrt{\text{Hz}}$
			$f = 1\text{ kHz}$	10.5		
$V_{n(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$		0.48		$\mu\text{V}$
		$f = 0.1\text{ Hz to }10\text{ Hz}$		0.51		
$I_n$	Equivalent input noise current	$f = 10\text{ Hz}$		1.89		$\text{pA}/\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$		0.47		
THD+N	Total harmonic distortion plus noise	$V_{O(PP)} = 20\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $A_{VD} = 10$ , $f = 10\text{ kHz}$		0.01		%
$B_1$	Unity-gain bandwidth	$R_L = 2\text{ k}\Omega$ , $C_L = 100\text{ pF}$		6		MHz
	Gain-bandwidth product	$R_L = 2\text{ k}\Omega$ , $C_L = 100\text{ pF}$ , $f = 100\text{ kHz}$		5.9		MHz
BOM	Maximum output-swing bandwidth	$V_{O(PP)} = 20\text{ V}$ , $A_{VD} = 1$ , $R_L = 2\text{ k}\Omega$ , $C_L = 100\text{ pF}$		668		kHz
$\phi_m$	Phase margin at unity gain	$R_L = 2\text{ k}\Omega$ , $C_L = 100\text{ pF}$		58		$^\circ$



## TYPICAL CHARACTERISTICS

### Table 1. Table of Graphs

$V_{IO}$	Input offset voltage	Distribution	<a href="#">Figure 2</a>
$I_{IO}$	Input offset current	vs Free-air temperature	<a href="#">Figure 3</a>
$I_{IB}$	Input bias current	vs Common-mode input voltage	<a href="#">Figure 4</a>
		vs Free-air temperature	<a href="#">Figure 5</a>
$V_{OM+}$	Maximum positive peak output voltage	vs Supply voltage	<a href="#">Figure 6</a>
		vs Free-air temperature	<a href="#">Figure 7</a>
		vs Output current	<a href="#">Figure 8</a>
		vs Settling time	<a href="#">Figure 10</a>
$V_{OM-}$	Maximum negative peak output voltage	vs Supply voltage	<a href="#">Figure 6</a>
		vs Free-air temperature	<a href="#">Figure 7</a>
		vs Output current	<a href="#">Figure 9</a>
		vs Settling time	<a href="#">Figure 10</a>
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	<a href="#">Figure 11</a>
$V_{OH}$	High-level output voltage	vs Output current	<a href="#">Figure 12</a>
$V_{OL}$	Low-level output voltage	vs Output current	<a href="#">Figure 13</a>
	Phase shift	vs Frequency	<a href="#">Figure 14</a>
$A_{VD}$	Large-signal differential voltage amplification	vs Frequency	<a href="#">Figure 14</a>
		vs Free-air temperature	<a href="#">Figure 15</a>
$z_o$	Closed-loop output impedance	vs Frequency	<a href="#">Figure 16</a>
$I_{OS}$	Short-circuit output current	vs Free-air temperature	<a href="#">Figure 17</a>
CMRR	Common-mode rejection ratio	vs Frequency	<a href="#">Figure 18</a>
		vs Free-air temperature	<a href="#">Figure 19</a>
$k_{SVR}$	Supply-voltage rejection ratio	vs Frequency	<a href="#">Figure 20</a>
		vs Free-air temperature	<a href="#">Figure 21</a>
$I_{CC}$	Supply current	vs Supply voltage	<a href="#">Figure 22</a>
		vs Free-air temperature	<a href="#">Figure 23</a>
$V_n$	Equivalent input noise voltage	vs Frequency	<a href="#">Figure 24</a>
$V_n$	Input noise voltage	Over a 10-second period	<a href="#">Figure 25</a>
$I_n$	Noise current	vs Frequency	<a href="#">Figure 26</a>
THD+N	Total harmonic distortion plus noise	vs Frequency	<a href="#">Figure 27</a>
SR	Slew rate	vs Free-air temperature	<a href="#">Figure 28</a>
		vs Load capacitance	<a href="#">Figure 29</a>
	Pulse response	Noninverting large signal	vs Time <a href="#">Figure 30</a>
		Inverting large signal	vs Time <a href="#">Figure 31</a>
		Small signal	vs Time <a href="#">Figure 32</a>
$B_1$	Unity-gain bandwidth	vs Load capacitance	<a href="#">Figure 33</a>
	Gain margin	vs Load capacitance	<a href="#">Figure 34</a>
$\phi_m$	Phase margin	vs Load capacitance	<a href="#">Figure 35</a>

**TLE2141  
DISTRIBUTION OF  
INPUT OFFSET VOLTAGE**

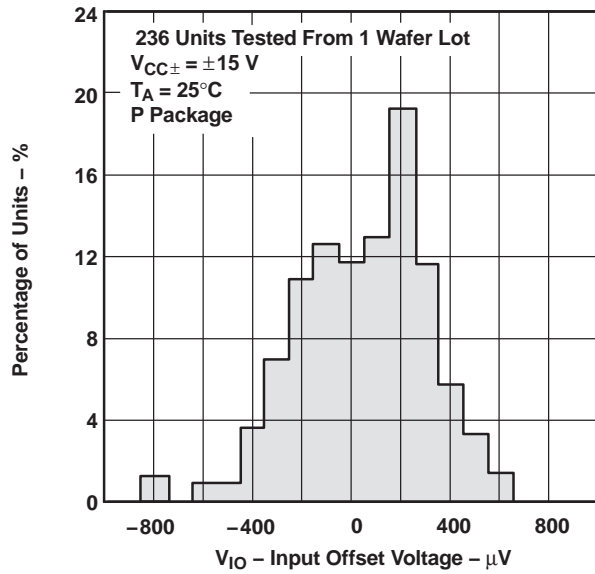


Figure 2.

**INPUT OFFSET CURRENT  
vs  
FREE-AIR TEMPERATURE**

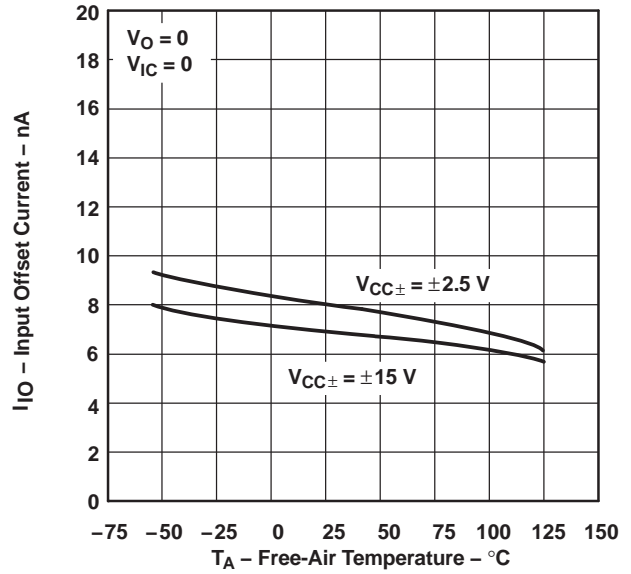


Figure 3.

**INPUT BIAS CURRENT  
vs  
COMMON-MODE INPUT VOLTAGE**

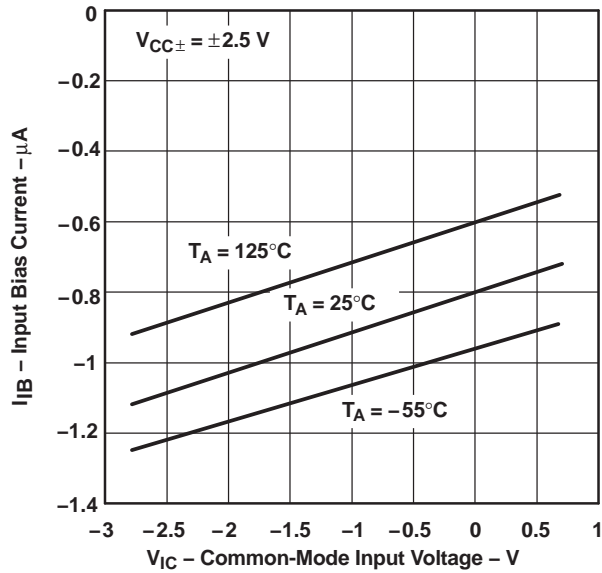


Figure 4.

**INPUT BIAS CURRENT  
vs  
FREE-AIR TEMPERATURE**

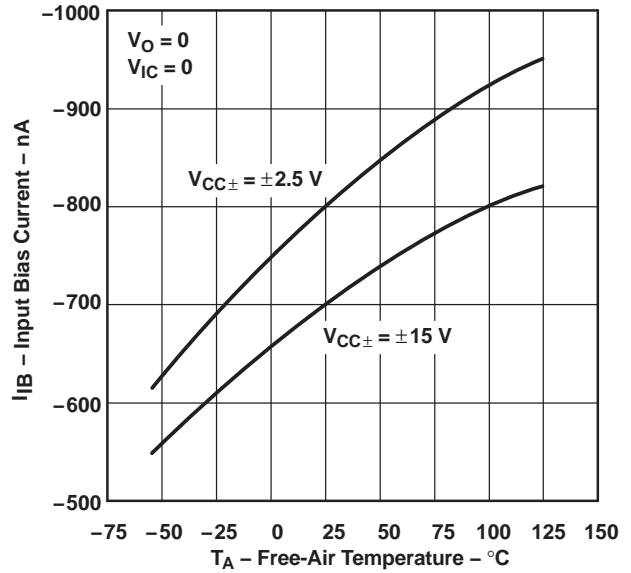


Figure 5.

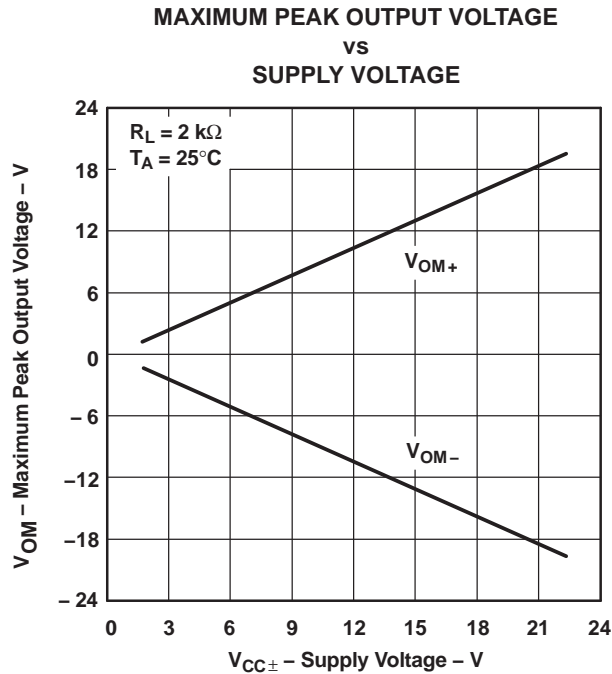


Figure 6.

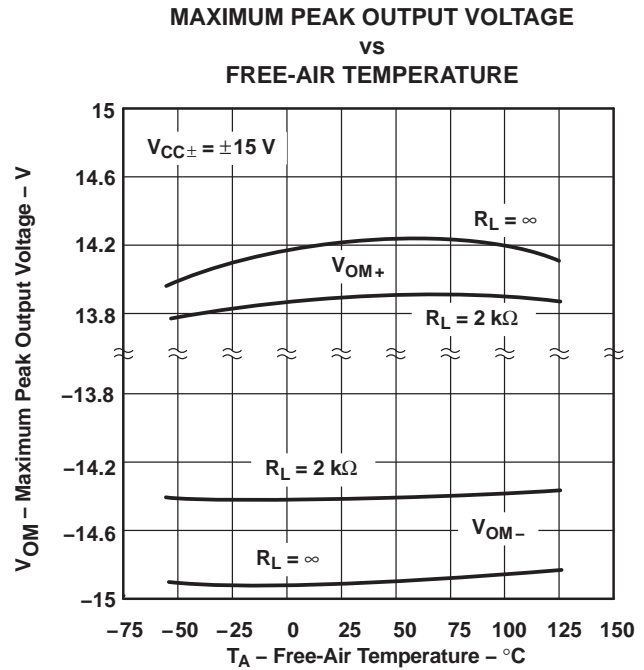


Figure 7.

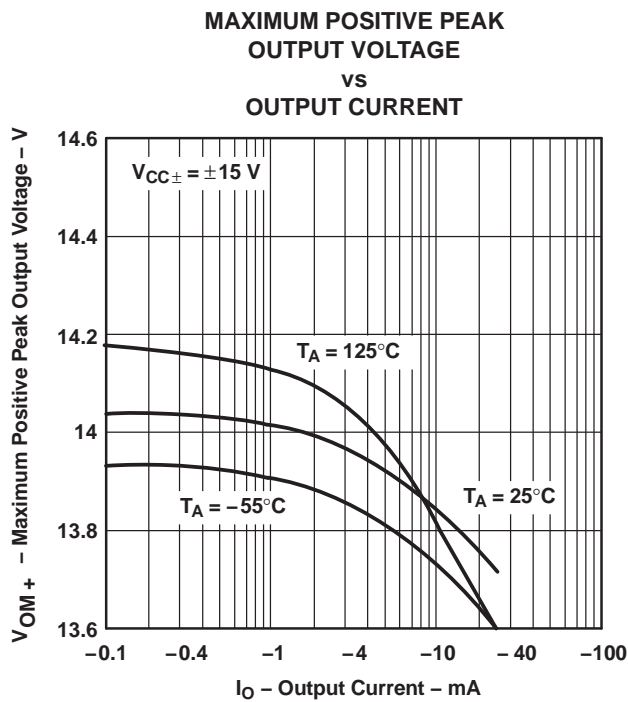


Figure 8.

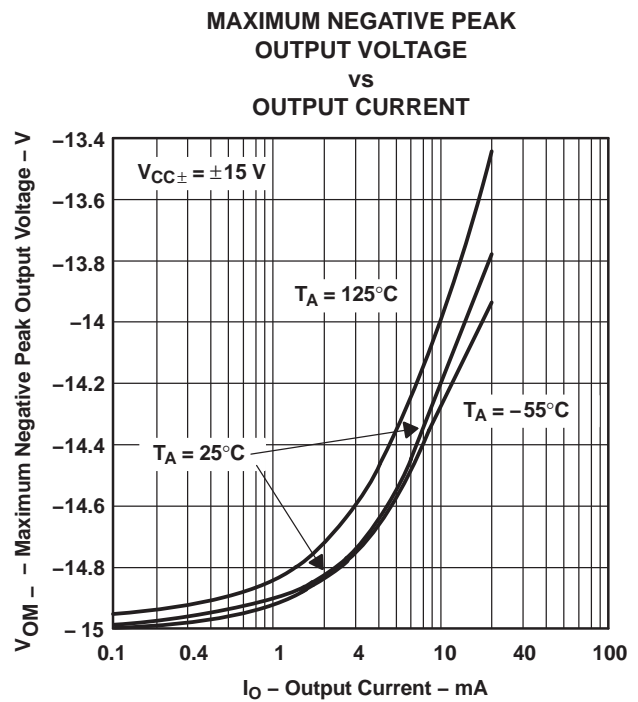


Figure 9.

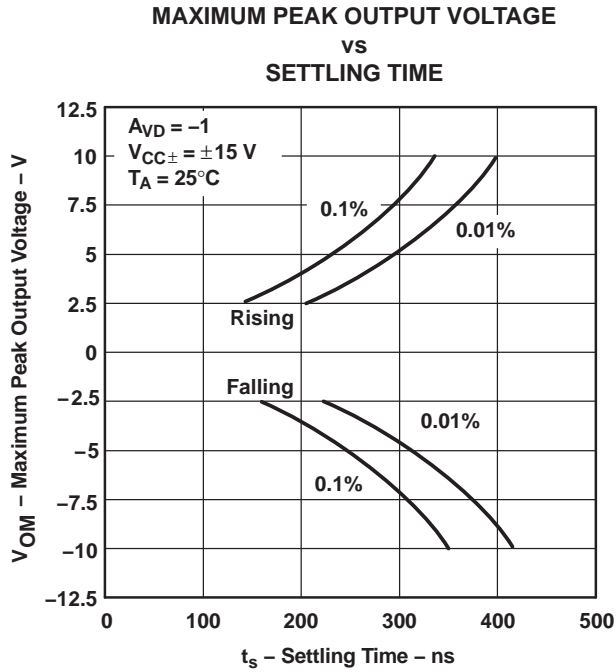


Figure 10.

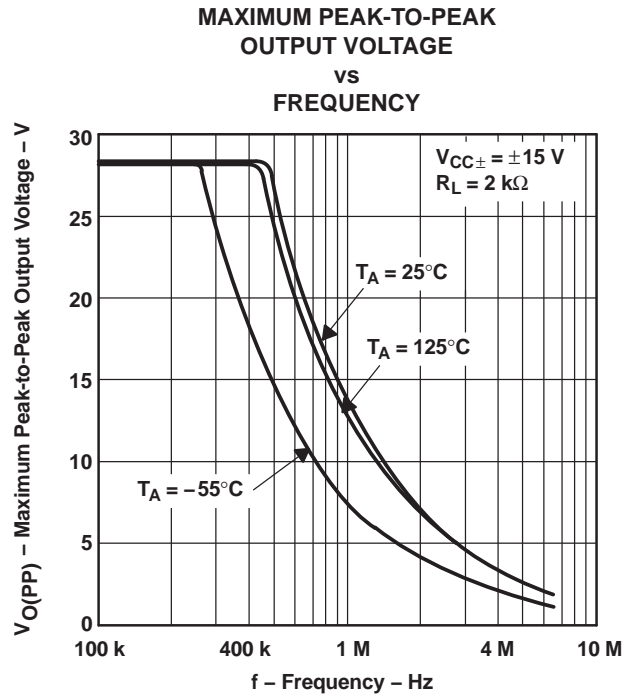


Figure 11.

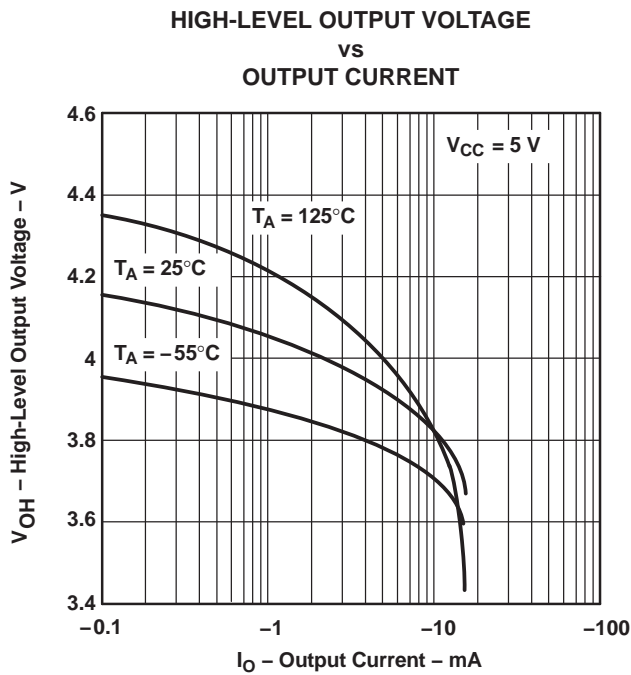


Figure 12.

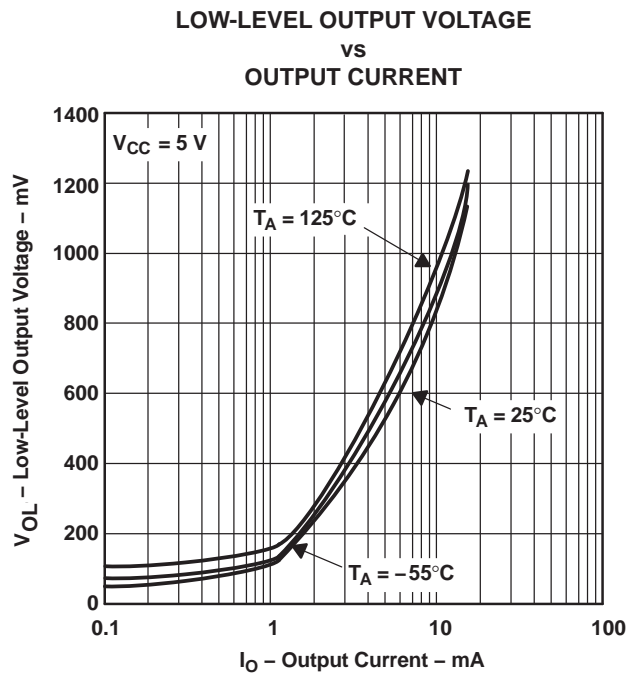


Figure 13.

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT VS FREQUENCY

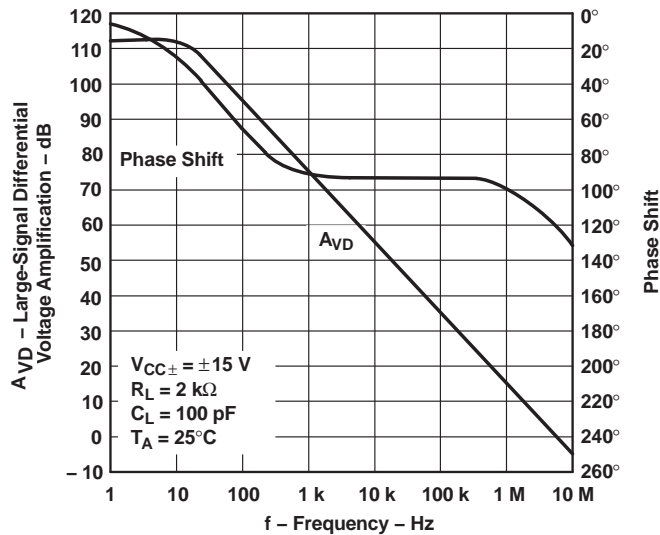


Figure 14.

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION VS FREE-AIR TEMPERATURE

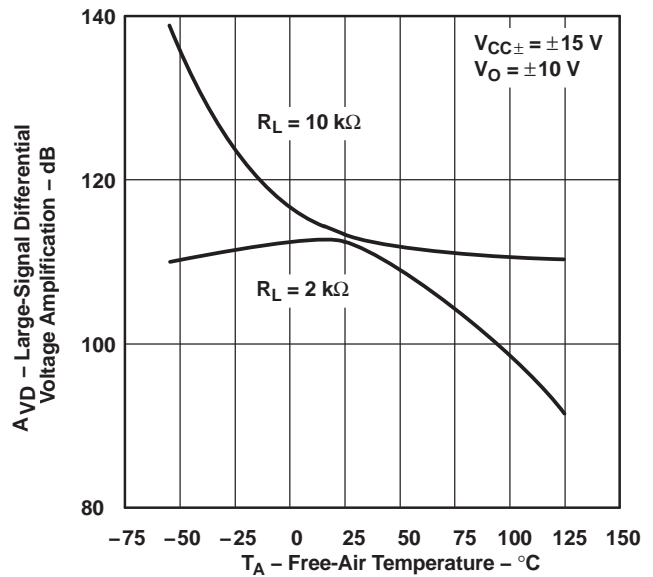


Figure 15.

CLOSED-LOOP OUTPUT IMPEDANCE VS FREQUENCY

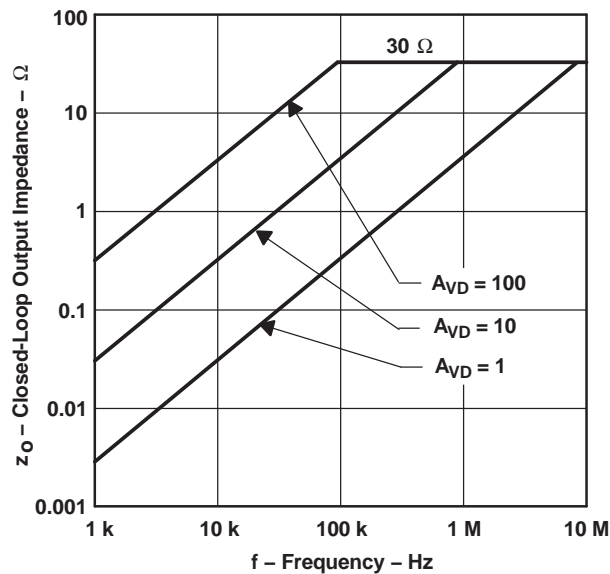


Figure 16.

SHORT-CIRCUIT OUTPUT CURRENT VS FREE-AIR TEMPERATURE

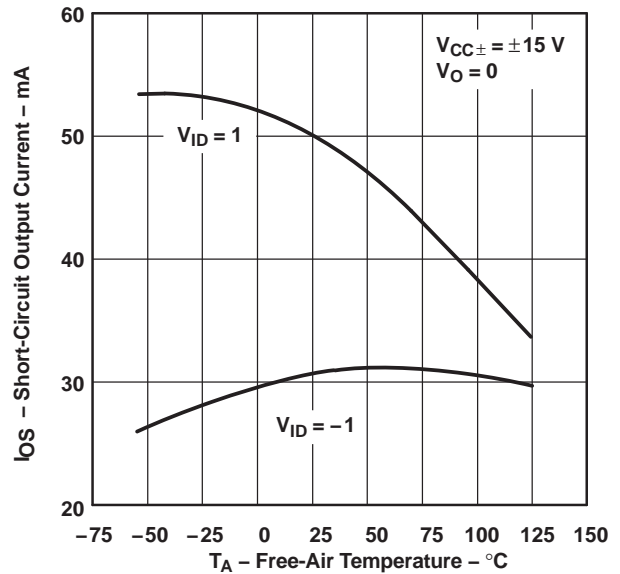
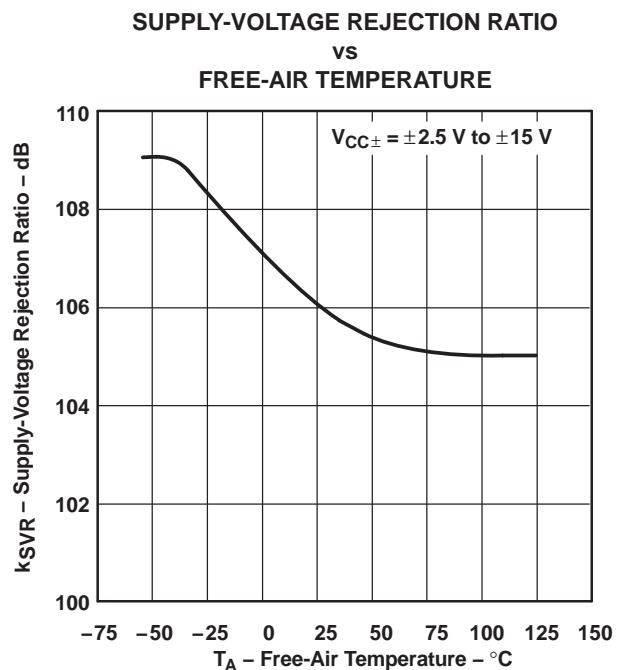
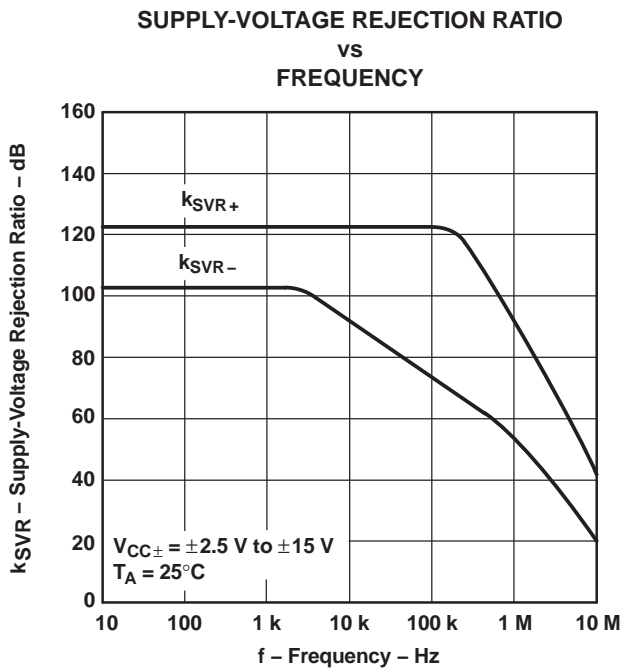
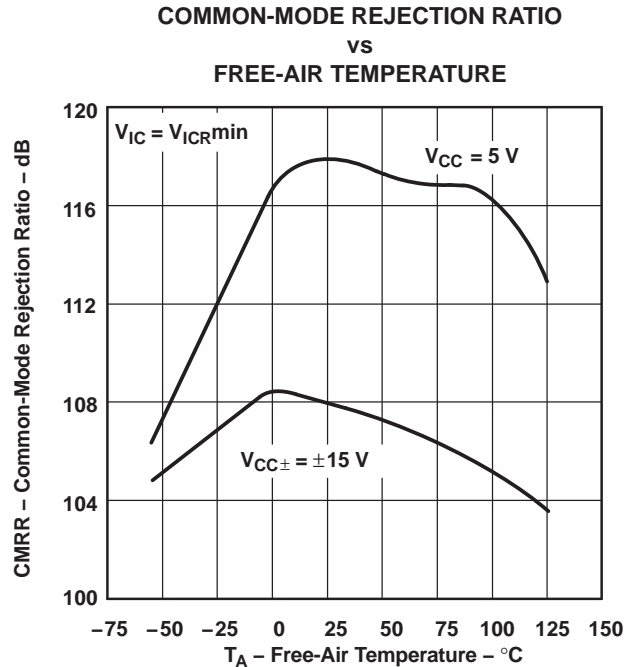
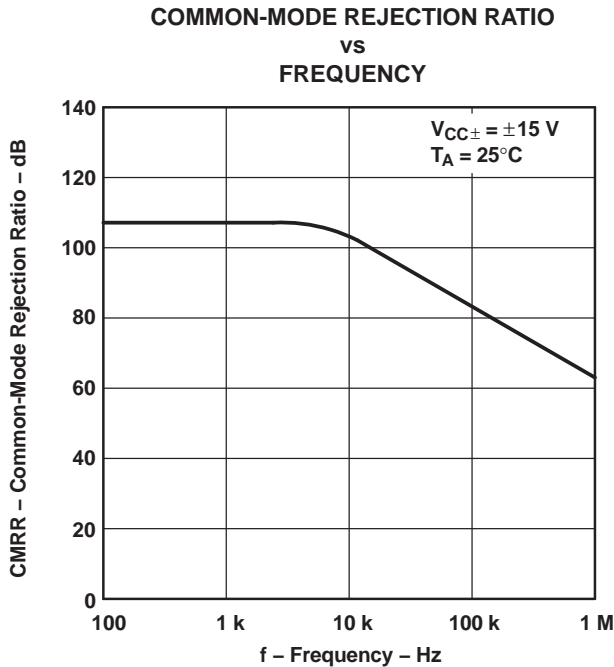


Figure 17.



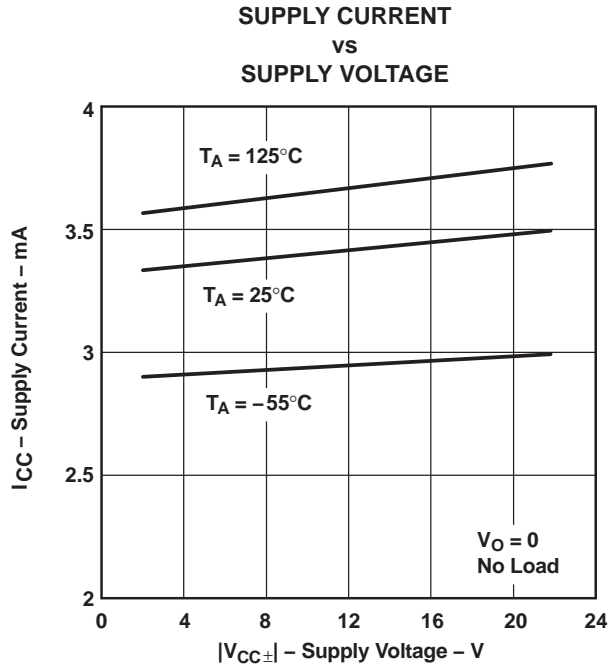


Figure 22.

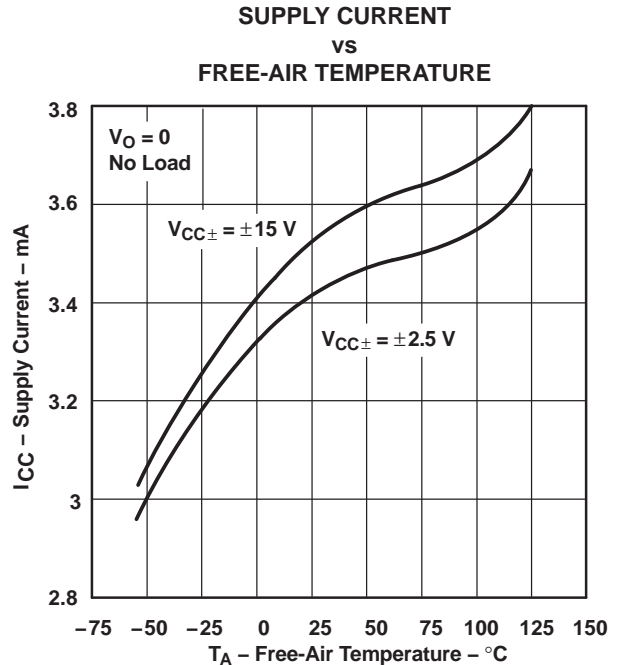


Figure 23.

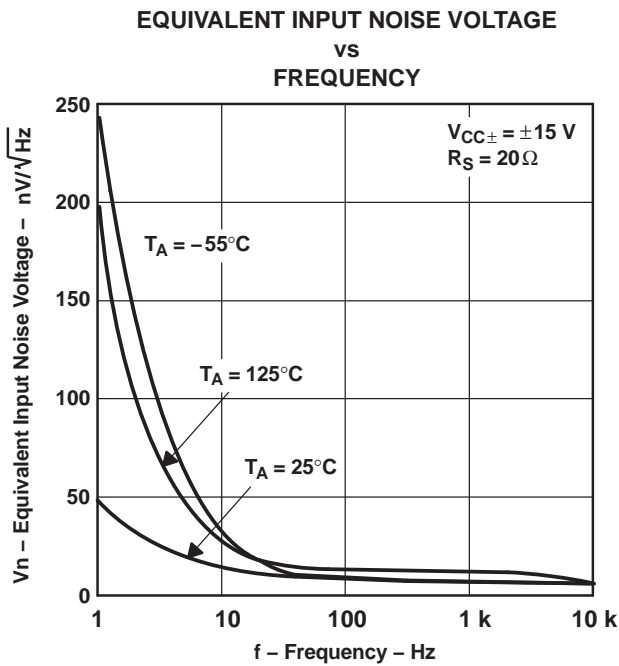


Figure 24.

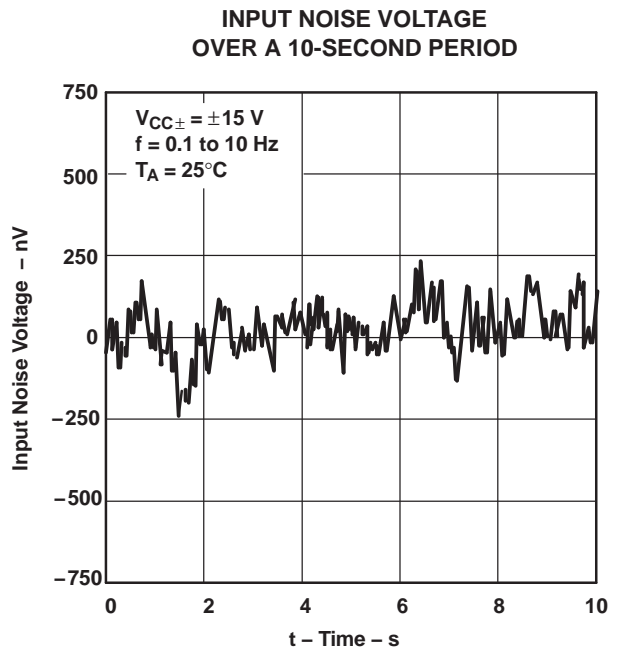


Figure 25.

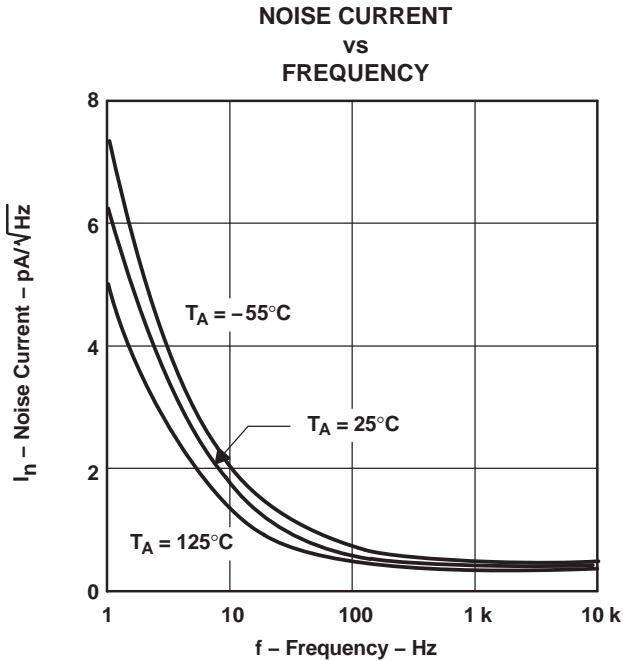


Figure 26.

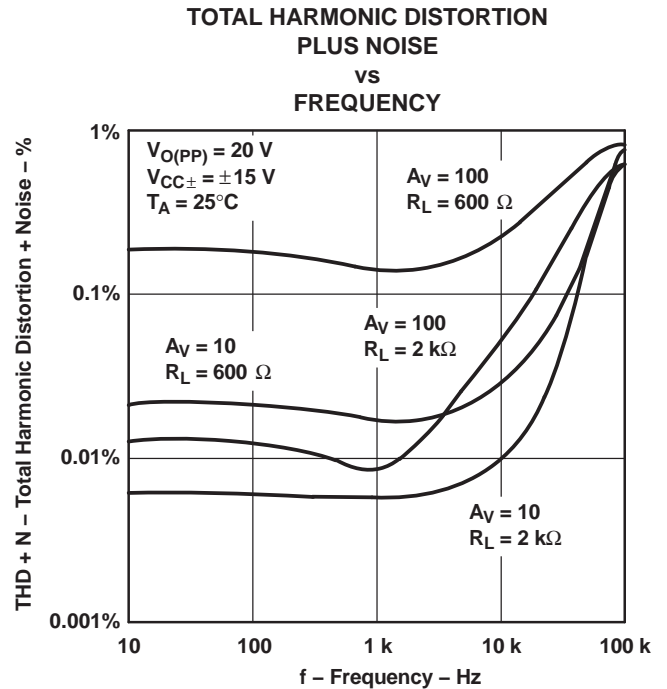


Figure 27.

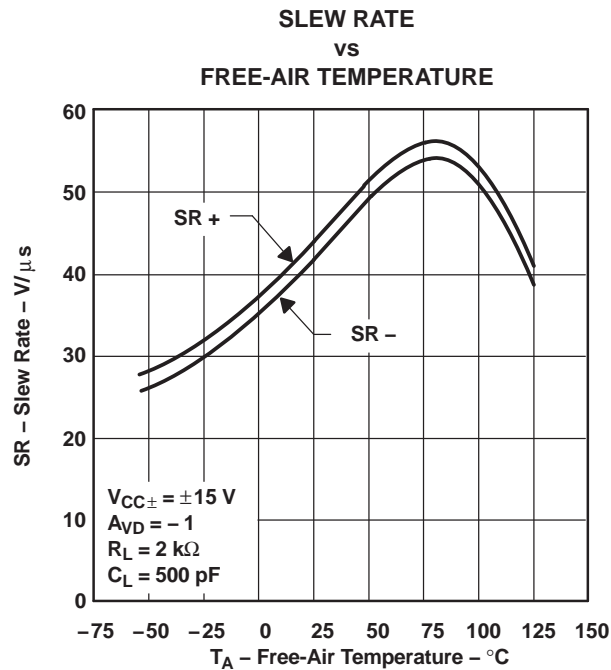


Figure 28.

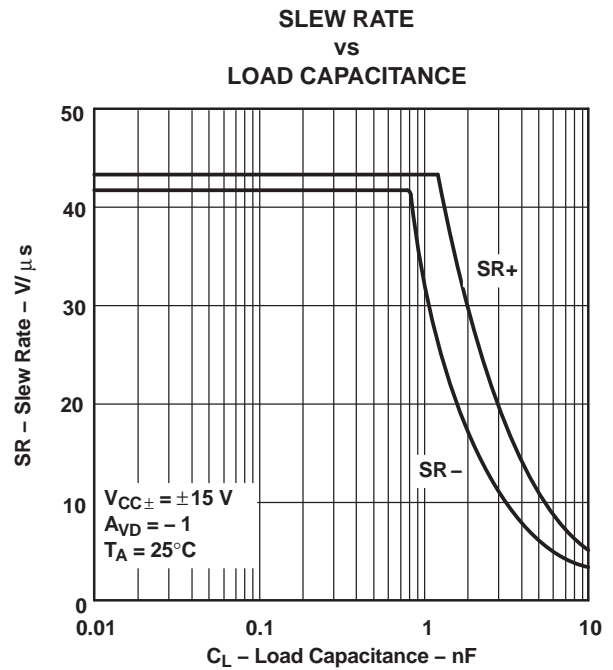


Figure 29.



**NONINVERTING  
LARGE-SIGNAL  
PULSE RESPONSE**

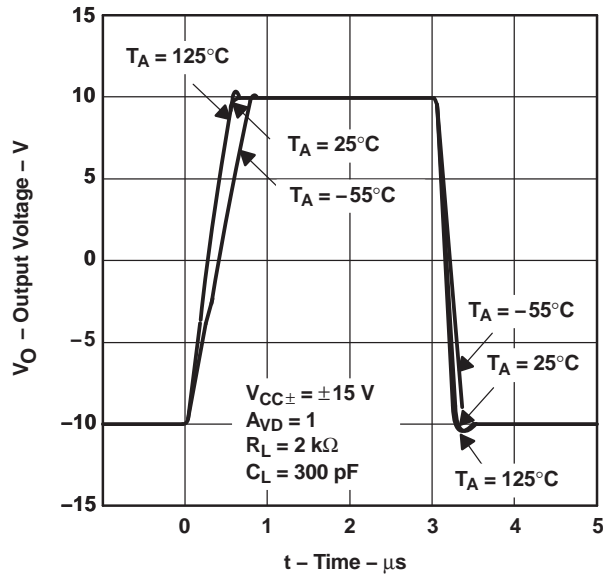


Figure 30.

**INVERTING  
LARGE-SIGNAL  
PULSE RESPONSE**

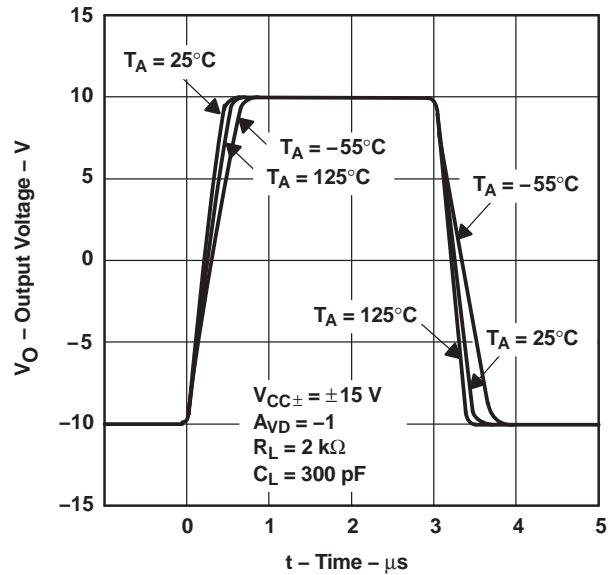


Figure 31.

**SMALL-SIGNAL  
PULSE RESPONSE**

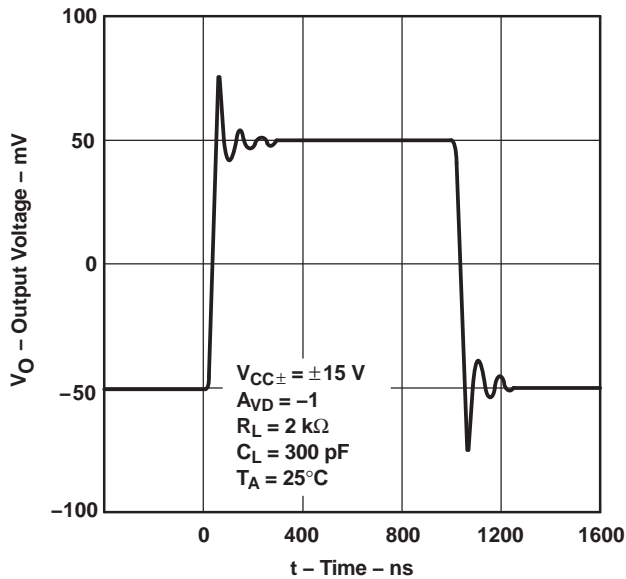


Figure 32.

**UNITY-GAIN BANDWIDTH  
vs  
LOAD CAPACITANCE**

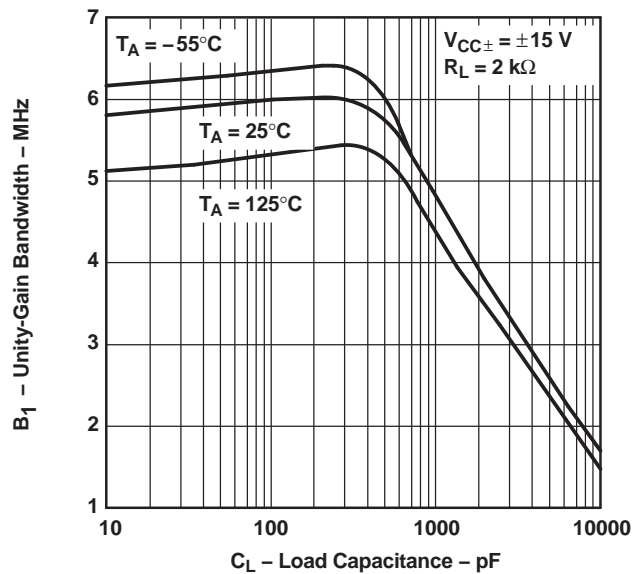


Figure 33.

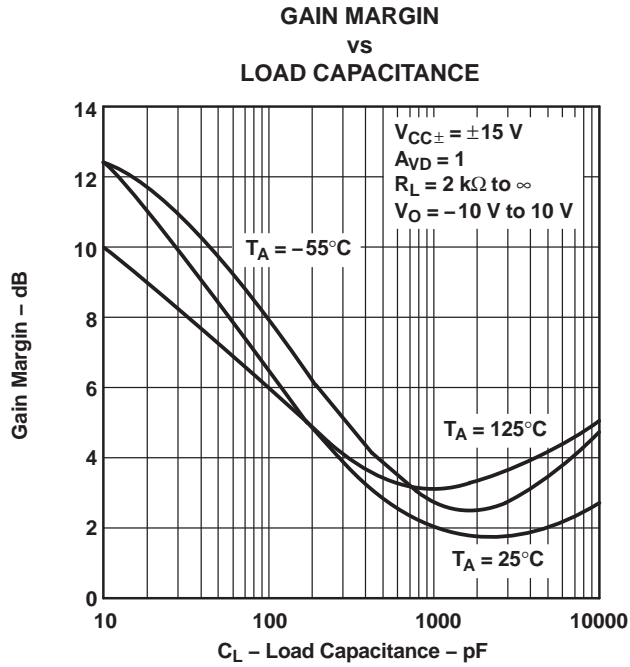


Figure 34.

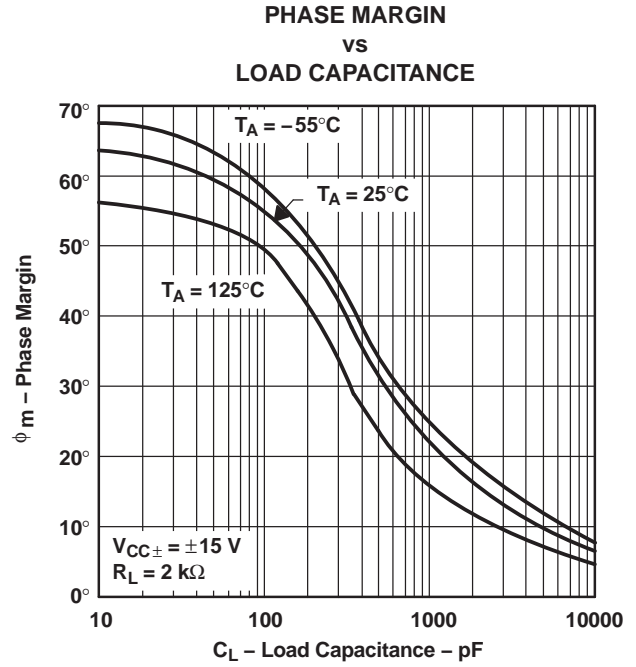


Figure 35.

## APPLICATION INFORMATION

### Input Offset Voltage Nulling

The TLE2141-Q1 offers external null pins that can be used to further reduce the input offset voltage. If this feature is desired, connect the circuit of [Figure 36](#) as shown. If external nulling is not needed, the null pins may be left unconnected.

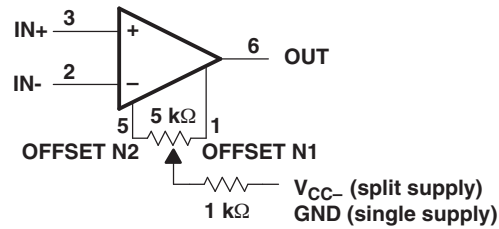


Figure 36. Input Offset Voltage Null Circuit

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLE2141QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2141Q	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF TLE2141-Q1 :**

- Catalog: [TLE2141](#)
- Enhanced Product: [TLE2141-EP](#)
- Military: [TLE2141M](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

## NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



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