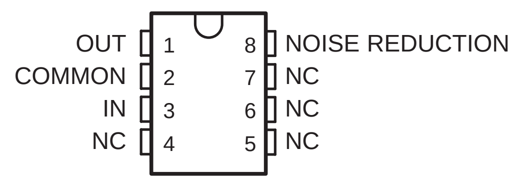
- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Extended Temperature Performance of −55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree**†
- **One-Half V_I Virtual Ground for Analog Systems**
- **Micropower Operation . . . 170 µA Typ, V_I = 5 V**
- **Wide V_I Range . . . 4 V to 40 V**
- **High Output-Current Capability**
  - **Source . . . 20 mA Typ**
  - **Sink . . . 20 mA Typ**
- **Excellent Output Regulation**
  - **−102 µV Typ at I_O = 0 mA to −10 mA**
  - **49 µV Typ at I_O = 0 mA to 10 mA**
- **Low-Impedance Output . . . 0.0075 Ω Typ**
- **Noise Reduction Pin**

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

D PACKAGE
(TOP VIEW)



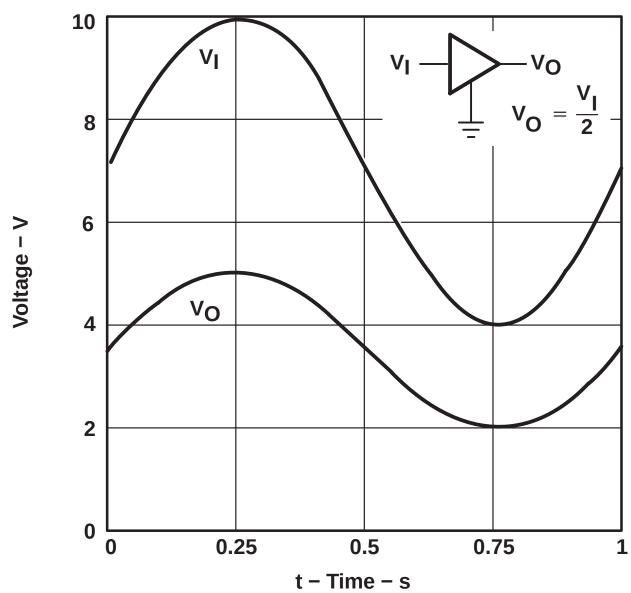
NC − No internal connection

description/ordering information

In signal-conditioning applications utilizing a single power source, a reference voltage equal to one-half the supply voltage is required for termination of all analog signal grounds. TI presents a precision virtual ground whose output voltage is always equal to one-half the input voltage—the TLE2426 rail splitter.

The unique combination of a high-performance, micropower operational amplifier and a precision-trimmed divider on a single silicon chip results in a precise V_O/V_I ratio of 0.5 while sinking and sourcing current. The TLE2426 provides a low-impedance output with 20 mA of sink and source capability, while drawing less than 280 µA of supply current over the full input range of 4 V to 40 V. A designer need not pay the price in terms of board space for a conventional signal ground consisting of resistors, capacitors, operational amplifiers, and voltage references. For increased performance, the 8-pin package provides a noise-reduction pin. With the addition of an external capacitor (C_{NR}), peak-to-peak noise is reduced, while line ripple rejection is improved.

INPUT/OUTPUT TRANSFER CHARACTERISTICS



Initial output tolerance for a single 5-V or 12-V system is better than 1% over the full 40-V input range. Ripple rejection exceeds 12 bits of accuracy. Whether the application is for a data-acquisition front end, analog signal termination, or simply a precision voltage reference, the TLE2426 eliminates a major source of system error.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−55°C to 125°C	SOIC (D)	Tape and reel	TLE2426MDREP	2426EP

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

- Continuous input voltage, V_I . . . . . 40 V
- Continuous filter trap voltage . . . . . 40 V
- Output current, I_O . . . . . ±80 mA
- Duration of short-circuit current at (or below) 25°C (see Note 1) . . . . . Unlimited
- Continuous total power dissipation . . . . . See Dissipation Rating Table
- Operating free-air temperature range, T_A . . . . . −55°C to 125°C
- Operating junction temperature, T_J (see Note 2) . . . . . 150°C
- Storage temperature range, T_{stg} (see Note 2) . . . . . 150°C
- Lead temperature 1,6 mm (1/16 in) from case for 10 s . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.
2. Long-term high-temperature storage and/or usage at the absolute maximum ratings may result in a reduction of overall device life. See http://www.ti.com/ep_quality for additional information on enhanced plastic packaging.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D	1102 mV	10.3 mW/°C	638.5 mW	484 mW	72.1 mW

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, V_I	4	40	V
Operating free-air temperature, T_A	−55	125	°C

electrical characteristics at specified free-air temperature, V_I = 5 V, I_O = 0 (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
Output voltage	V_I = 4 V		25°C	1.98	2	2.02	V
	V_I = 5 V			2.48	2.5	2.52	
	V_I = 40 V			19.8	20	20.2	
	V_I = 5 V		Full range	2.465		2.535	
Temperature coefficient of output voltage			Full range		25		ppm/°C
Supply current	No load	V_I = 5 V	25°C		170	300	µA
		V_I = 4 to 40 V	25°C			350	
			Full range			400	
Output voltage regulation (sourcing current)‡	I_O = 0 to −10 mA		25°C		−0.102	±0.7	mV
			Full range			±10	
	I_O = 0 to −20 mA		25°C		−0.121	±1.4	
Output voltage regulation (sinking current)‡	I_O = 0 to 10 mA		25°C		0.049	±0.5	mV
	I_O = 0 to 8 mA		Full range			±10	
	I_O = 0 to 20 mA		25°C		0.175	±1.4	
Output impedance‡			25°C		7.5	22.5	mΩ
Noise-reduction impedance			25°C		110		kΩ
Short-circuit current	Sinking current, V_O = 5 V		25°C		26		mA
	Sourcing current, V_O = 0				−47		
Output noise voltage, rms	f = 10 Hz to 10 kHz	C_{NR} = 0	25°C		120		µV
		C_{NR} = 1 µF			30		
Output voltage current step response	V_O to 0.1%, I_O = ±10 mA	C_L = 0	25°C		290		µs
		C_L = 100 pF			275		
	V_O to 0.01%, I_O = ±10 mA	C_L = 0	25°C		400		
		C_L = 100 pF			390		
Step response	V_I = 0 to 5 V, V_O to 0.1%	C_L = 100 pF	25°C		20		µs
	V_I = 0 to 5 V, V_O to 0.01%				120		

† Full range is −55°C to 125°C.
‡ The listed values are not production tested.

electrical characteristics at specified free-air temperature, V_I = 12 V, I_O = 0 (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
Output voltage	V_I = 4 V		25°C	1.98	2	2.02	V
	V_I = 12 V			5.95	6	6.05	
	V_I = 40 V			19.8	20	20.2	
	V_I = 12 V		Full range	5.925		6.075	
Temperature coefficient of output voltage			Full range		35		ppm/°C
Supply current	No load	V_I = 12 V	25°C		195	300	μA
		V_I = 4 to 40 V	25°C			350	
			Full range			400	
Output voltage regulation (sourcing current)‡	I_O = 0 to −10 mA		25°C		−1.48	±10	mV
			Full range			±10	
	I_O = 0 to −20 mA		25°C		−3.9	±10	
Output voltage regulation (sinking current)‡	I_O = 0 to 10 mA		25°C		2.27	±10	mV
	I_O = 0 to 8 mA		Full range			±10	
	I_O = 0 to 20 mA		25°C		4.3	±10	
Output impedance‡			25°C		7.5	22.5	mΩ
Noise-reduction impedance			25°C		110		kΩ
Short-circuit current	Sinking current, V_O = 12 V		25°C		31		mA
	Sourcing current, V_O = 0				−70		
Output noise voltage, rms	f = 10 Hz to 10 kHz	C_{NR} = 0	25°C		120		μV
		C_{NR} = 1 μF			30		
Output voltage current step response	V_O to 0.1%, I_O = ±10 mA	C_L = 0	25°C		290		μs
		C_L = 100 pF			275		
	V_O to 0.01%, I_O = ±10 mA	C_L = 0	25°C		400		
		C_L = 100 pF			390		
Step response	V_I = 0 to 12 V, V_O to 0.1%	C_L = 100 pF	25°C		12		μs
	V_I = 0 to 12 V, V_O to 0.01%				120		

† Full range is −55°C to 125°C.
‡ The listed values are not production tested.

TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE
Output voltage	Distribution	1, 2
Output voltage change	vs Free-air temperature	3
Output voltage error	vs Input voltage	4
Input bias current	vs Input voltage	5
	vs Free-air temperature	6
Output voltage regulation	vs Output current	7
Output impedance	vs Frequency	8
Short-circuit output current	vs Input voltage	9, 10
	vs Free-air temperature	11, 12
Ripple rejection	vs Frequency	13
Spectral noise voltage density	vs Frequency	14
Output voltage response to output current step	vs Time	15
Output voltage power-up response	vs Time	16
Output current	vs Load capacitance	17

TYPICAL CHARACTERISTICS†

DISTRIBUTION
OF
OUTPUT VOLTAGE

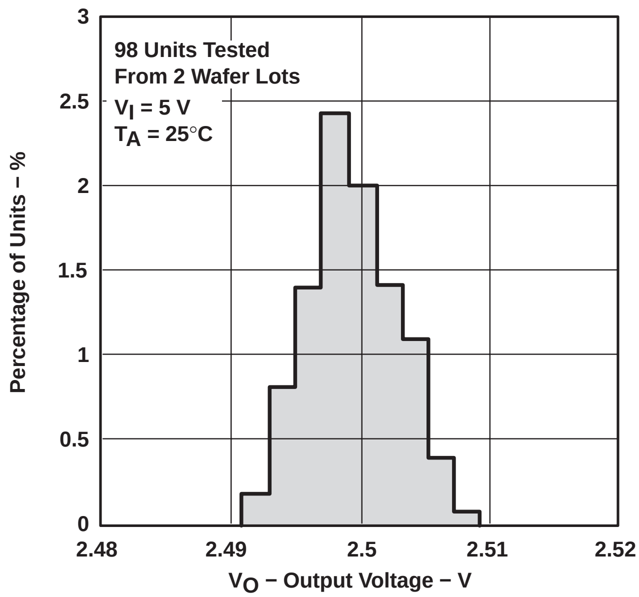


Figure 1

DISTRIBUTION
OF
OUTPUT VOLTAGE

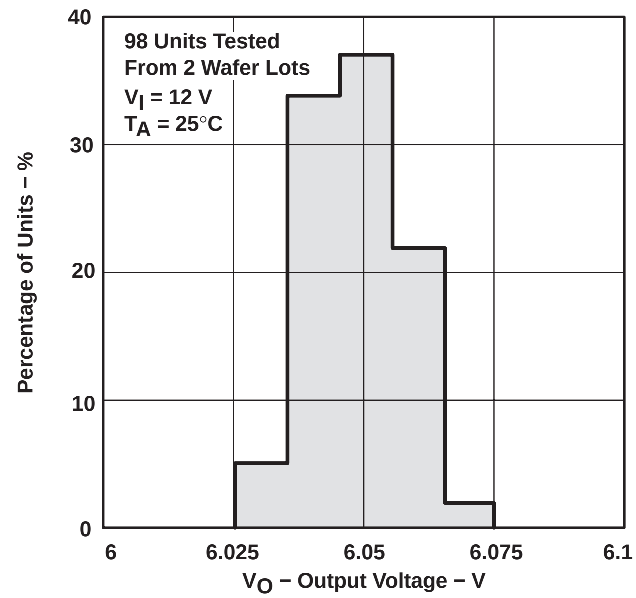


Figure 2

OUTPUT VOLTAGE CHANGE
vs
FREE-AIR TEMPERATURE

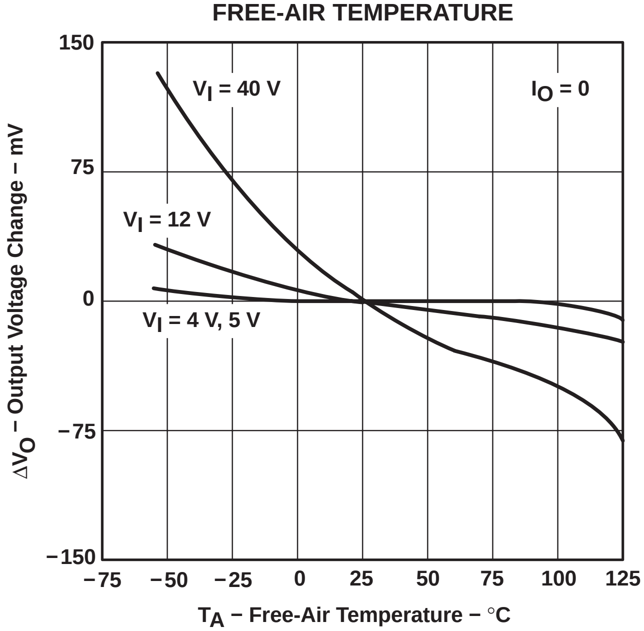


Figure 3

OUTPUT VOLTAGE ERROR
vs
INPUT VOLTAGE

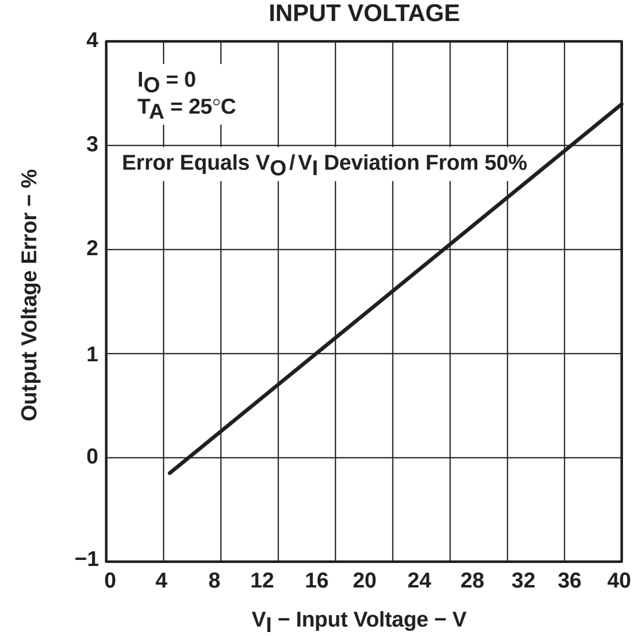


Figure 4

† Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

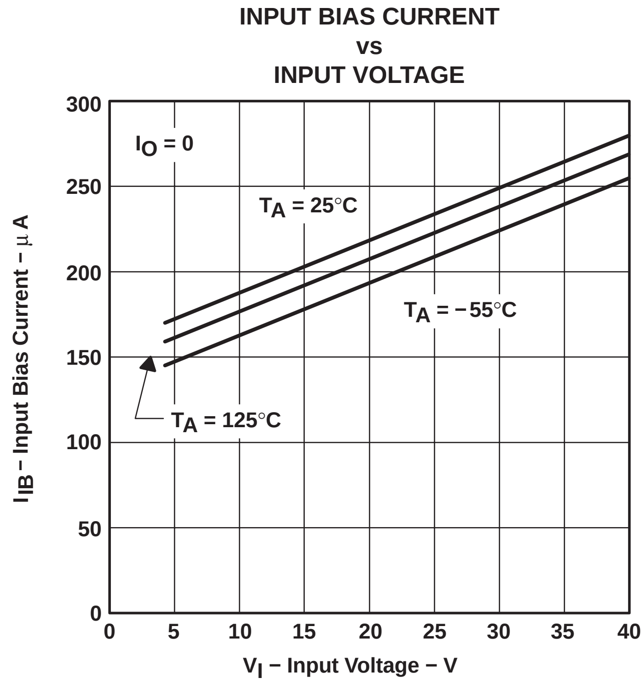


Figure 5

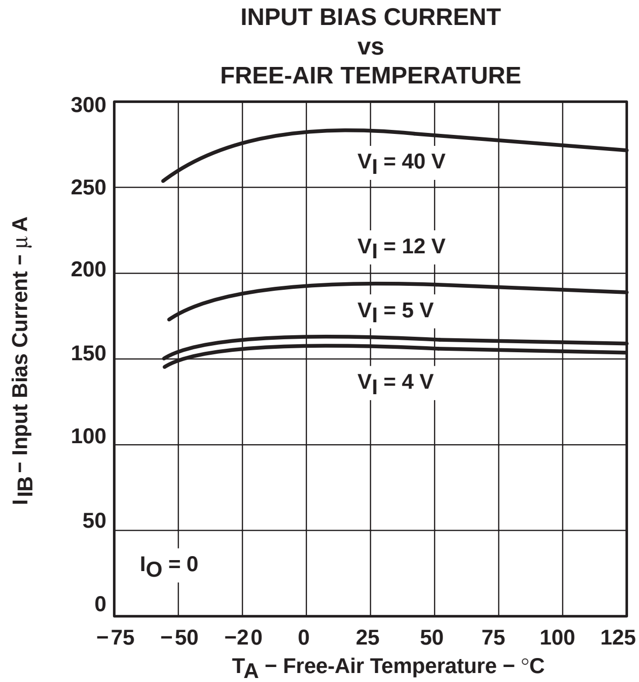


Figure 6

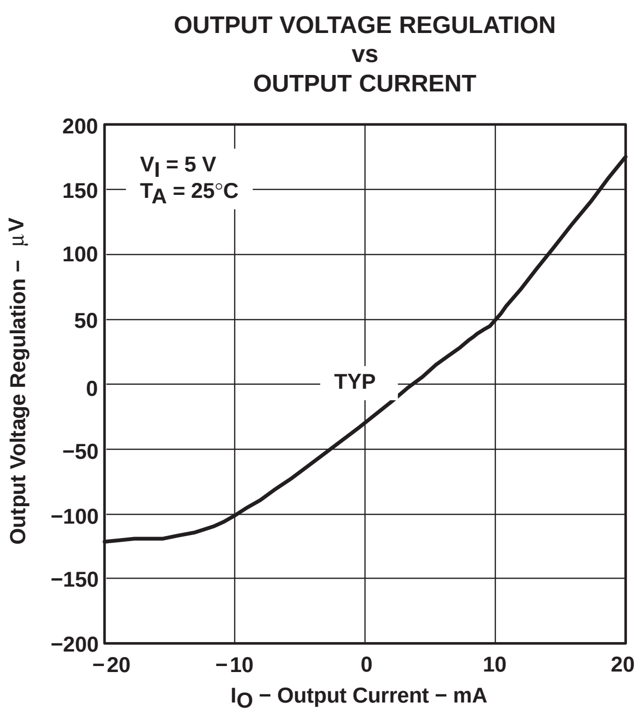


Figure 7

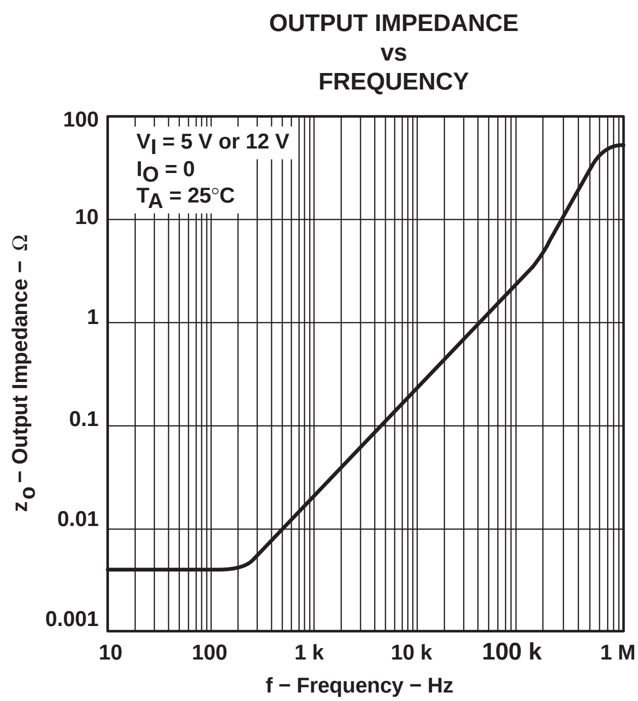


Figure 8

† Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SHORT-CIRCUIT OUTPUT CURRENT
vs
INPUT VOLTAGE

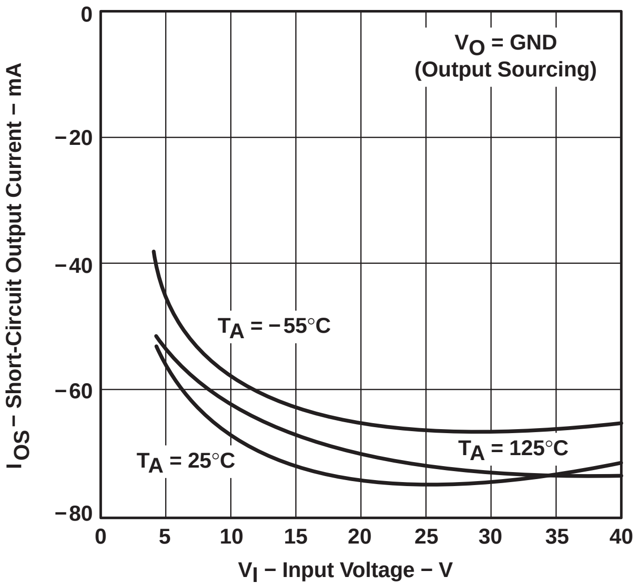


Figure 9

SHORT-CIRCUIT OUTPUT CURRENT
vs
INPUT VOLTAGE

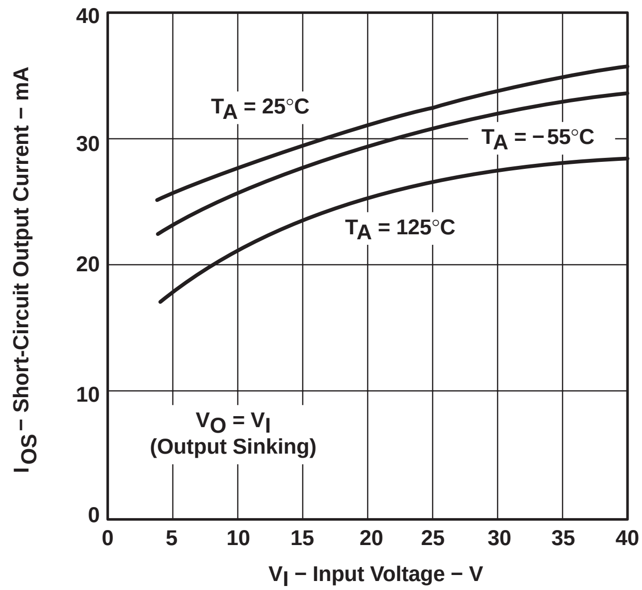


Figure 10

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

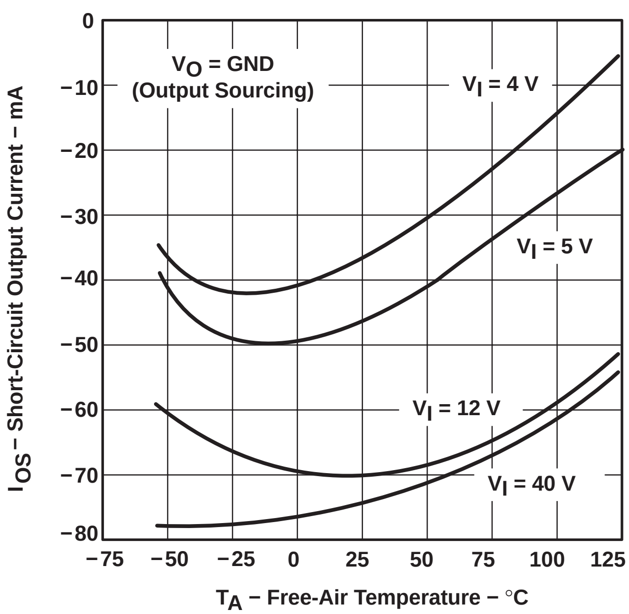


Figure 11

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

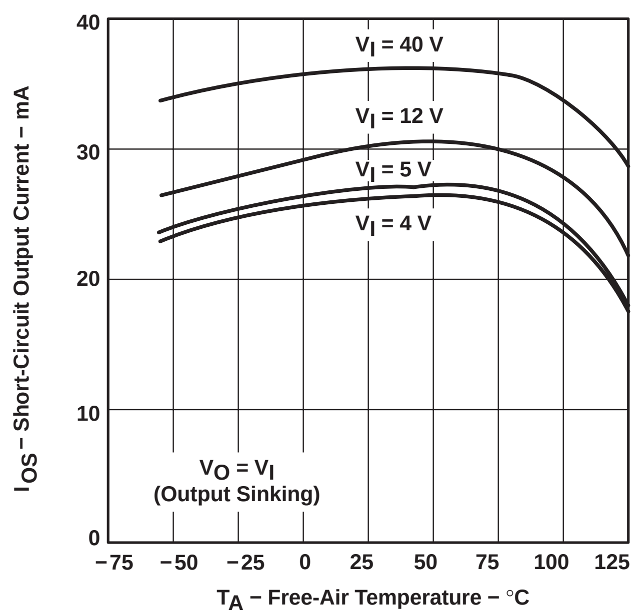


Figure 12

† Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

RIPPLE REJECTION vs FREQUENCY

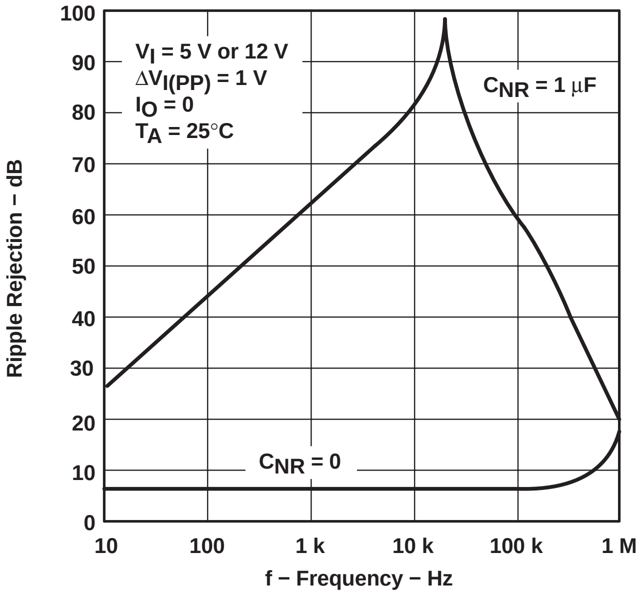


Figure 13

SPECTRAL NOISE VOLTAGE DENSITY vs FREQUENCY

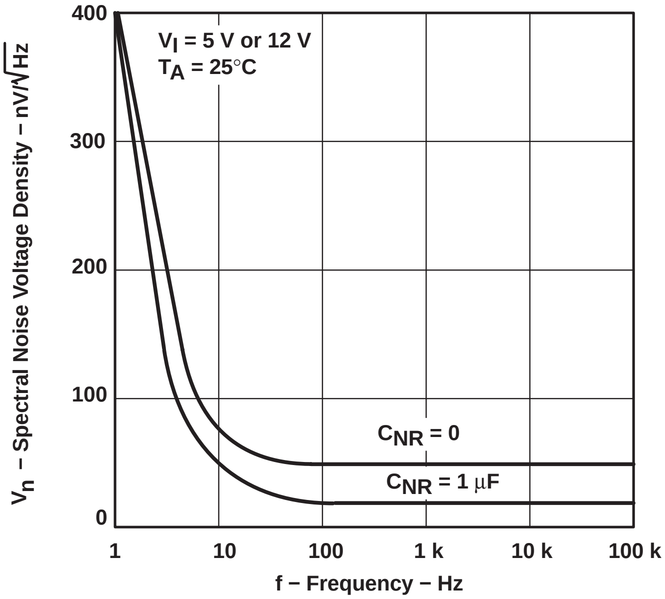


Figure 14

OUTPUT VOLTAGE RESPONSE TO OUTPUT CURRENT STEP

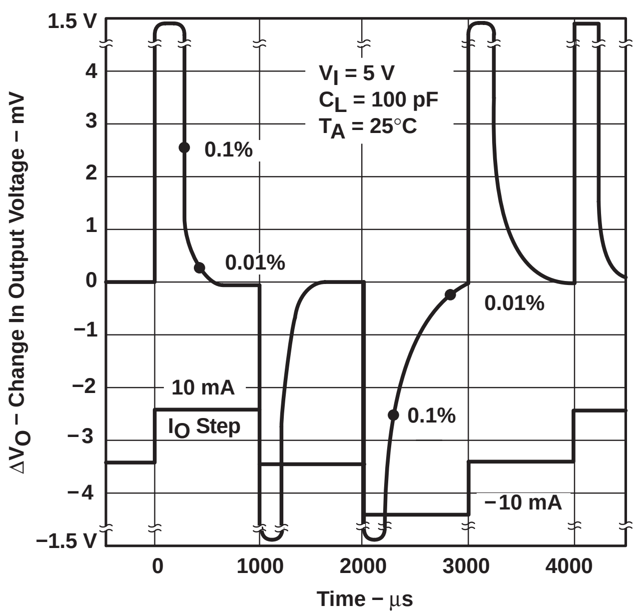


Figure 15

OUTPUT VOLTAGE POWER-UP RESPONSE

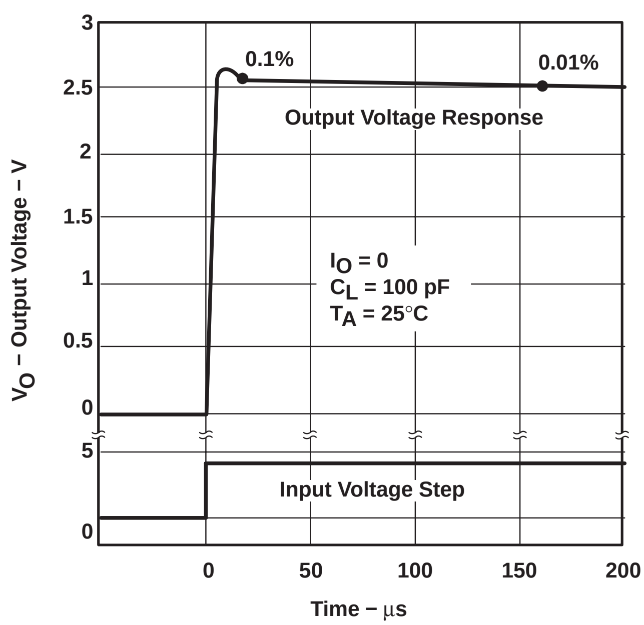


Figure 16

TYPICAL CHARACTERISTICS

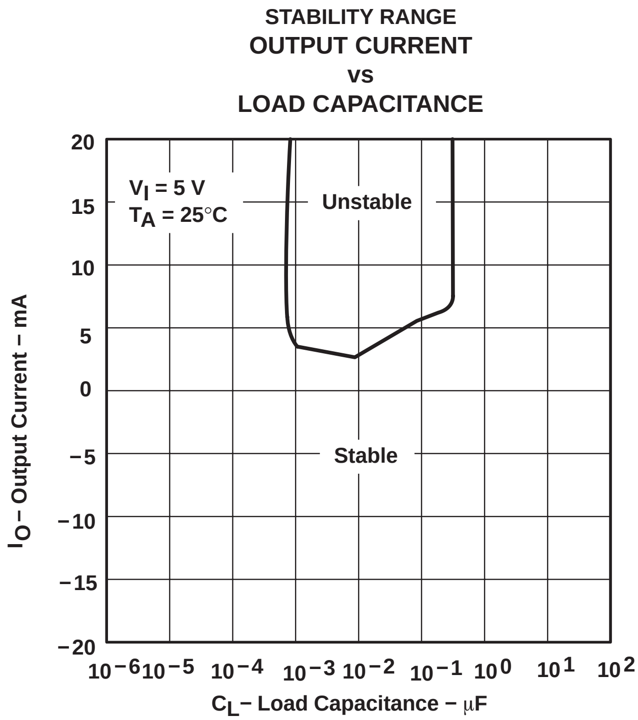


Figure 17

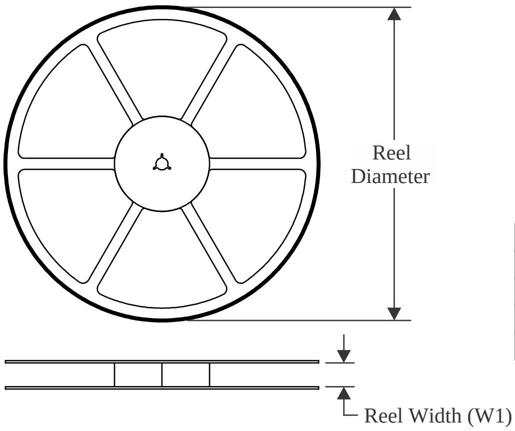
MACROMODEL INFORMATION

```
*   TLE2426 OPERATIONAL AMPLIFIER “MACROMODEL” SUBCIRCUIT
*   CREATED USING PARTS RELEASE 4.03 0N 08/21/90 AT 13:51
*   REV (N/A)     SUPPLY VOLTAGE: 5 V
*   CONNECTIONS:     FILTER
                     |   INPUT
*                    |   |   COMMON
*                    |   |   |   OUTPUT
*                    |   |   |   |
.SUBCKT TLE2426      1   3   4   5
```

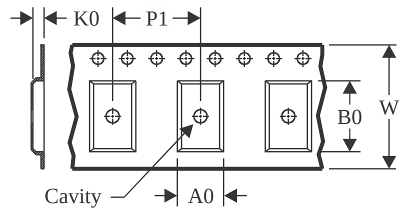
```
   C1      11  12  21.66E-12
   C2       6   7  30.00E-12
   C3      87   0  10.64E-9
   CPSR    85  86  15.9E-9
   DCM+    81  82  DX
   DCM-    83  81  DX
   DC       5  53  DX
   DE      54   5  DX
   DLP     90  91  DX
   DLN     92  90  DX
   DP       4   3  DX
   ECMR    84  99  (2,99) 1
   EGND    99   0  POLY(2)   (3,0) (4,0)   0   .5  .5
   EPSR    85   0  POLY(1)   (3,4)  -16.22E-6 3.24E-6
   ENSE    89   2  POLY(1)   (88,0) 120E-6 1
   FB       7  99  POLY(6)   VB  VC  VE  VLP VLN VPSR 0 74.8E6 -10E6  10E6   10E6   -10E6  74E6
   GA       6   0  11  12  320.4E-6
   GCM      0   6  10  99  1.013E-9
   GPSR    85  86  (85,86)   100E-6
   GRC1     4  11  (4,11) 3.204E-4
   GRC2     4  12  (4,12) 3.204E-4
   GRE1    13  10  (13,10)   1.038E-3
   GRE2    14  10  (14,10)   1.038E-3
   HLIM    90   0  VLIM   1K
   HCMR    80   1  POLY(2)   VCM+   VCM-   0   1E2    1E2
   IRP      3   4  146E-6
   IEE      3  10  DC  24.05E-6
   IIO      2   0  .2E-9
   I1      88   0  1E-21
   Q1      11  89  13  QX
   Q2      12  80  14  QX
   R2       6   9  100.0E3
   RCM     84  81  1K
   REE     10  99   8.316E6
   RN1     87   0   2.55E8
   RN2     87  88  11.67E3
   RO1      8   5  63
   RO2      7  99  62
   VCM+    82  99  1.0
   VCM-    83  99  -2.3
   VB       9   0  DC  0
   VC       3  53  DC  1.400
   VE      54   4  DC  1.400
   VLIM     7   8  DC  0
   VLP     91   0  DC  30
   VLN      0  92  DC  30
   VPSR     0  86  DC  0
   RFB      5   2  1K
   RIN1     3   1  220K
   RIN2     1   4  220K
.MODEL DX  D(IS=800.OE-18)
.MODEL QX  PNP(IS=800.OE-18 BF=480)
.ENDS
```

TAPE AND REEL INFORMATION

REEL DIMENSIONS

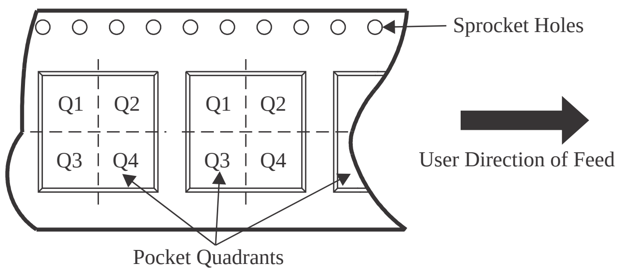


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

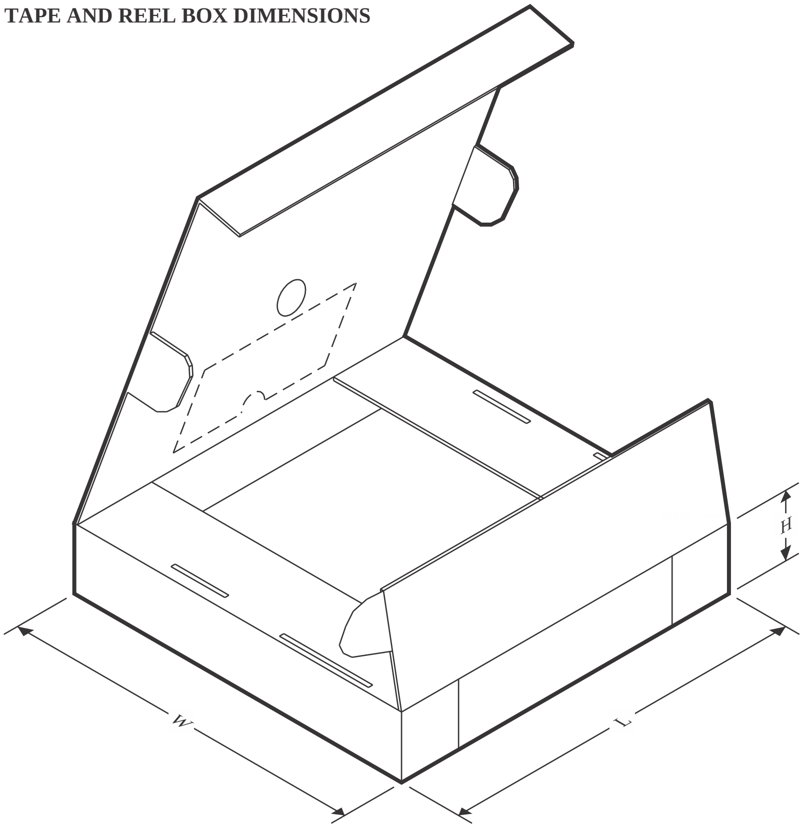
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

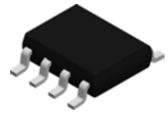
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLE2426MDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

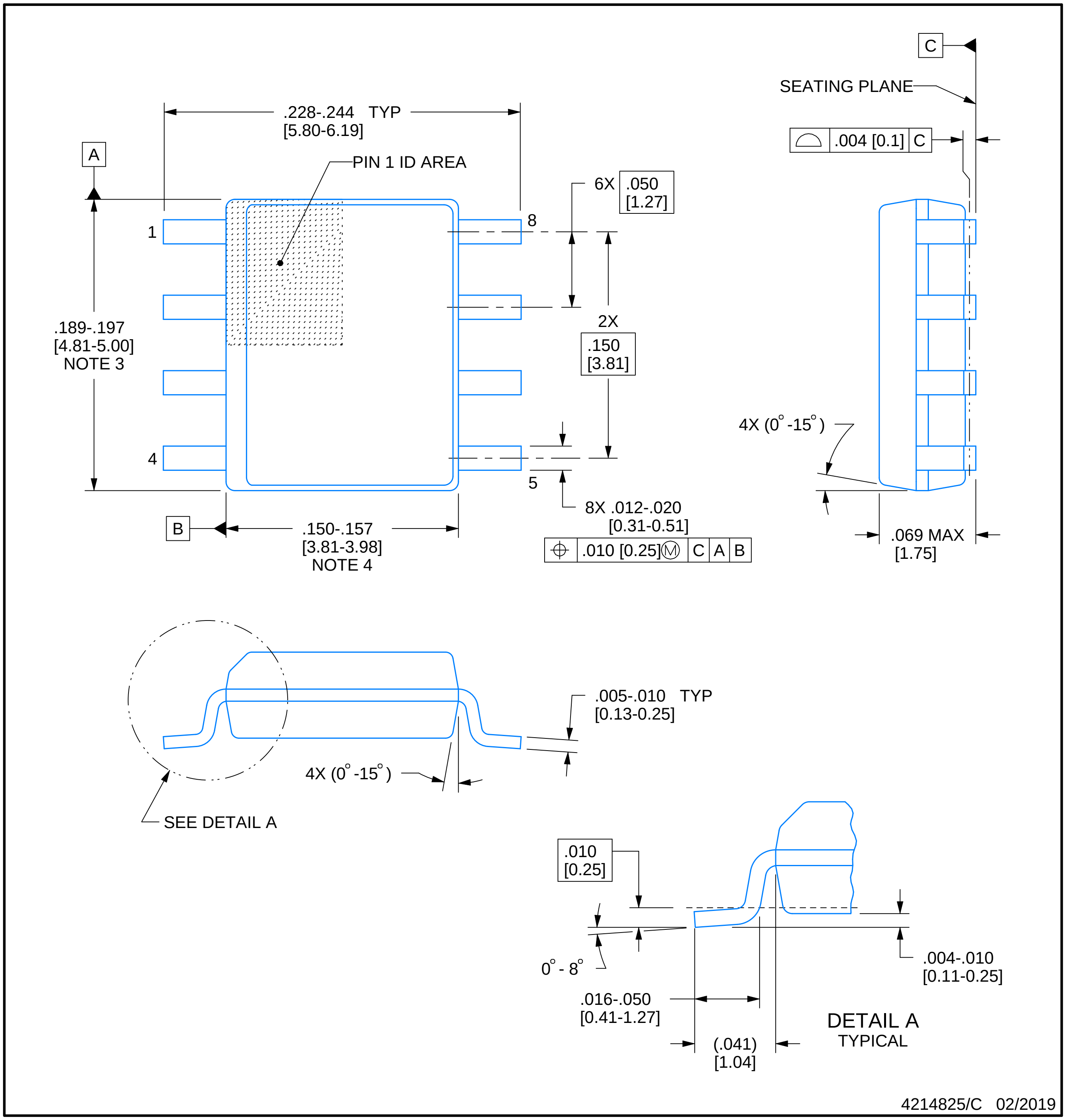
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLE2426MDREP	SOIC	D	8	2500	350.0	350.0	43.0



PACKAGE OUTLINE

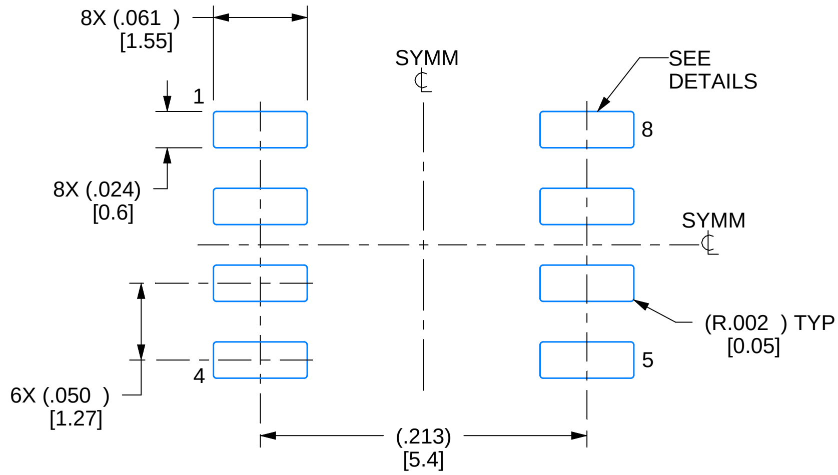
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

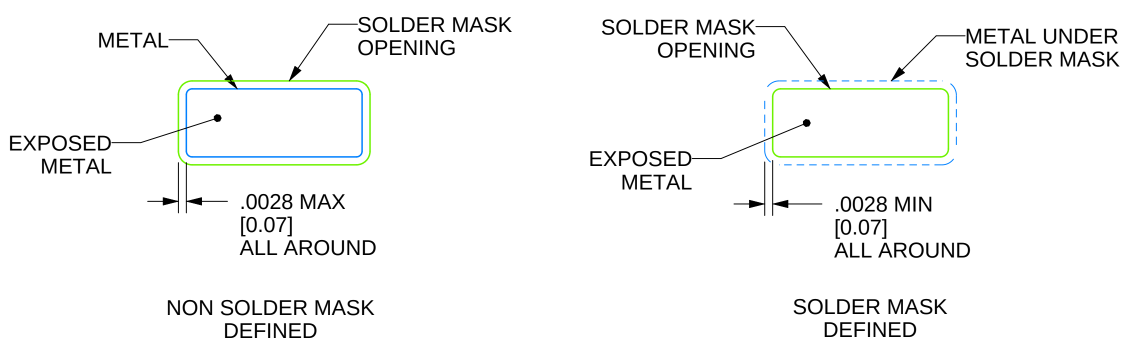


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

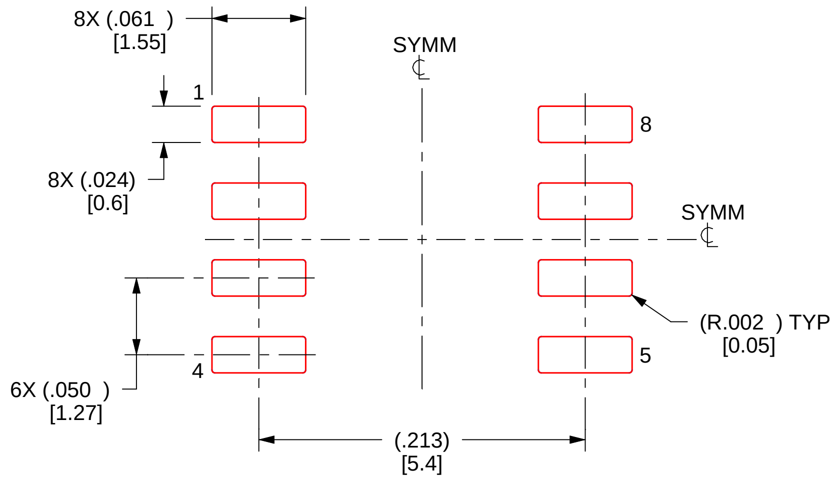


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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