TLV1704-SEP 2.2-V to 36-V, Radiation Hardened microPower Quad Comparator in Space Enhanced Plastic

1 Features

- VID V62/18613
- Radiation Hardened
  - Single Event Latch-up (SEL) Immune to 43 MeV-cm^2/mg at 125°C
  - ELDRS Free to 30 krad(Si)
  - Total Ionizing Dose (TID) RLAT for Every Wafer Lot up to 20 krad(Si)
- Space Enhanced Plastic
  - Controlled Baseline
  - Gold Wire
  - NiPdAu Lead Finish
  - One Assembly and Test Site
  - One Fabrication Site
  - Available in Military (–55°C to 125°C) Temperature Range
  - Extended Product Life Cycle
  - Extended Product-Change Notification
  - Product Traceability
  - Enhanced Mold Compound for Low Outgassing
- Supply Range: 2.2 V to 36 V or ±1.1 V to ±18 V
- Low Quiescent Current: 55 µA per Comparator
- Input Common-Mode Range Includes Both Rails
- Low Propagation Delay: 560 ns
- Low Input Offset Voltage: 300 µV
- Open Collector Outputs:
  - Up to 36 V Above Negative Supply Regardless of Supply Voltage
- Small Packages:
  - Quad: TSSOP-14

2 Applications

- Support Low Earth Orbit Space Applications
- Overvoltage and Undervoltage Detectors
- Satellite Telemetry and Telecommand for On-board Data Handling
- Window Comparators
- Overcurrent Detectors
- Zero-Crossing Detectors
- System Monitoring for Space

3 Description

The TLV1704-SEP (Quad) device offers a wide supply range, rail-to-rail inputs, low quiescent current, and low propagation delay. All these features come in industry-standard, extremely-small packages, making these devices the best general-purpose comparators available.

The open collector output offers the advantage of allowing the output to be pulled to any voltage rail up to 36 V above the negative power supply, regardless of the TLV1704-SEP supply voltage.

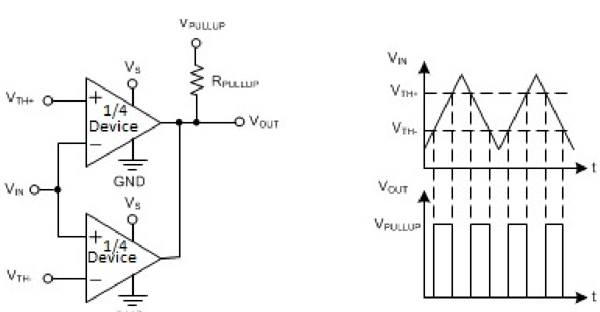
The device is a microPower comparator. Low input offset voltage, low input bias currents, low supply current, and open-collector configuration make the TLV1704-SEP device flexible enough to handle almost any application, from simple voltage detection to driving a single relay.

Device Information(1)

PART NUMBER	GRADE	PACKAGE
TLV1704AMPWTPSEP	20 krad(Si) RLAT	TSSOP (14)
TLV1704AMPWPSEP		

(1) For all available packages, see the package option addendum at the end of the data sheet.

TLV1704-SEP as a Window Comparator



Stable Propagation Delay vs Temperature

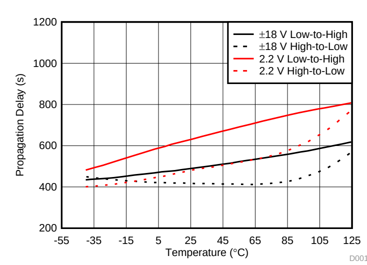


Table of Contents

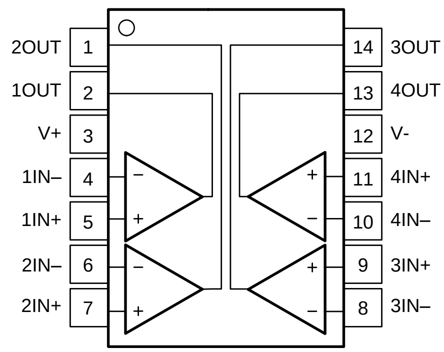
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
November 2018	*	Initial release.

5 Pin Configuration and Functions

TLV1704-SEP PW Package
14-Pin TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
IN+	—	I	Noninverting input.
1IN+	5	I	Noninverting input, channel 1.
2IN+	7	I	Noninverting input, channel 2.
3IN+	9	I	Noninverting input, channel 3.
4IN+	11	I	Noninverting input, channel 4.
IN–	—	I	Inverting input.
1IN–	4	I	Inverting input, channel 1.
2IN–	6	I	Inverting input, channel 2.
3IN–	8	I	Inverting input, channel 3.
4IN–	10	I	Inverting input, channel 4.
OUT	—	O	Output.
1OUT	2	O	Output, channel 1.
2OUT	1	O	Output, channel 2.
3OUT	14	O	Output, channel 3.
4OUT	13	O	Output, channel 4.
V+	3	—	Positive (highest) power supply.
V–	12	—	Negative (lowest) power supply.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Supply voltage			40 (±20)	V
Signal input pins	Voltage[2]	(V_S–) – 0.5	(V_S+) + 0.5	V
	Current[2]		±10	mA
Output short-circuit[3]		Continuous		mA
Operating Junction temperature, T_J		–55	125	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(3) Short-circuit to ground; one comparator per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1]	±1000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage V_S = (V_S+) – (V_S–)	2.2 (±1.1)		36 (±18)	V
Specified temperature	–55		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		TLV1704-SEP PW (TSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	128.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	69.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	69.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at T_A = –55°C to 125°C, V_S = 2.2 V to 36 V, C_L = 15 pF, R_{PULLUP} = 5.1 kΩ, V_{CM} = V_S / 2, and V_S = V_{PULLUP} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	T_A = 25°C, V_S = 2.2 V		±0.5	±3.5	mV
		T_A = 25°C, V_S = 36 V		±0.3	±2.5	mV
		T_A = –55°C to 125°C			±5.5	mV
dV_{OS}/dT	Input offset voltage drift	T_A = –55°C to 125°C		±4	±20	µV/°C
PSRR	Power-supply rejection ratio	T_A = 25°C		15	100	µV/V
		T_A = –55°C to 125°C		20		µV/V
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	T_A = –55°C to 125°C	(V–)		(V+)	V
INPUT BIAS CURRENT						
I_B	Input bias current	T_A = 25°C		5	15	nA
		T_A = –55°C to 125°C			20	nA
I_{OS}	Input offset current	T_A = 25°C		0.5		nA
C_{LOAD}	Capacitive load drive		See *Typical Characteristics*			
OUTPUT						
V_O	Voltage output swing from rail	I_O ≤ 4 mA, input overdrive = 100 mV, V_S = 36 V			1100	mV
		I_O = 0 mA, input overdrive = 100 mV, V_S = 36 V			700	mV
I_{SC}	Short circuit sink current	T_A = 25°C		20		mA
	Output leakage current	V_{IN+} > $V_{IN–}$, T_J = 25°C		70		nA
POWER SUPPLY						
V_S	Specified voltage range		2.2		36	V
I_Q	Quiescent current (per channel)	I_O = 0 A , T_A = 25°C		55	75	µA
		I_O = 0 A, T_A = –55°C to 125°C			100	µA

6.6 Switching Characteristics

at T_A = –55°C to 125°C, V_S = 2.2 V to 36 V, C_L = 15 pF, R_{PULLUP} = 5.1 kΩ, V_{CM} = V_S / 2, and V_S = V_{PULLUP} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pHL}	Propagation delay time, high-to-low	Input overdrive = 100 mV, T_A = 25°C		460		ns
t_{pLH}	Propagation delay time, low-to-high	Input overdrive = 100 mV, T_A = 25°C		560		ns
t_R	Rise time	Input overdrive = 100 mV, T_A = 25°C		365		ns
t_F	Fall time	Input overdrive = 100 mV, T_A = 25°C		240		ns

6.7 Typical Characteristics

at T_A = 25°C, V_S = 5 V, R_{PULLUP} = 5.1 kΩ, and input overdrive = 100 mV (unless otherwise noted)

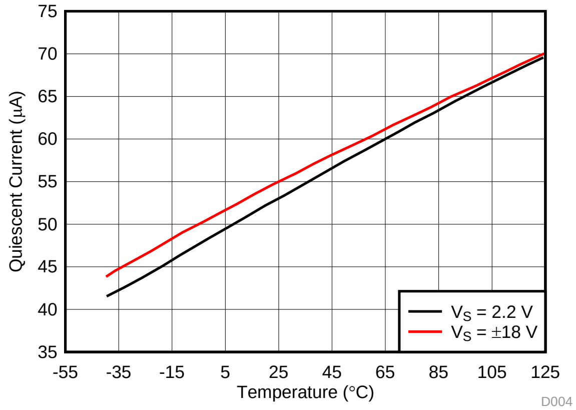


Figure 1. Quiescent Current vs Temperature

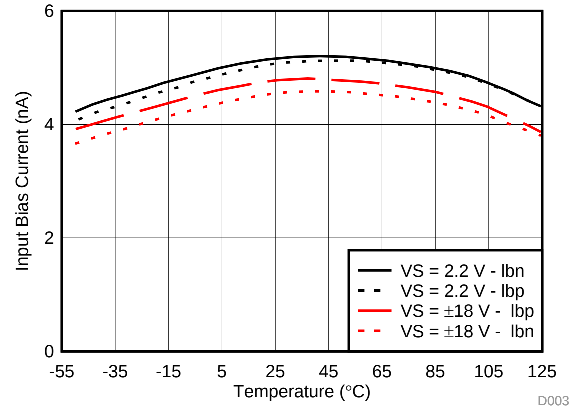


Figure 2. Input Bias Current vs Temperature

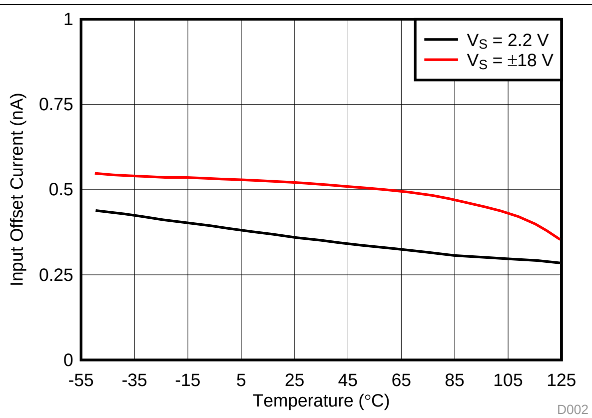


Figure 3. Input Offset Current vs Temperature

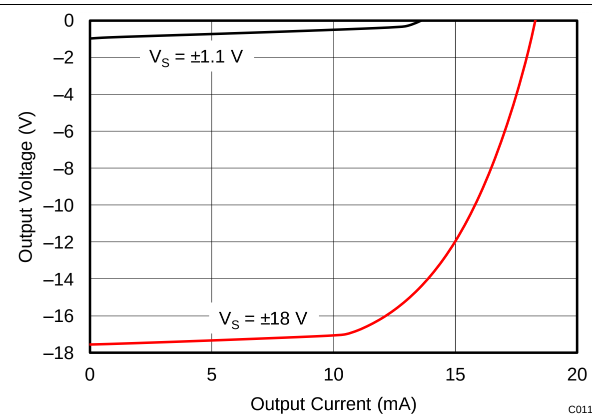


Figure 4. Output Voltage vs Output Current

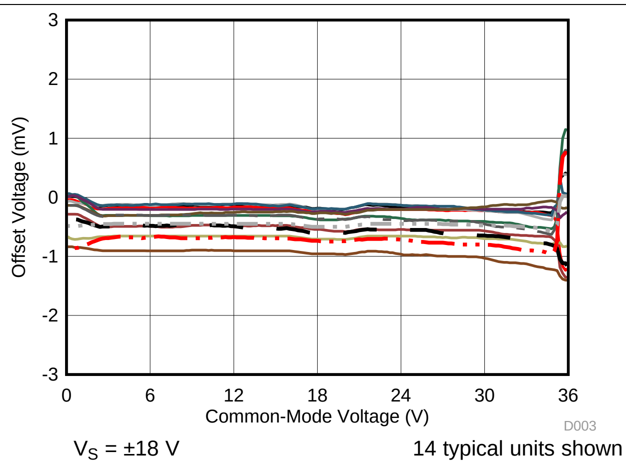


Figure 5. Offset Voltage vs Common-Mode Voltage

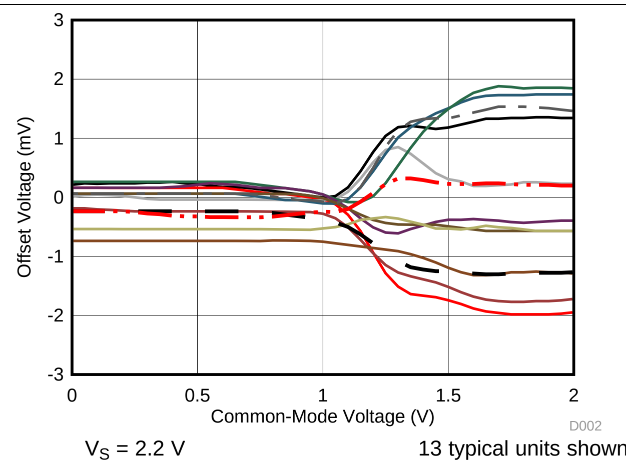
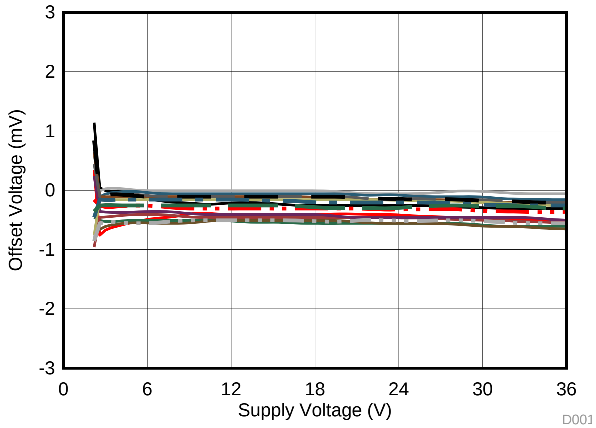


Figure 6. Offset Voltage vs Common-Mode Voltage

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, R_{PULLUP} = 5.1 kΩ, and input overdrive = 100 mV (unless otherwise noted)



16 typical units shown

Figure 7. Offset Voltage vs Supply Voltage

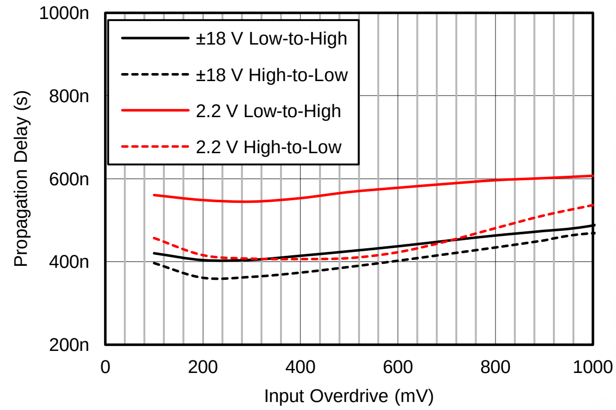


Figure 8. Propagation Delay vs Input Overdrive

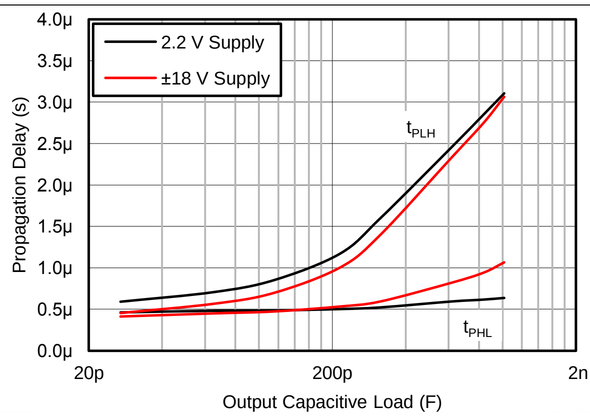
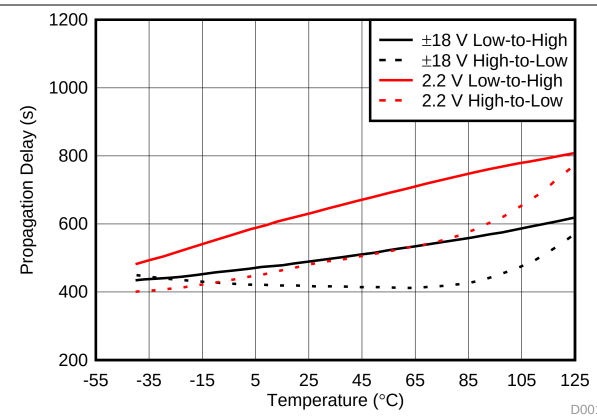
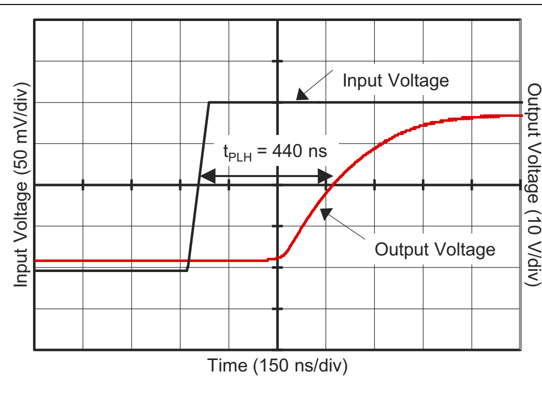


Figure 9. Propagation Delay vs Capacitive Load



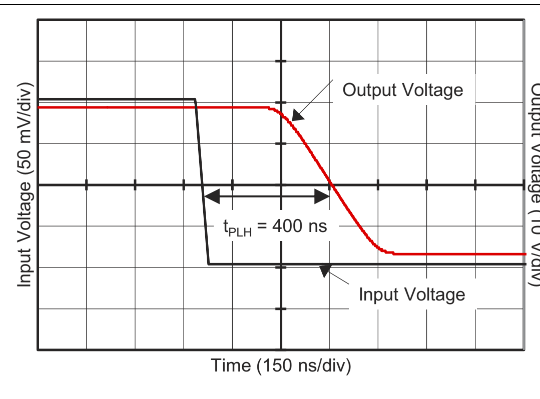
V_{OD} = 100 mV

Figure 10. Propagation Delay vs Temperature



V_S = 36 V Overdrive = 100 mV

Figure 11. Propagation Delay (T_{pLH})

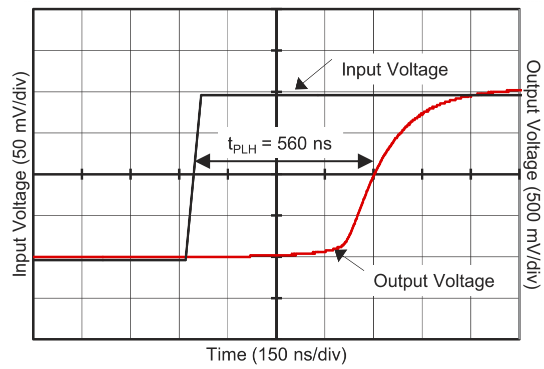


V_S = 36 V Overdrive = 100 mV

Figure 12. Propagation Delay (T_{pHL})

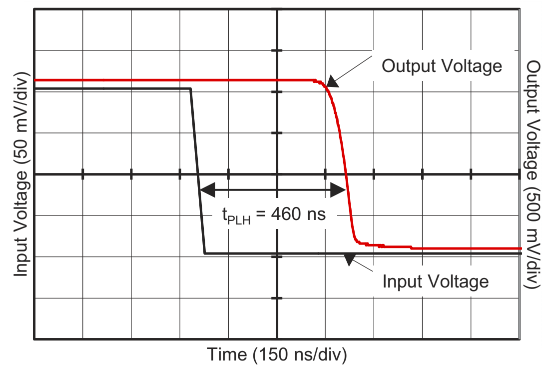
Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, R_{PULLUP} = 5.1 kΩ, and input overdrive = 100 mV (unless otherwise noted)



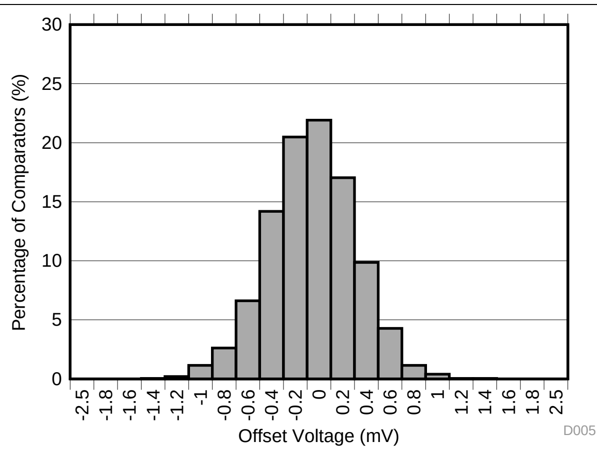
V_S = 2.2 V Overdrive = 100 mV

Figure 13. Propagation Delay (T_{pLH})



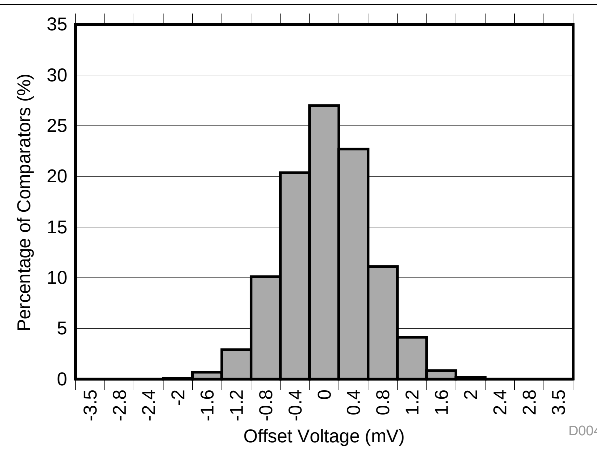
V_S = 2.2 V Overdrive = 100 mV

Figure 14. Propagation Delay (T_{pHL})



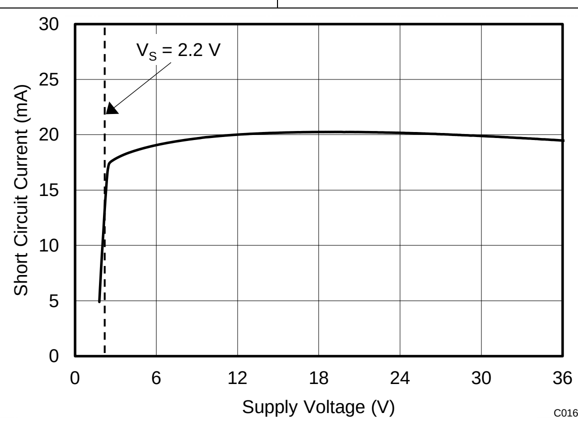
V_S = ±18 V Distribution taken from 2524 comparators

Figure 15. Offset Voltage Production Distribution



V_S = 2.2 V Distribution taken from 2524 comparators

Figure 16. Offset Voltage Production Distribution



Sink current

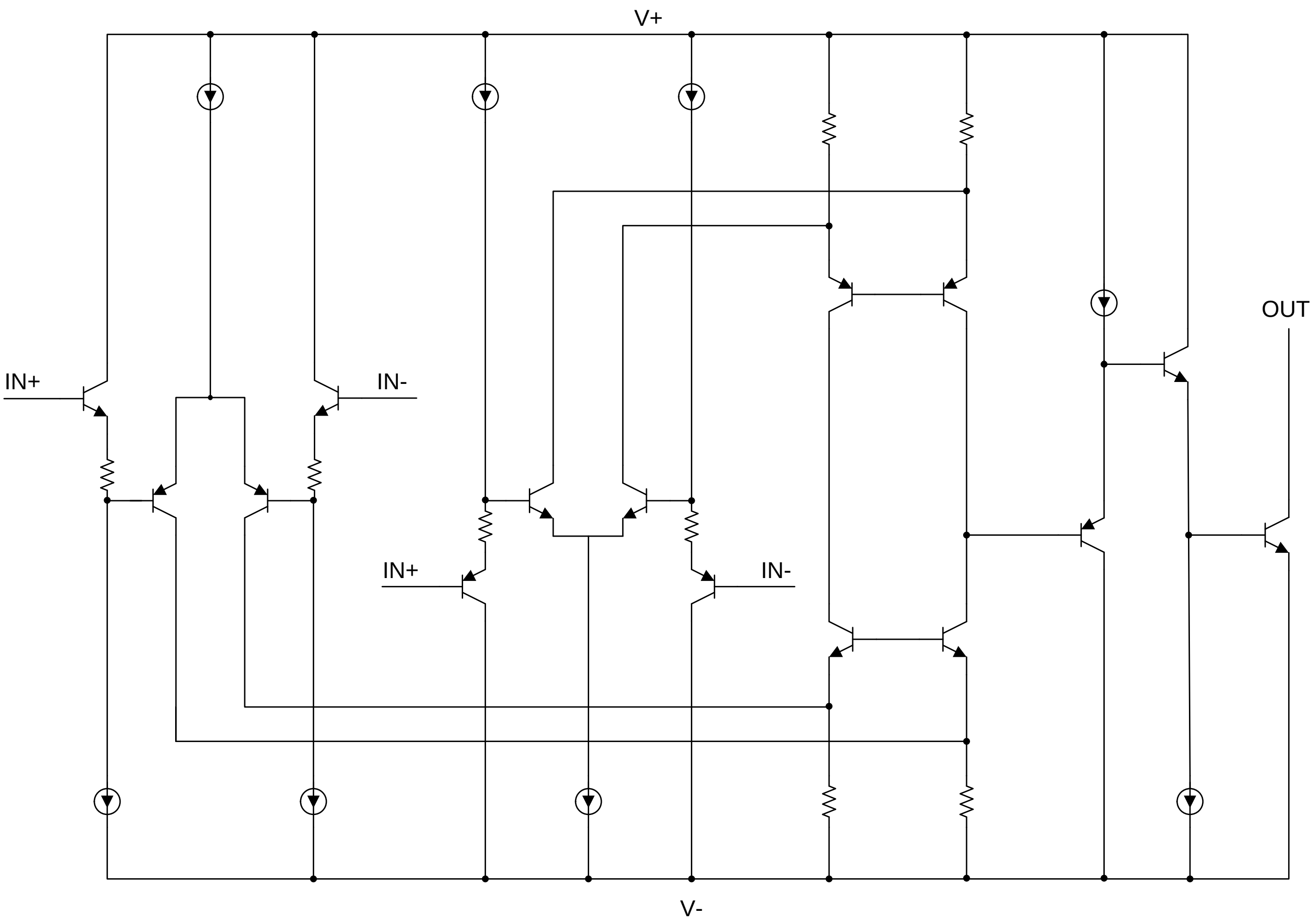
Figure 17. Short-Circuit Current vs Supply Voltage

7 Detailed Description

7.1 Overview

The TLV1704-SEP comparator features rail-to-rail input and output on supply voltages as high as 36 V. The rail-to-rail input stage enables detection of signals close to the supply and ground. The open-collector configuration allows the device to be used in wired-OR configurations, such as a window comparator. A low supply current of 55 µA per channel with small, space-saving packages, makes these comparators versatile for use in a wide range of applications, from portable to industrial.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Comparator Inputs

The TLV1704-SEP device is a rail-to-rail input comparator, with an input common-mode range that includes the supply rails. The TLV1704-SEP device is designed to prevent phase inversion when the input pins exceed the supply voltage. Figure 18 shows the TLV1704-SEP device response when input voltages exceed the supply, resulting in no phase inversion.

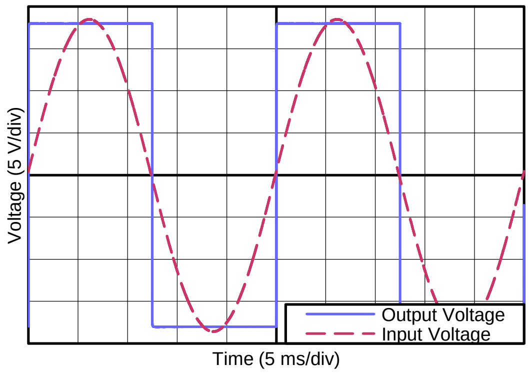


Figure 18. No Phase Inversion: Comparator Response to Input Voltage (Propagation Delay Included)

7.4 Device Functional Modes

7.4.1 Setting Reference Voltage

Using a stable reference is important when setting the transition point for the TLV1704-SEP device. The REF3333, as shown in Figure 19, provides a 3.3-V reference voltage with low drift and only 3.9 μA of quiescent current.

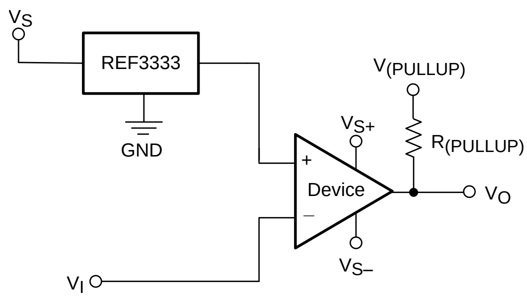


Figure 19. Reference Voltage for the TLV1704-SEP

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV1704-SEP device can be used in a wide variety of applications, such as zero crossing detectors, window comparators, over and undervoltage detectors, and high-side voltage sense circuits.

8.2 Typical Application

Comparators are used to differentiate between two different signal levels. For example, a comparator differentiates between an overtemperature and normal-temperature condition. However, noise or signal variation at the comparison threshold causes multiple transitions. This application example sets upper and lower hysteresis thresholds to eliminate the multiple transitions caused by noise.

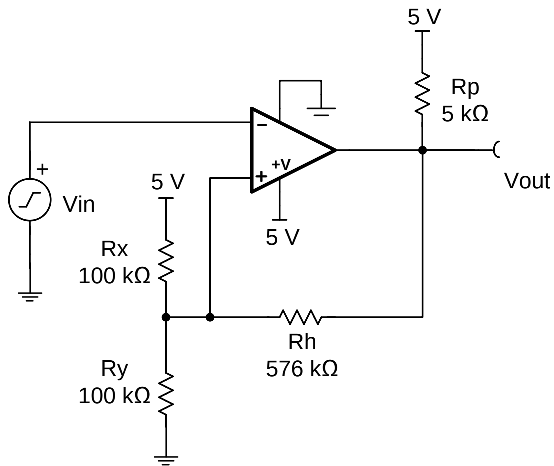


Figure 20. Comparator Schematic With Hysteresis

8.2.1 Design Requirements

The design requirements are as follows:

- Supply voltage: 5 V
- Input: 0 V to 5 V
- Lower threshold (VL) = 2.3 V ±0.1 V
- Upper threshold (VH) = 2.7 V ±0.1 V
- VH – VL = 2.4 V ±0.1 V
- Low-power consumption

Typical Application (continued)

8.2.2 Detailed Design Procedure

Make a small change to the comparator circuit to add hysteresis. Hysteresis uses two different threshold voltages to avoid the multiple transitions introduced in the previous circuit. The input signal must exceed the upper threshold (VH) to transition low, or below the lower threshold (VL) to transition high.

Figure 20 illustrates hysteresis on a comparator. Resistor Rh sets the hysteresis level. An open-collector output stage requires a pullup resistor (Rp). The pullup resistor creates a voltage divider at the comparator output that introduces an error when the output is at logic high. This error can be minimized if Rh > 100 Rp.

When the output is at a logic high (5 V), Rh is in parallel with Rx (ignoring Rp). This configuration drives more current into Ry, and raises the threshold voltage (VH) to 2.7 V. The input signal must drive above VH = 2.7 V to cause the output to transition to logic low (0 V).

When the output is at logic low (0 V), Rh is in parallel with Ry. This configuration reduces the current into Ry, and reduces the threshold voltage to 2.3 V. The input signal must drive below VL = 2.3 V to cause the output to transition to logic high (5 V).

For more details on this design and other alternative devices that can be used in place of the TLV1702, refer to Precision Design TIPD144, *Comparator with Hysteresis Reference Design*.

8.2.3 Application Curve

Figure 21 shows the upper and lower thresholds for hysteresis. The upper threshold is 2.76 V and the lower threshold is 2.34 V, both of which are close to the design target.

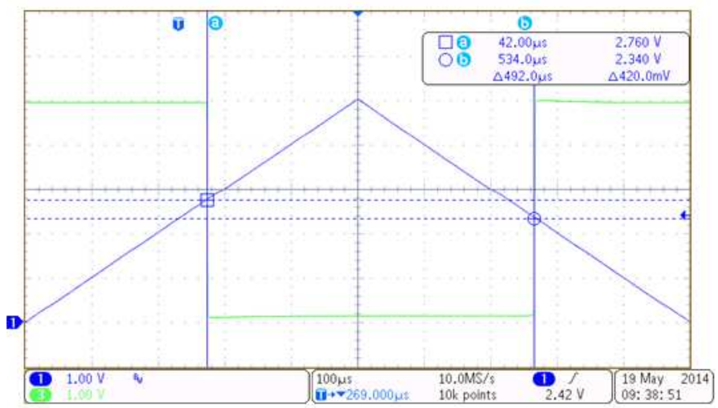


Figure 21. TLV1701 Upper and Lower Threshold With Hysteresis

9 Power Supply Recommendations

The TLV1704-SEP device is specified for operation from 2.2 V to 36 V (±1.1 to ±18 V); many specifications apply from –55°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section.

CAUTION

Supply voltages larger than 40 V can permanently damage the device; see the *Absolute Maximum Ratings*.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement; see the *Layout Guidelines* section.

10 Layout

10.1 Layout Guidelines

Comparators are very sensitive to input noise. For best results, maintain the following layout guidelines:

- Use a printed-circuit board (PCB) with a good, unbroken low-inductance ground plane. Proper grounding (use of ground plane) helps maintain specified performance of the TLV1704-SEP device.
- To minimize supply noise, place a decoupling capacitor (0.1-µF ceramic, surface-mount capacitor) as close as possible to V_S as shown in Figure 22.
- On the inputs and the output, keep lead lengths as short as possible to avoid unwanted parasitic feedback around the comparator. Keep inputs away from the output.
- Solder the device directly to the PCB rather than using a socket.
- For slow-moving input signals, take care to prevent parasitic feedback. A small capacitor (1000 pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes some degradation to propagation delay when the impedance is low. Run the topside ground plane between the output and inputs.
- Run the ground pin ground trace under the device up to the bypass capacitor, shielding the inputs from the outputs.

10.2 Layout Example

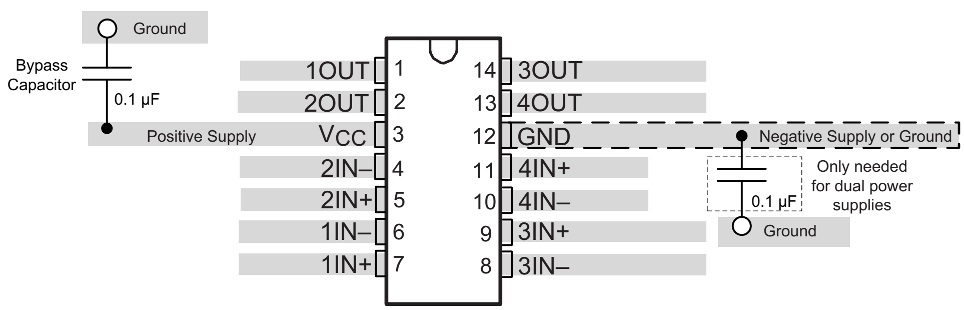


Figure 22. Comparator Board Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- *Precision Design, Comparator with Hysteresis Reference Design*, TIDU020
- *REF33xx 3.9-μA, SC70-3, SOT-23-3, and UQFN-8, 30-ppm/°C Drift Voltage Reference*, SBOS392

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV1704AMPWPSEP	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1704SEP	Samples
TLV1704AMPWTPSEP	ACTIVE	TSSOP	PW	14	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1704SEP	Samples
V62/18613-01XE	ACTIVE	TSSOP	PW	14	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1704SEP	Samples
V62/18613-01XE-T	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1704SEP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

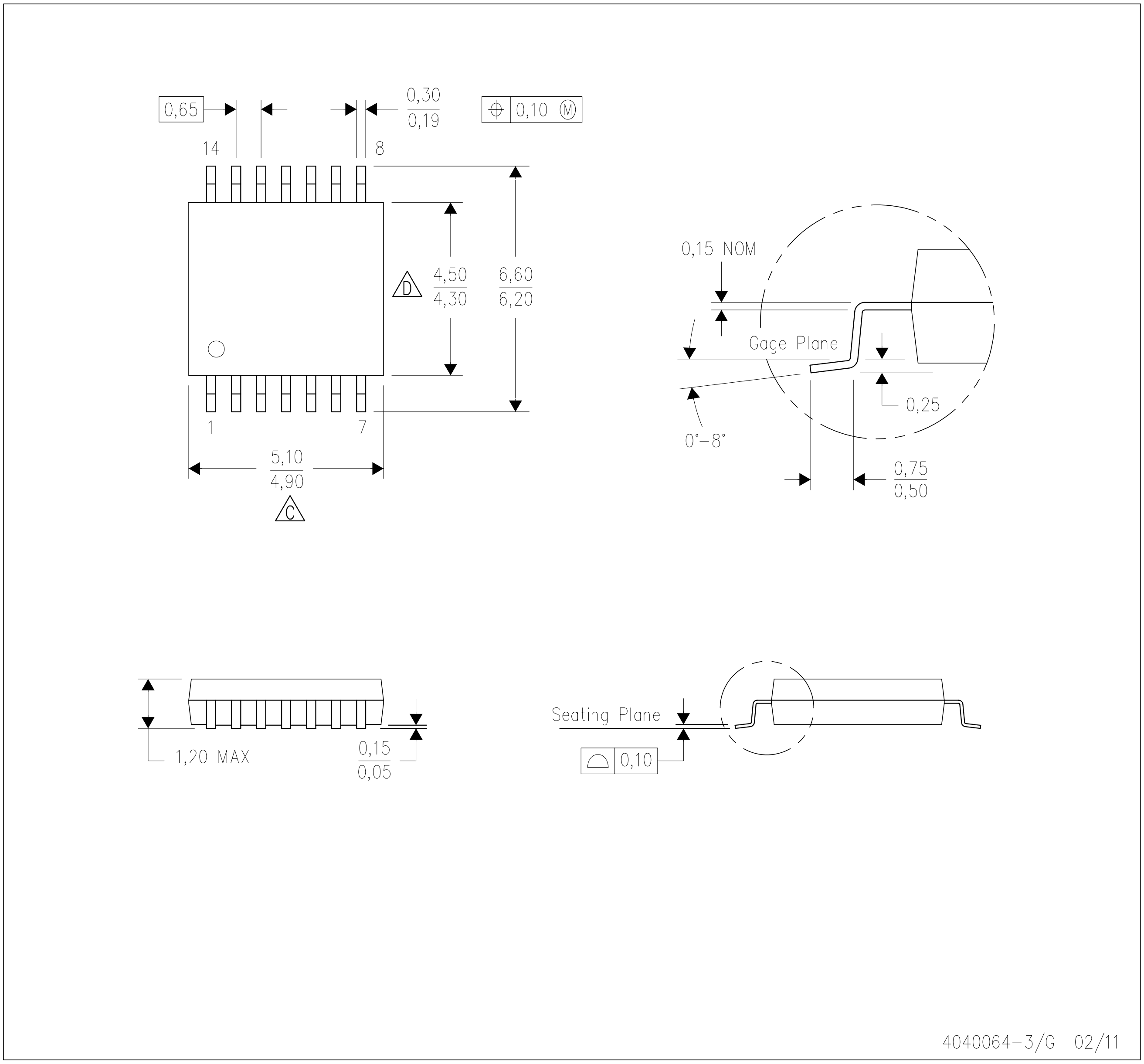
OTHER QUALIFIED VERSIONS OF TLV1704-SEP :

- Automotive: TLV1704-Q1

NOTE: Qualified Version Definitions:

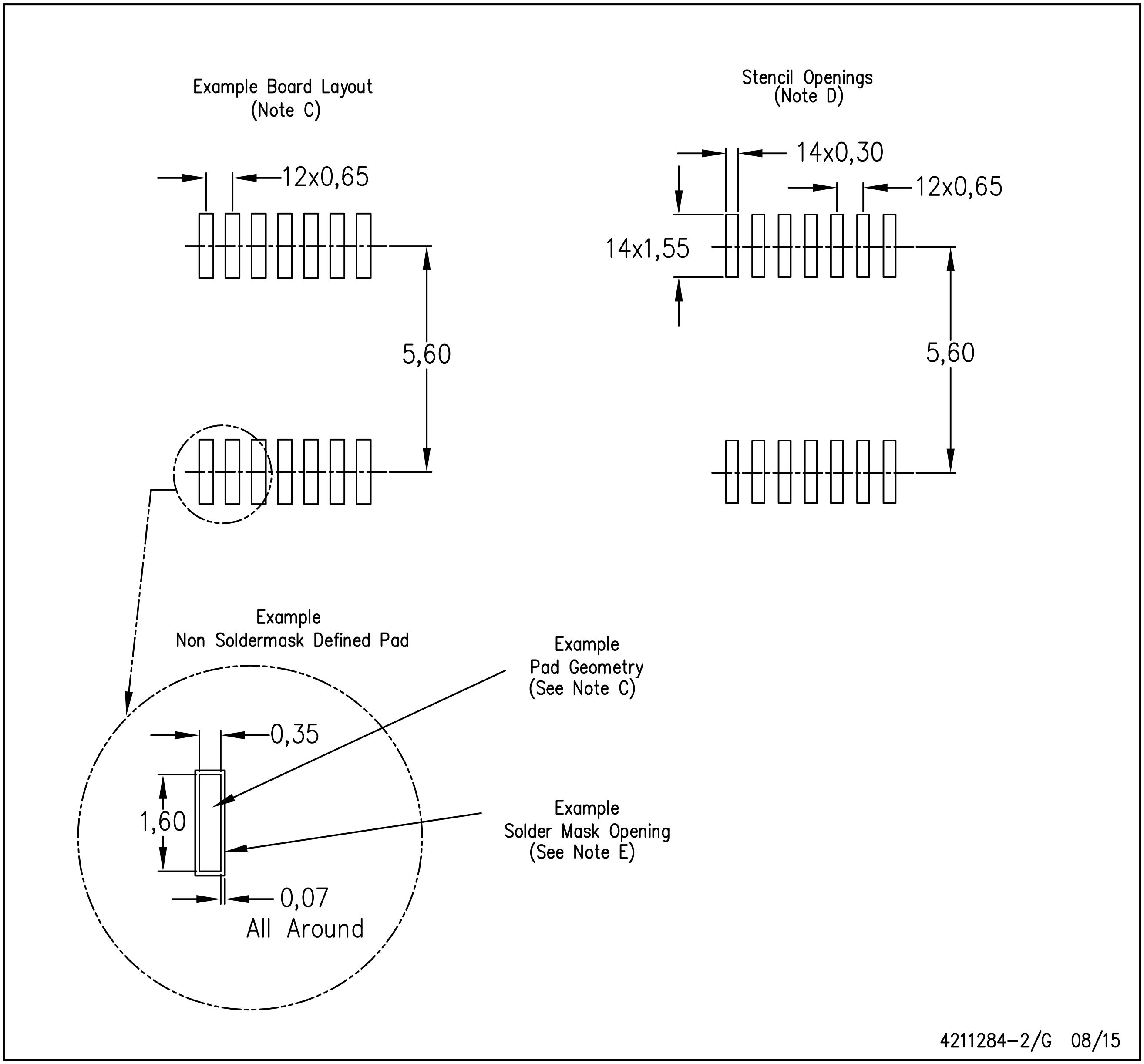
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.