

# TLV2172-Q1 36-V, Single-Supply, Low-Power Operational Amplifier for Cost-Sensitive Systems

## 1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 3A
  - Device CDM ESD Classification Level C6
- Supply Range: 4.5 V to 36 V,  $\pm 2.25$  V to  $\pm 18$  V
- Low Noise:  $9\text{ nV}/\sqrt{\text{Hz}}$
- Low Offset Drift:  $\pm 1\text{ }\mu\text{V}/^{\circ}\text{C}$  (Typical)
- EMI-Hardened
- Input Range Includes Negative Supply
- Rail-to-Rail Output
- Gain Bandwidth: 10 MHz
- Slew Rate:  $10\text{ V}/\mu\text{s}$
- Low Quiescent Current: 1.6 mA per Amplifier
- High Common-Mode Rejection: 116 dB (Typical)
- Low Input Bias Current: 10 pA

## 2 Applications

- Automotive
- HEV and EV Power Trains
- Advanced Driver Assist (ADAS)
- Automotive Climate Controls
- Avionics and Landing Gear
- Medical Instrumentation
- Current Sensing

## 3 Description

The TLV2172-Q1 operational amplifier features a THD+N of 0.0002% at 1 kHz with the ability to operate on supplies ranging from 4.5 V ( $\pm 2.25$  V) to 36 V ( $\pm 18$  V). These features, along with low noise and very high PSRR, enable the TLV2172-Q1 to amplify microvolt-level signals in applications such as HEV and EV automobiles and power trains, medical instrumentation, and more. The TLV2172-Q1 device offers good offset and drift, a high bandwidth of 10 MHz, and a slew rate of  $10\text{ V}/\mu\text{s}$  with only 2.3 mA of quiescent current over temperature (maximum.)

Unlike most op amps that are specified at only one supply voltage, the TLV2172-Q1 device is specified from 4.5 V to 36 V. Input signals beyond the supply rails do not cause phase reversal. The TLV2172-Q1 device is stable with capacitive loads up to 300 pF. The input can operate 100 mV below the negative rail and within 2 V of the positive rail for normal operation. Note that the device can operate with a full rail-to-rail input 100 mV beyond the positive rail, but with reduced performance within 2 V of the positive rail.

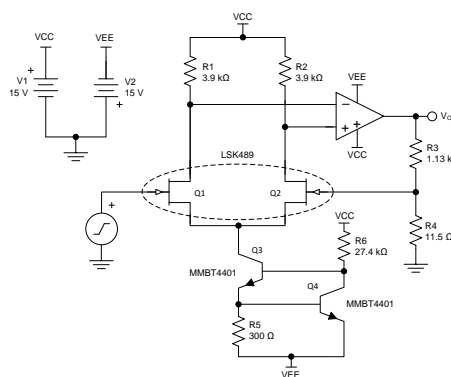
The TLV2172-Q1 op amp is specified from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV2172-Q1	VSSOP (8)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Simplified Schematic



Copyright © 2017, Texas Instruments Incorporated



## Table of Contents

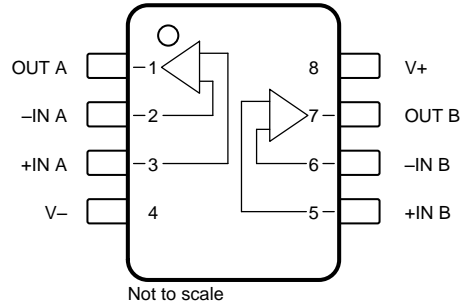
<b>1 Features</b> .....	<b>1</b>	<b>8 Application and Implementation</b> .....	<b>16</b>
<b>2 Applications</b> .....	<b>1</b>	8.1 Application Information.....	16
<b>3 Description</b> .....	<b>1</b>	8.2 Typical Application .....	16
<b>4 Revision History</b> .....	<b>2</b>	<b>9 Power Supply Recommendations</b> .....	<b>18</b>
<b>5 Pin Configuration and Functions</b> .....	<b>3</b>	<b>10 Layout</b> .....	<b>18</b>
<b>6 Specifications</b> .....	<b>4</b>	10.1 Layout Guidelines .....	18
6.1 Absolute Maximum Ratings .....	4	10.2 Layout Example .....	19
6.2 ESD Ratings .....	4	<b>11 Device and Documentation Support</b> .....	<b>20</b>
6.3 Recommended Operating Conditions.....	4	11.1 Device Support.....	20
6.4 Thermal Information: TLV2172-Q1 .....	4	11.2 Documentation Support .....	21
6.5 Electrical Characteristics.....	5	11.3 Related Links .....	21
6.6 Typical Characteristics.....	6	11.4 Receiving Notification of Documentation Updates	21
<b>7 Detailed Description</b> .....	<b>11</b>	11.5 Community Resources.....	21
7.1 Overview .....	11	11.6 Trademarks .....	21
7.2 Functional Block Diagram .....	11	11.7 Electrostatic Discharge Caution.....	21
7.3 Feature Description.....	12	11.8 Glossary .....	21
7.4 Device Functional Modes.....	15	<b>12 Mechanical, Packaging, and Orderable Information</b> .....	<b>21</b>

## 4 Revision History

DATE	REVISION	NOTES
December 2017	*	Initial release.

## 5 Pin Configuration and Functions

**D and DGK Packages  
8-Pin SOIC and VSSOP  
Top View**



### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
-IN A	2	I	Inverting input, channel A
-IN B	6	I	Inverting input, channel B
+IN A	3	I	Noninverting input, channel A
+IN B	5	I	Noninverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V-	4	—	Negative (lowest) power supply
V+	8	—	Positive (highest) power supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT	
Voltage	Supply voltage, V+ to V-	-20	20	V	
	Single-supply voltage		40		
	Signal input pin <sup>(2)</sup>	Common-mode	(V-) - 0.5		(V+) + 0.5
		Differential <sup>(3)</sup>	-0.5		0.5
Current	Signal input pin	-10	10	mA	
	Output short-circuit <sup>(4)</sup>	Continuous			
Operating, T <sub>A</sub>		-55	150	°C	
Junction, T <sub>J</sub>			150		
Storage, T <sub>stg</sub>		-65	150		

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Transient conditions that exceed these voltage ratings must be current limited to 10 mA or less.
- (3) See the *Electrical Overstress* section for more information.
- (4) Short-circuit to ground, one amplifier per package.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±4000
		Charged-device model (CDM), per AEC Q100-011	±1000

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage, (V+) - (V-)	Single-supply	4.5		36	V
	Dual-supply	±2.25		±18	
Specified temperature		-40		125	°C

### 6.4 Thermal Information: TLV2172-Q1

THERMAL METRIC <sup>(1)</sup>		TLV2172-Q1		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	116.1	158	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	69.8	48.6	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	56.6	78.7	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	22.5	3.9	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	56.1	77.3	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	—	—	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 2.25\text{ V}$  to  $\pm 18\text{ V}$ ,  $V_{CM} = V_{OUT} = V_S / 2$ , and  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFFSET VOLTAGE</b>						
$V_{OS}$	Input offset voltage	$T_A = 25^\circ\text{C}$		0.5	1.7	mV
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			2	
$dV_{OS}/dT$	Input offset voltage drift	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		1		$\mu\text{V}/^\circ\text{C}$
PSRR	Power-supply rejection ratio	$V_S = 4\text{ V}$ to $36\text{ V}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	100	120		dB
	Channel separation, DC			5		$\mu\text{V}/\text{V}$
<b>INPUT BIAS CURRENT</b>						
$I_B$	Input bias current	$T_A = 25^\circ\text{C}$		$\pm 10$		pA
$I_{OS}$	Input offset current	$T_A = 25^\circ\text{C}$		$\pm 2$		pA
<b>NOISE</b>						
	Input voltage noise	$f = 0.1\text{ Hz}$ to $10\text{ Hz}$		2.5		$\mu\text{V}_{PP}$
$e_n$	Input voltage noise density	$f = 100\text{ Hz}$		14		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$		9		$\text{nV}/\sqrt{\text{Hz}}$
$i_n$	Input current noise density	$f = 1\text{ kHz}$		1.6		$\text{fA}/\sqrt{\text{Hz}}$
<b>INPUT VOLTAGE</b>						
$V_{CM}$	Common-mode voltage range <sup>(1)</sup>		$(V_-) - 0.1$		$(V_+) - 2$	V
CMRR	Common-mode rejection ratio	$V_S = \pm 18\text{ V}$ , $(V_-) - 0.1\text{ V} < V_{CM} < (V_+) - 2\text{ V}$ $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	94	116		dB
<b>INPUT IMPEDANCE</b>						
	Differential			$100 \parallel 4$		$\text{M}\Omega \parallel \text{pF}$
	Common-mode			$6 \parallel 4$		$10^{13} \Omega \parallel \text{pF}$
<b>OPEN-LOOP GAIN</b>						
$A_{OL}$	Open-loop voltage gain	$(V_-) + 0.35\text{ V} < V_O < (V_+) - 0.35\text{ V}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	97	115		dB
		$(V_-) + 0.5\text{ V} < V_O < (V_+) - 0.5\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		107		
<b>FREQUENCY RESPONSE</b>						
GBP	Gain bandwidth product			10		MHz
SR	Slew rate	$G = +1$		10		$\text{V}/\mu\text{s}$
$t_s$	Settling time	To 0.1%, $V_S = \pm 18\text{ V}$ , $G = 1$ , 10-V step		2		$\mu\text{s}$
		To 0.01% (12-bit), $V_S = \pm 18\text{ V}$ , $G = +1$ , 10-V step			3.2	
	Overload recovery time	$V_{IN} \times \text{gain} > V_S$		200		ns
THD+N	Total harmonic distortion + noise	$V_S = 36\text{ V}$ , $G = +1$ , $f = 1\text{ kHz}$ , $V_O = 3.5\text{ V}_{RMS}$		0.0002%		
<b>OUTPUT</b>						
$V_O$	Voltage output swing from rail	$V_S = \pm 18\text{ V}$ , $R_L = 10\text{ k}\Omega$	$T_A = 25^\circ\text{C}$	70		mV
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	95		
		$V_S = \pm 18\text{ V}$ , $R_L = 2\text{ k}\Omega$	$T_A = 25^\circ\text{C}$	330	400	
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	470	530	
$I_{SC}$	Short-circuit current			$\pm 75$		mA
$C_{LOAD}$	Capacitive load drive			See <a href="#">Typical Characteristics</a>		pF
$R_O$	Open-loop output resistance	$f = 1\text{ MHz}$ , $I_O = 0\text{ A}$		60		$\Omega$
<b>POWER SUPPLY</b>						
$V_S$	Specified voltage range		4.5		36	V
$I_Q$	Quiescent current per amplifier	$I_O = 0\text{ A}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		1.6	2.3	mA

(1) The input range can be extended beyond  $(V_+) - 2\text{ V}$  up to  $V_+$ . See the [Typical Characteristics](#) and [Application and Implementation](#) sections for additional information.

## 6.6 Typical Characteristics

at  $V_S = \pm 18\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$  (unless otherwise noted)

**Table 1. Characteristic Performance Measurements**

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	<a href="#">Figure 1</a>
Offset Voltage vs Common-Mode Voltage	<a href="#">Figure 2</a>
Offset Voltage vs Common-Mode Voltage (Upper Stage)	<a href="#">Figure 3</a>
Input Bias Current vs Temperature	<a href="#">Figure 4</a>
Output Voltage Swing vs Output Current (Maximum Supply)	<a href="#">Figure 5</a>
CMRR and PSRR vs Frequency (Referred-to-Input)	<a href="#">Figure 6</a>
0.1-Hz to 10-Hz Noise	<a href="#">Figure 7</a>
Input Voltage Noise Spectral Density vs Frequency	<a href="#">Figure 8</a>
Quiescent Current vs Supply Voltage	<a href="#">Figure 9</a>
Open-Loop Gain and Phase vs Frequency	<a href="#">Figure 10</a>
Closed-Loop Gain vs Frequency	<a href="#">Figure 11</a>
Open-Loop Output Impedance vs Frequency	<a href="#">Figure 12</a>
Small-Signal Overshoot vs Capacitive Load	<a href="#">Figure 13</a> , <a href="#">Figure 14</a>
No Phase Reversal	<a href="#">Figure 15</a>
Small-Signal Step Response (10 mV)	<a href="#">Figure 16</a> , <a href="#">Figure 17</a>
Large-Signal Step Response	<a href="#">Figure 18</a> , <a href="#">Figure 19</a>
Large-Signal Settling Time	<a href="#">Figure 20</a> , <a href="#">Figure 21</a>
Short-Circuit Current vs Temperature	<a href="#">Figure 22</a>
Maximum Output Voltage vs Frequency	<a href="#">Figure 23</a>
EMIRR IN+ vs Frequency	<a href="#">Figure 24</a>

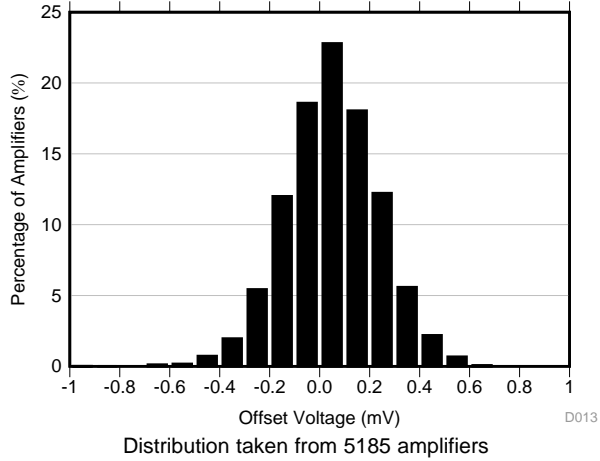


Figure 1. Offset Voltage Production Distribution Histogram

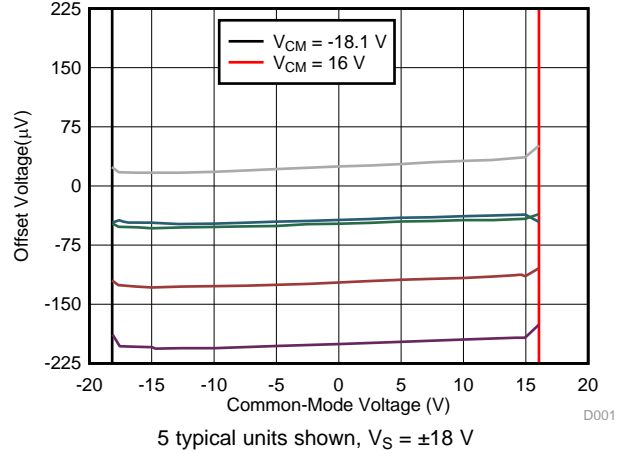


Figure 2. Offset Voltage vs Common-Mode Voltage

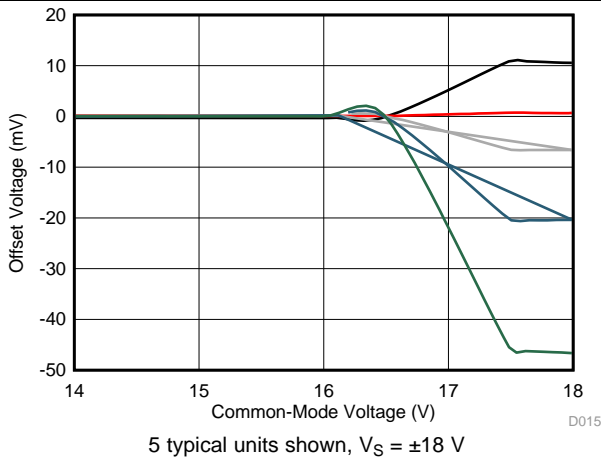


Figure 3. Offset Voltage vs Common-Mode Voltage (Upper Stage)

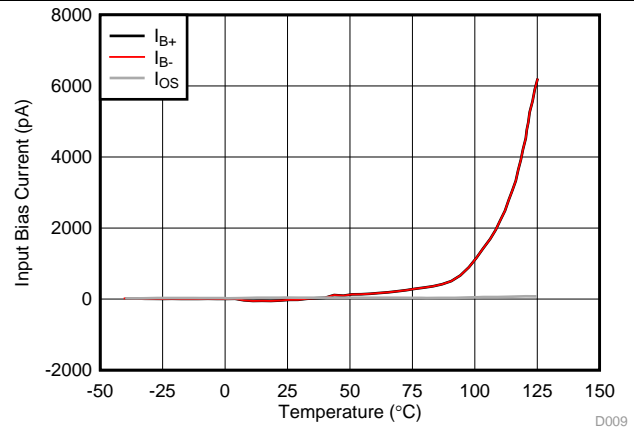


Figure 4. Input Bias Current vs Temperature

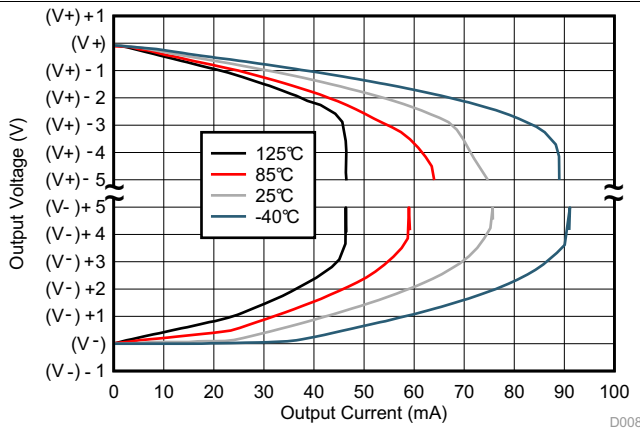


Figure 5. Output Voltage Swing vs Output Current (Maximum Supply)

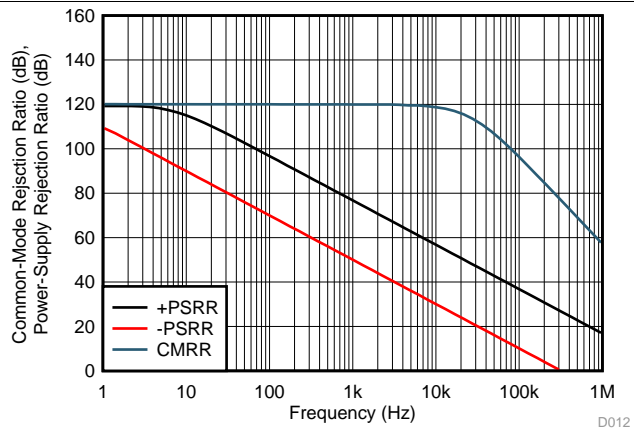


Figure 6. CMRR and PSRR vs Frequency (Referred-to-Input)

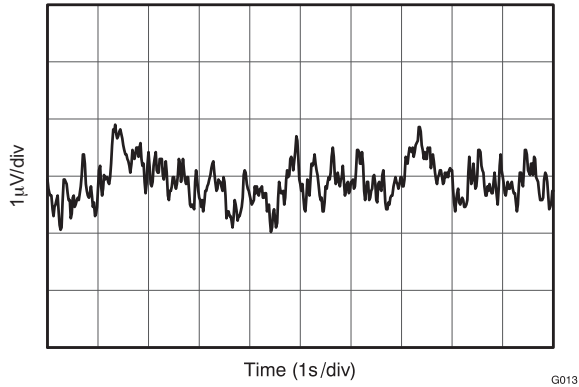


Figure 7. 0.1-Hz to 10-Hz Noise

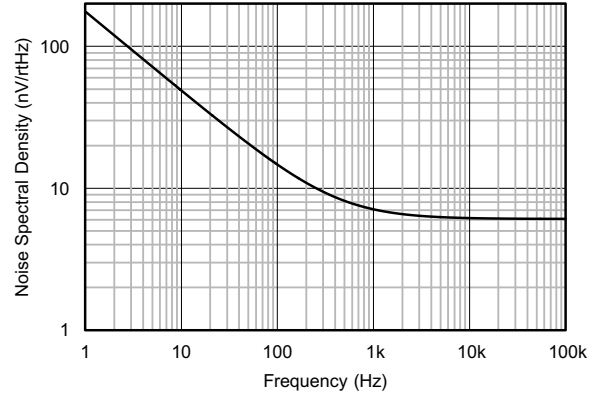


Figure 8. Input Voltage Noise Spectral Density vs Frequency

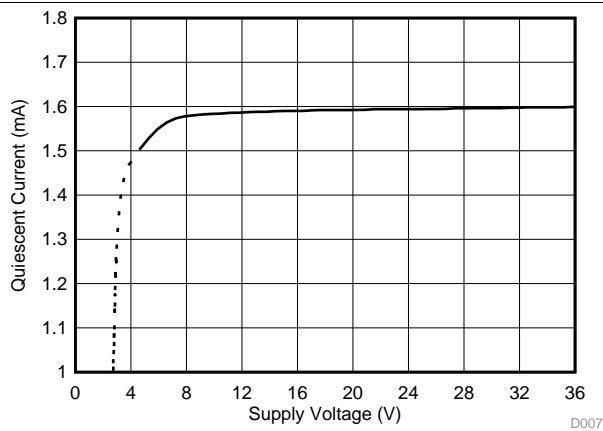


Figure 9. Quiescent Current vs Supply Voltage

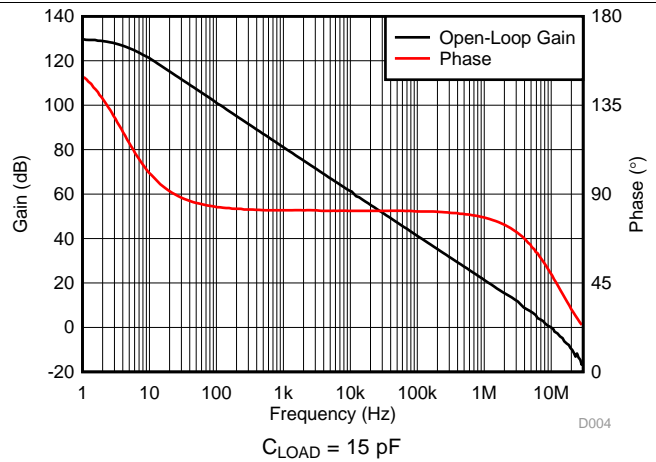


Figure 10. Open-Loop Gain and Phase vs Frequency

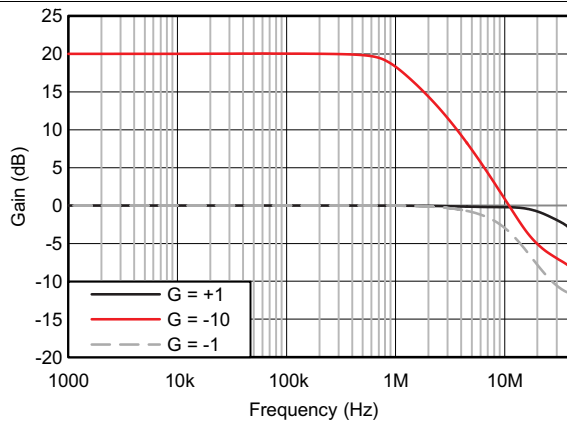


Figure 11. Closed-Loop Gain vs Frequency

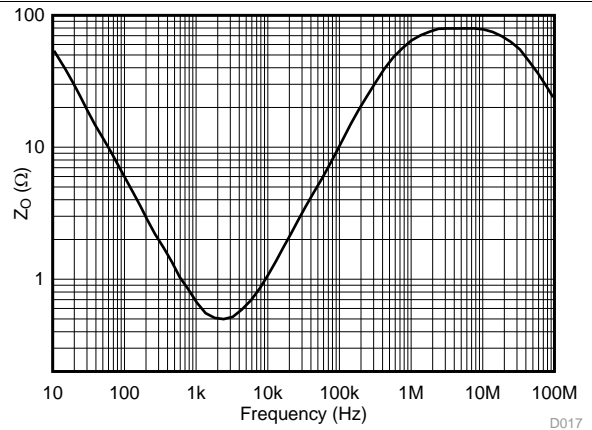


Figure 12. Open-Loop Output Impedance vs Frequency



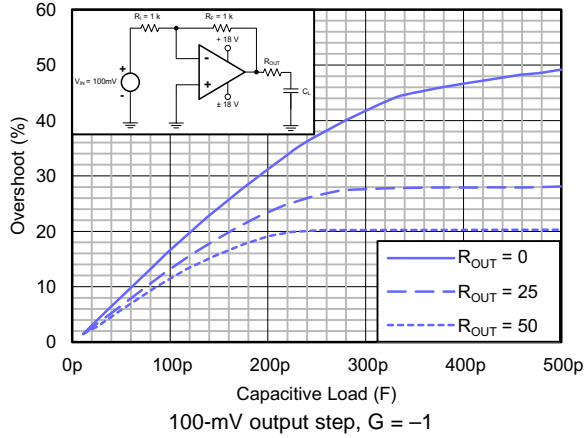


Figure 13. Small-Signal Overshoot vs Capacitive Load

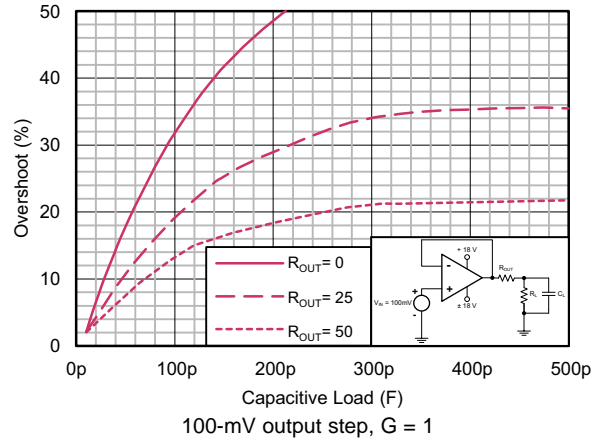


Figure 14. Small-Signal Overshoot vs Capacitive Load

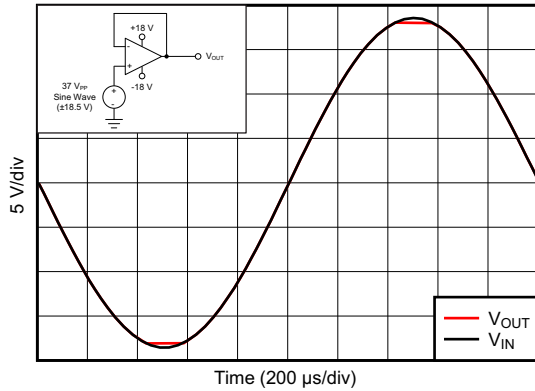


Figure 15. No Phase Reversal

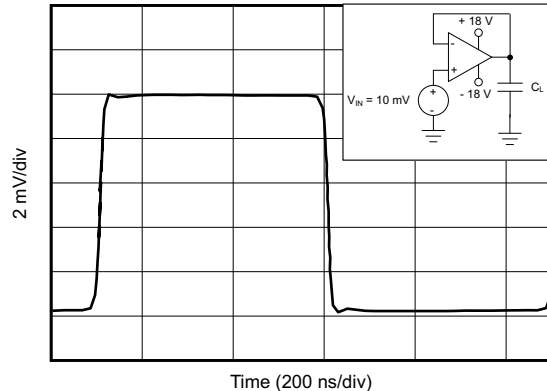


Figure 16. Small-Signal Step Response

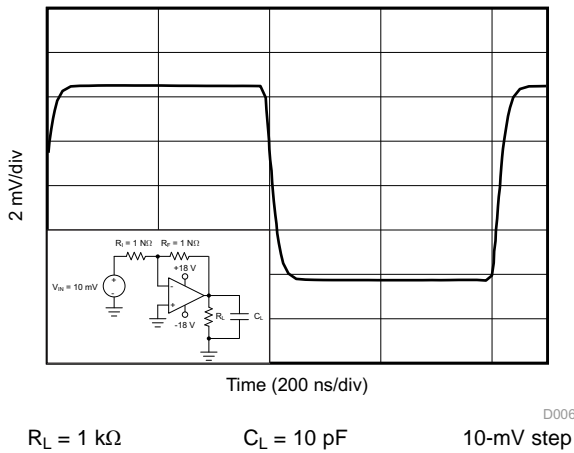


Figure 17. Small-Signal Step Response

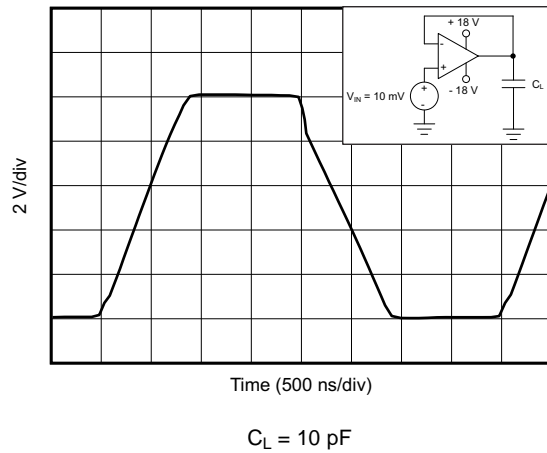
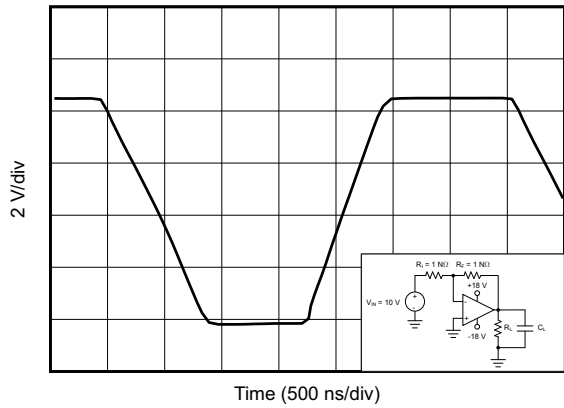


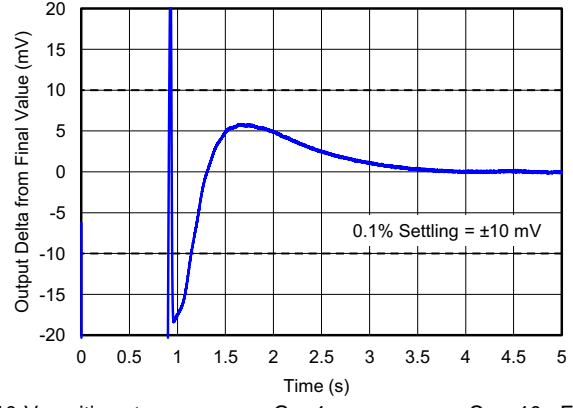
Figure 18. Large-Signal Step Response



$R_L = 1\text{ k}\Omega$        $C_L = 10\text{ pF}$

D005

Figure 19. Large-Signal Step Response

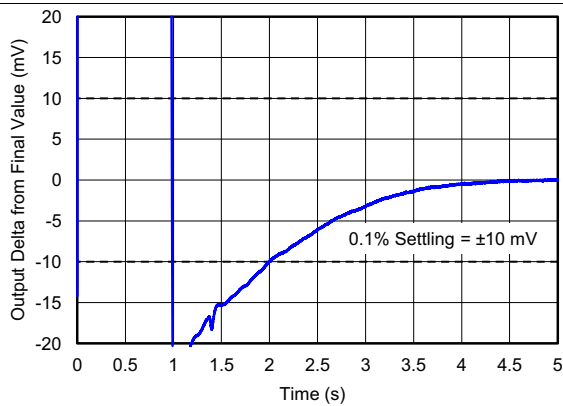


10-V positive step

$G = 1$

$C_L = 10\text{ pF}$

Figure 20. Large-Signal Settling Time

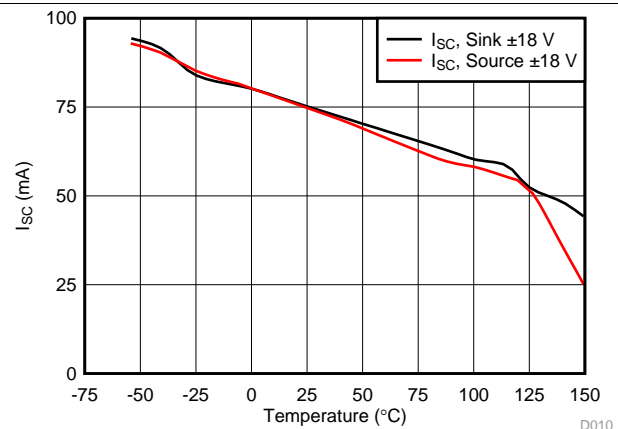


10-V negative step

$G = 1$

$C_L = 10\text{ pF}$

Figure 21. Large-Signal Settling Time



D010

Figure 22. Short-Circuit Current vs Temperature

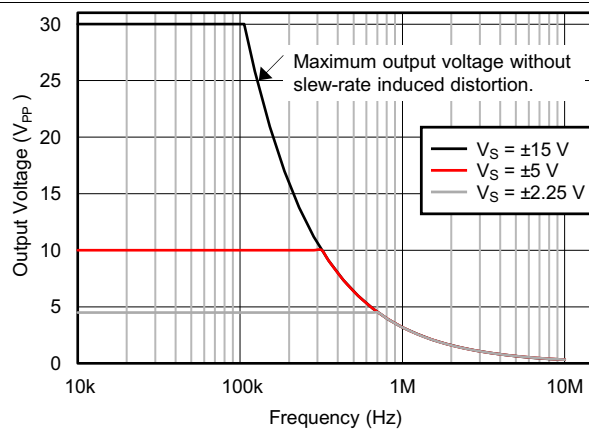
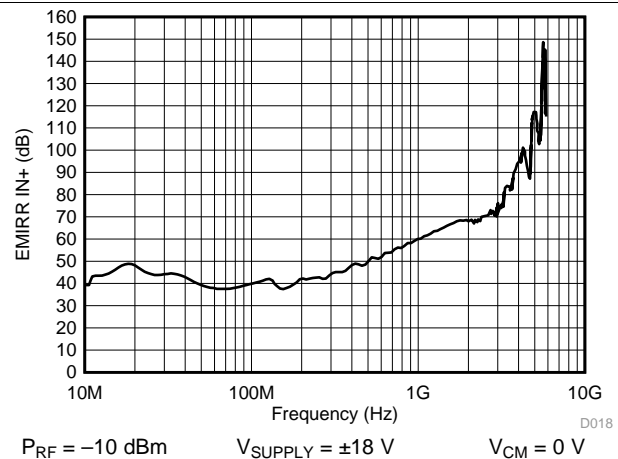


Figure 23. Maximum Output Voltage vs Frequency



$P_{RF} = -10\text{ dBm}$

$V_{SUPPLY} = \pm 18\text{ V}$

$V_{CM} = 0\text{ V}$

D018

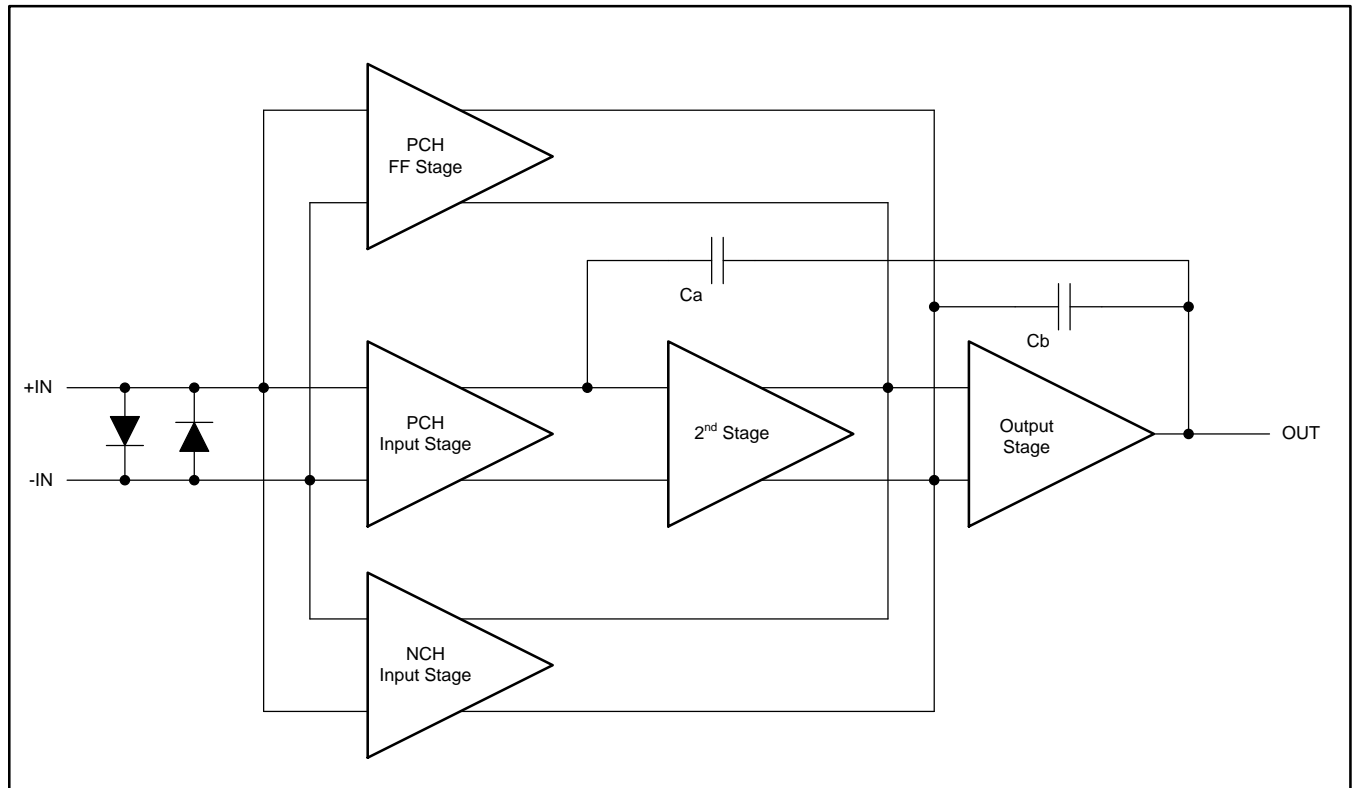
Figure 24. EMIRR IN+ vs Frequency

## 7 Detailed Description

### 7.1 Overview

The TLV2172-Q1 operational amplifier provides high overall performance, making these devices designed for many general-purpose applications. The excellent offset drift of only  $1 \mu\text{V}/^\circ\text{C}$  provides excellent stability over the entire temperature range. In addition, the device offers very good overall performance with high CMRR, PSRR, and  $A_{OL}$ .

### 7.2 Functional Block Diagram



Copyright © 2017, Texas Instruments Incorporated

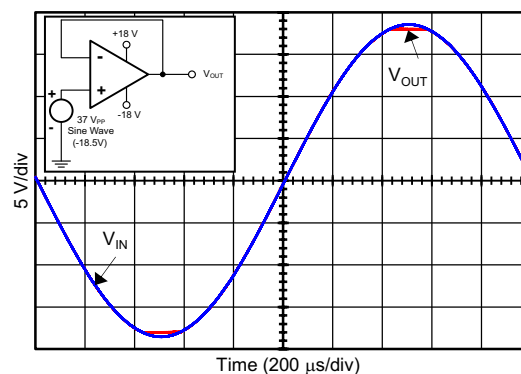
## 7.3 Feature Description

### 7.3.1 Operating Characteristics

The TLV2172-Q1 amplifier is specified for operation from 4.5 V to 36 V ( $\pm 2.25$  V to  $\pm 18$  V). Many of the specifications apply from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ . Parameters that can exhibit significant variance with regard to operating voltage or temperature are shown in the [Typical Characteristics](#) section.

### 7.3.2 Phase-Reversal Protection

The TLV2172-Q1 device has an internal phase-reversal protection. Many operational amplifiers exhibit a phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the TLV2172-Q1 prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. This performance is shown in [Figure 25](#).



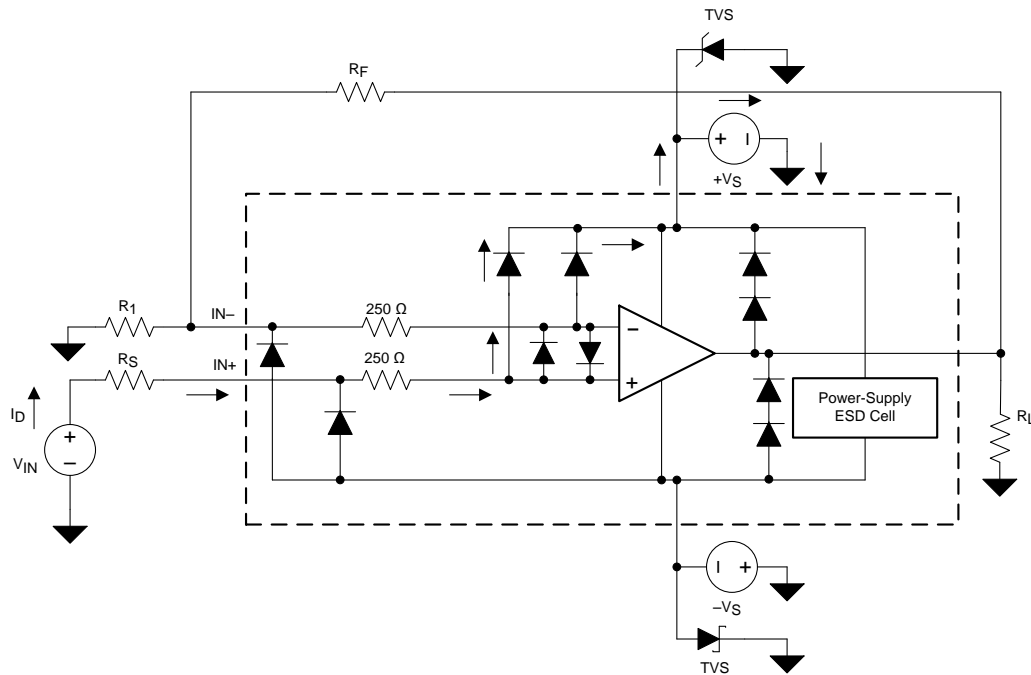
**Figure 25. No Phase Reversal**

### 7.3.3 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits for protection from accidental ESD events both before and during product assembly.

A good understanding of this basic ESD circuitry and the relevance to an electrical overstress event is helpful. [Figure 26](#) shows the ESD circuits contained in the TLV2172-Q1 (indicated by the dashed box). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

Feature Description (continued)



Copyright © 2016, Texas Instruments Incorporated

Figure 26. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse when discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device pins, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device can activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the TLV2172-Q1 but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit, as shown in Figure 26, the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances can arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some internal ESD protection circuits can turn on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

Figure 26 shows a specific example where the input voltage ( $V_{IN}$ ) exceeds the positive supply voltage ( $V+$ ) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If  $V+$  can sink the current, then one of the upper input steering diodes conducts and directs current to  $V+$ . Excessively high current levels can flow with increasingly higher  $V_{IN}$ . As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current,  $V_{IN}$  can begin sourcing current to the operational amplifier and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

### Feature Description (continued)

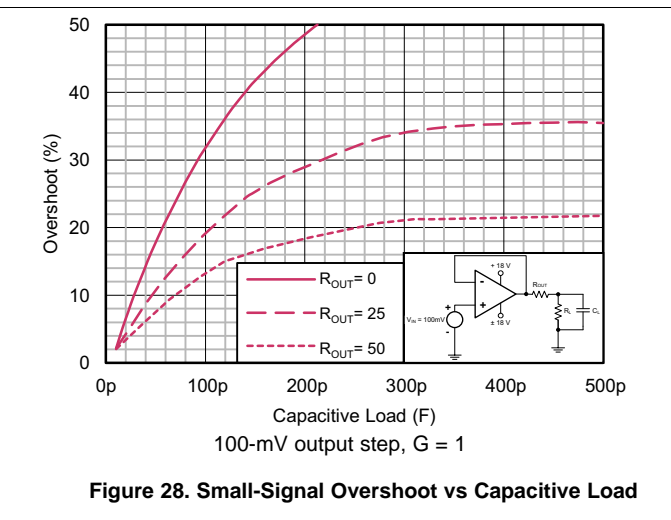
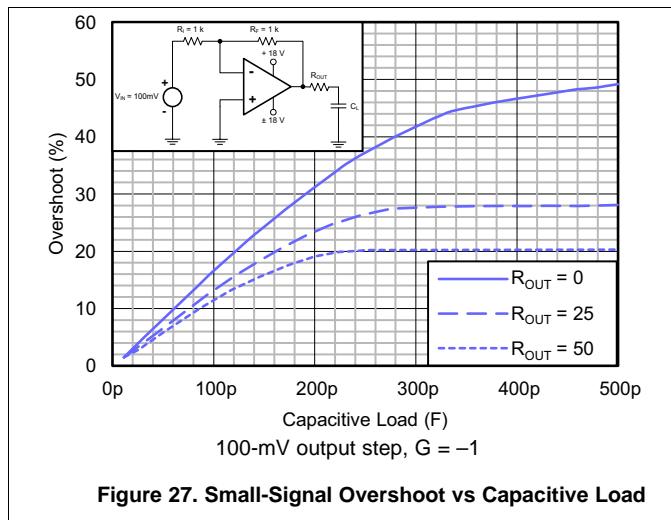
Another common question involves what happens to the amplifier if an input signal is applied to the input when the power supplies ( $V+$  or  $V-$ ) are at 0 V. Again, this question depends on the supply characteristic when at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the input source supplies the operational amplifier current through the current-steering diodes. This state is not a normal bias condition; most likely, the amplifier does not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, add external Zener diodes to the supply pins; see [Figure 26](#). Select the Zener voltage so that the diode does not turn on during normal operation. However, the Zener voltage must be low enough so that the Zener diode conducts if the supply pin begins to rise above the safe-operating, supply-voltage level.

The input pins of the TLV2172-Q1 are protected from excessive differential voltage with back-to-back diodes; see [Figure 26](#). In most circuit applications, the input protection circuitry has no effect. However, in low-gain or  $G = 1$  circuits, fast-ramping input signals can forward-bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. If the input signal is fast enough to create this forward-bias condition, then limit the input signal current to 10 mA or less. If the input signal current is not inherently limited, an input series resistor can limit the input signal current. This input series resistor degrades the low-noise performance of the TLV2172-Q1. [Figure 26](#) shows an example configuration that implements a current-limiting feedback resistor.

#### 7.3.4 Capacitive Load and Stability

The dynamic characteristics of the TLV2172-Q1 are optimized for common operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example,  $R_{OUT}$  equal to 50  $\Omega$ ) in series with the output. [Figure 27](#) and [Figure 28](#) show graphs of small-signal overshoot versus capacitive load for several values of  $R_{OUT}$ . See the [Feedback Plots Define Op Amp AC Performance](#) application note for details of analysis techniques and application circuits.



## 7.4 Device Functional Modes

### 7.4.1 Common-Mode Voltage Range

The input common-mode voltage range of the TLV2172-Q1 device extends 100 mV below the negative rail and within 2 V of the top rail for normal operation.

This device can operate with full rail-to-rail input 100 mV beyond the top rail, but with reduced performance within 2 V of the top rail. [Table 2](#) lists the typical performances in this range.

**Table 2. Typical Performance for Common-Mode Voltages Within 2 V of the Positive Supply**

PARAMETER	MIN	TYP	MAX	UNIT
Input common-mode voltage	$(V+) - 2$		$(V+) + 0.1$	V
Offset voltage		7		mV
Offset voltage vs temperature		12		$\mu\text{V}/^\circ\text{C}$
Common-mode rejection		65		dB
Open-loop gain		60		dB
Gain-bandwidth product		0.3		MHz
Slew rate		0.3		V/ $\mu\text{s}$

### 7.4.2 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from the saturated state to the linear state. The output devices of the operational amplifier enter the saturation region when the output voltage exceeds the rated operating voltage, which is a result from the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the normal state. After the charge carriers return back to the equilibrium state, the device begins to slew at the normal slew rate. As a result, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the TLV2172-Q1 is approximately 2  $\mu\text{s}$ .

## 8 Application and Implementation

### NOTE

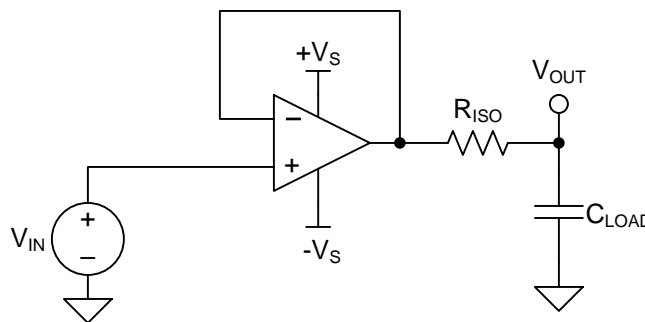
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The TLV2172-Q1 operational amplifier provides high overall performance in a large number of general-purpose applications. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors placed close to the device pins. In most cases, 0.1- $\mu$ F capacitors are adequate. Follow the additional recommendations in the [Layout Guidelines](#) section to achieve the maximum performance from this device. Many applications introduce capacitive loading to the output of the amplifier (which potentially causes instability). To stabilize the amplifier, add an isolation resistor between the amplifier output and the capacitive load. [Typical Application](#) section shows the process for selecting a resistor.

### 8.2 Typical Application

This circuit can drive capacitive loads (such as cable shields, reference buffers, MOSFET gates, and diodes). The circuit uses an isolation resistor ( $R_{ISO}$ ) to stabilize the output of an operational amplifier.  $R_{ISO}$  modifies the open-loop gain of the system to ensure that the circuit has sufficient phase margin.



Copyright © 2017, Texas Instruments Incorporated

**Figure 29. Unity-Gain Buffer With  $R_{ISO}$  Stability Compensation**

#### 8.2.1 Design Requirements

The design requirements are:

- Supply voltage: 30 V ( $\pm 15$  V)
- Capacitive loads: 100 pF, 1000 pF, 0.01  $\mu$ F, 0.1  $\mu$ F, and 1  $\mu$ F
- Phase margin: 45° and 60°

#### 8.2.2 Detailed Design Procedure

[Figure 29](#) shows a unity-gain buffer driving a capacitive load. [Equation 1](#) shows the transfer function for the circuit in [Figure 29](#). [Figure 29](#) does not show the open-loop output resistance of the operational amplifier ( $R_o$ ).

$$T(s) = \frac{1 + C_{LOAD} \times R_{ISO} \times s}{1 + (R_o + R_{ISO}) \times C_{LOAD} \times s} \quad (1)$$

The transfer function in [Equation 1](#) has a pole and a zero. The frequency of the pole ( $f_p$ ) is determined by  $(R_o + R_{ISO})$  and  $C_{LOAD}$ . The  $R_{ISO}$  and  $C_{LOAD}$  components determine the frequency of the zero ( $f_z$ ). A stable system is obtained by selecting  $R_{ISO}$  so that the rate of closure (ROC) between the open-loop gain ( $A_{OL}$ ) and  $1/\beta$  is 20 dB per decade. [Figure 30](#) shows the concept. The  $1/\beta$  curve for a unity-gain buffer is 0 dB.



Typical Application (continued)

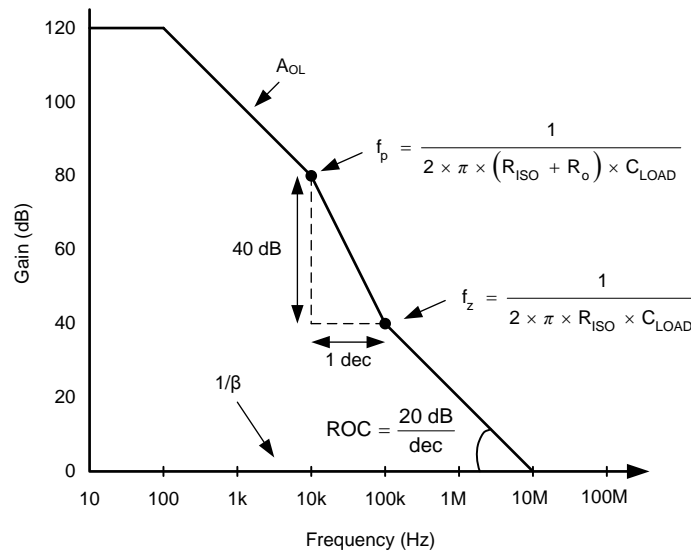


Figure 30. Unity-Gain Amplifier With R<sub>ISO</sub> Compensation

Typically, ROC stability analysis is simulated. The validity of the analysis depends on multiple factors, especially the accurate modeling of R<sub>o</sub>. In addition to simulating the ROC, a robust stability analysis includes a measurement of overshoot percentage and AC gain peaking of the circuit using a function generator, oscilloscope, and gain and phase analyzer. Phase margin is then calculated from these measurements. Table 3 shows the overshoot percentage and AC gain peaking that correspond to phase margins of 45° and 60°. For more details on this design and other alternative devices that can replace the TLV2172-Q1, see the [Capacitive Load Drive Solution Using an Isolation Resistor](#) precision design.

Table 3. Phase Margin versus Overshoot and AC Gain Peaking

PHASE MARGIN	OVERSHOOT	AC GAIN PEAKING
45°	23.3%	2.35 dB
60°	8.8%	0.28 dB

8.2.3 Application Curve

The values of R<sub>ISO</sub> that yield phase margins of 45° and 60° for various capacitive loads are determined using the described methodology. Figure 31 shows the results.

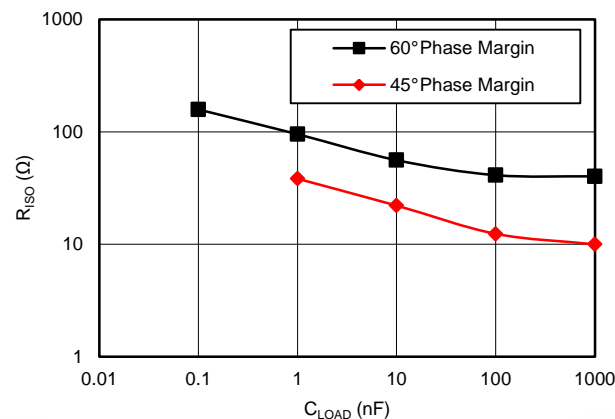


Figure 31. Isolation Resistor Required for Various Capacitive Loads to Achieve a Target Phase Margin

## 9 Power Supply Recommendations

The TLV2172-Q1 is specified for operation from 4.5 V to 36 V ( $\pm 2.25$  V to  $\pm 18$  V); many specifications apply from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ . Parameters that can exhibit significant variance with regard to operating voltage or temperature are shown in the [Typical Characteristics](#) section.

### CAUTION

Supply voltages larger than 40 V can permanently damage the device; see the [Absolute Maximum Ratings](#) table.

Place 0.1- $\mu\text{F}$  bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the [Layout](#) section.

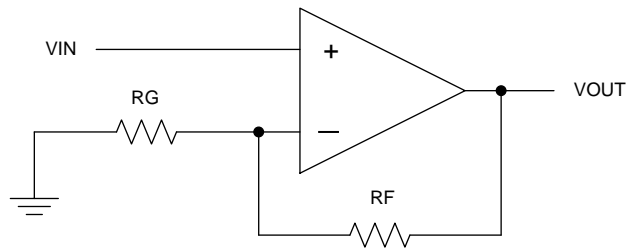
## 10 Layout

### 10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

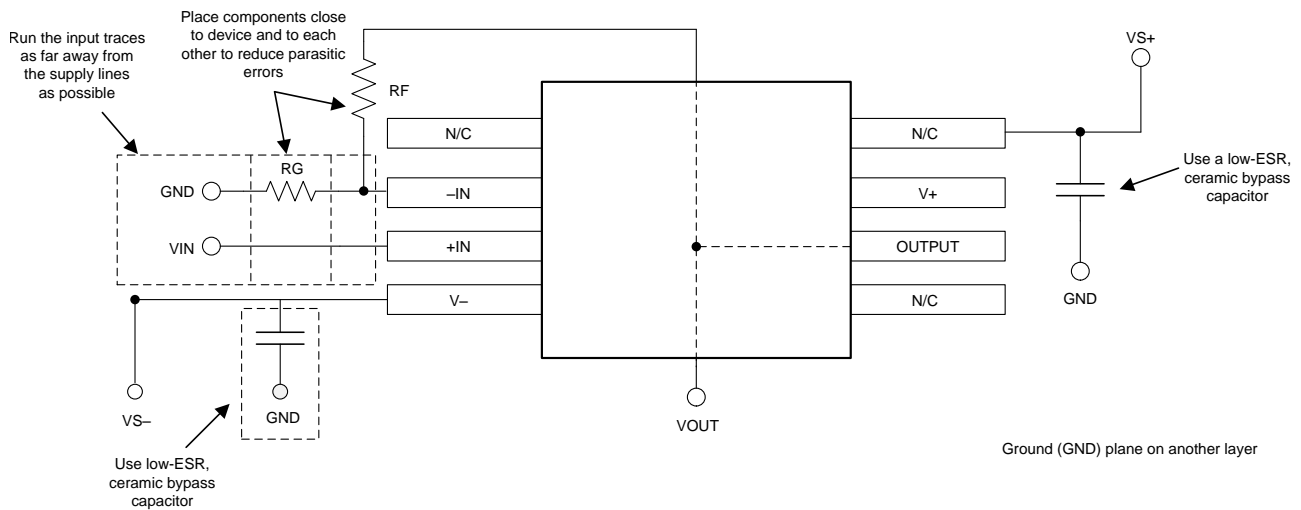
- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1- $\mu\text{F}$  ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in [Figure 33](#), keeping  $R_F$  and  $R_G$  close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

## 10.2 Layout Example



Copyright © 2017, Texas Instruments Incorporated

**Figure 32. Schematic Representation**



Copyright © 2017, Texas Instruments Incorporated

**Figure 33. Operational Amplifier Board Layout for a Noninverting Configuration**

## 11 Device and Documentation Support

### 11.1 Device Support

#### 11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

#### 11.1.2 Development Support

##### 11.1.2.1 TINA-TI™ (Free Software Download)

TINA-TI™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI™ is a free, fully-functional version of the TINA software, preloaded with a library of macromodels in addition to a range of both passive and active models. TINA-TI™ provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a [free download](#) from the Analog eLab Design Center, TINA-TI™ offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, thus creating a dynamic quick-start tool.

---

#### NOTE

These files require that either the TINA software (from DesignSoft™) or the TINA-TI™ software be installed. Download the free TINA-TI™ software from the [TINA-TI™ folder](#).

---

##### 11.1.2.2 DIP Adapter EVM

The [DIP Adapter EVM](#) tool provides an easy, low-cost way to prototype small surface-mount devices. The evaluation tool uses these TI packages: D or U (SOIC-8), PW (TSSOP-8), DGK (VSSOP-8), DBV (SOT23-6, SOT23-5, and SOT23-3), DCK (SC70-6 and SC70-5), and DRL (SOT563-6). The DIP adapter EVM can also be used with terminal strips or can be wired directly to existing circuits.

##### 11.1.2.3 Universal Op Amp EVM

The [Universal Op Amp EVM](#) is a series of general-purpose, blank circuit boards that simplify prototyping circuits for a variety of device package types. The evaluation module board design allows many different circuits to be constructed easily and quickly. Five models are offered, with each model intended for a specific package type. PDIP, SOIC, VSSOP, TSSOP, and SOT23 packages are all supported.

---

#### NOTE

These boards are unpopulated, so users must provide their own devices. TI recommends requesting several op amp device samples when ordering the Universal Op Amp EVM.

---

##### 11.1.2.4 TI Precision Designs

TI precision designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, a complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI precision designs are available online at [www.ti.com/ww/en/analog/precision-designs/](http://www.ti.com/ww/en/analog/precision-designs/).

##### 11.1.2.5 WEBENCH® Filter Designer

The [WEBENCH® Filter Designer](#) is a simple, powerful, and easy-to-use active filter design program. The WEBENCH® Filter Designer allows optimized filter designs to be created by using a selection of TI operational amplifiers and passive components from TI's vendor partners.

## Device Support (continued)

Available as a web-based tool from the WEBENCH® design center, the WEBENCH® filter designer allows complete multistage active filter solutions to be designed, optimized, and simulated within minutes.

### 11.2 Documentation Support

#### 11.2.1 Related Documentation

For related documentation see the following:

- [Feedback Plots Define Op Amp AC Performance](#)
- [EMI Rejection Ratio of Operational Amplifiers](#)
- [Compensate Transimpedance Amplifiers Intuitively](#)
- [Noise Analysis for High-Speed Op Amps](#)

### 11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

### 11.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.6 Trademarks

TINA-TI, E2E are trademarks of Texas Instruments.

WEBENCH is a registered trademark of Texas Instruments.

DesignSoft is a trademark of DesignSoft, Inc.

All other trademarks are the property of their respective owners.

### 11.7 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.8 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TLV2172QDQGRQ1</a>	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1IQ6
TLV2172QDQGRQ1.Z	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1IQ6

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TLV2172-Q1 :**

- Catalog : [TLV2172](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2172QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1



**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2172QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0

# DGK0008A



# PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

**NOTES:**

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DGK0008A

<sup>TM</sup> VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2025, Texas Instruments Incorporated