

# TLV2422, TLV2422A, TLV2422Y Advanced LinCMOS™ RAIL-TO-RAIL OUTPUT WIDE-INPUT-VOLTAGE MICROPOWER DUAL OPERATIONAL AMPLIFIERS

SLOS199C – SEPTEMBER 1997 – REVISED APRIL 2001

- Output Swing Includes Both Supply Rails
- Extended Common-Mode Input Voltage Range . . . 0 V to 4.5 V (Min) With 5-V Single Supply
- No Phase Inversion
- Low Noise . . . 18 nV/√Hz Typ at f = 1 kHz
- Low Input Offset Voltage  
950 μV Max at T<sub>A</sub> = 25°C (TLV2422A)
- Low Input Bias Current . . . 1 pA Typ
- Micropower Operation . . . 50 μA Per Channel
- 600-Ω Output Drive
- Available in Q-Temp Automotive  
HighRel Automotive Applications  
Configuration Control / Print Support  
Qualification to Automotive Standards

## description

The TLV2422 and TLV2422A are dual low-voltage operational amplifiers from Texas Instruments. The common-mode input voltage range for this device has been extended over the typical CMOS amplifiers making them suitable for a wide range of applications. In addition, the devices do not phase invert when the common-mode input is driven to the supply rails. This satisfies most design requirements without paying a premium for rail-to-rail input performance. They also exhibit rail-to-rail output performance for increased dynamic range in single- or split-supply applications. This family is fully characterized at 3-V and 5-V supplies and is optimized for low-voltage operation. The TLV2422 only requires 50 μA of supply current per channel, making it ideal for battery-powered applications. The TLV2422 also has increased output drive over previous rail-to-rail operational amplifiers and can drive 600-Ω loads for telecom applications.

Other members in the TLV2422 family are the high-power, TLV2442, and low-power, TLV2432, versions.

The TLV2422, exhibiting high input impedance and low noise, is excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micropower dissipation levels and low-voltage operation, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single- or split-supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs). For precision applications, the TLV2422A is available with a maximum input offset voltage of 950 μV.

If the design requires single operational amplifiers, see the TI TLV2211/21/31. This is a family of rail-to-rail output operational amplifiers in the SOT-23 package. Their small size and low power consumption, make them ideal for high density, battery-powered equipment.

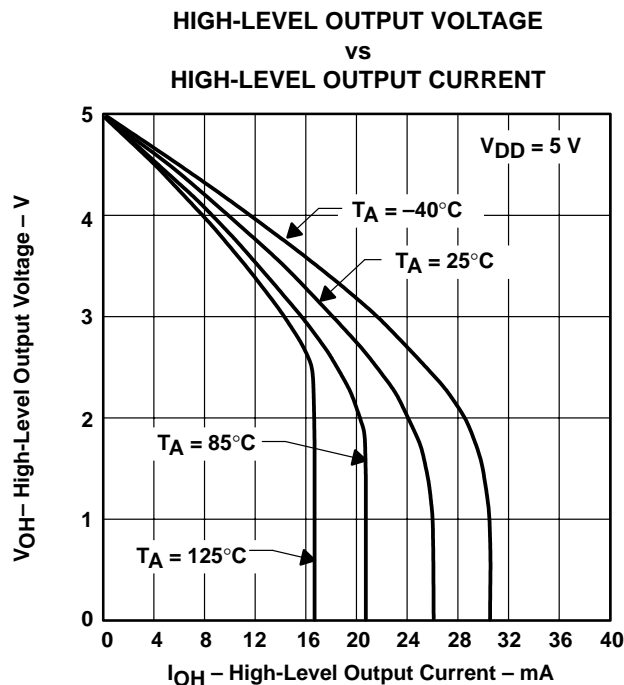


Figure 1



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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# TLV2422, TLV2422A, TLV2422Y

## Advanced LinCMOS™ RAIL-TO-RAIL OUTPUT

### WIDE-INPUT-VOLTAGE MICROPOWER DUAL OPERATIONAL AMPLIFIERS

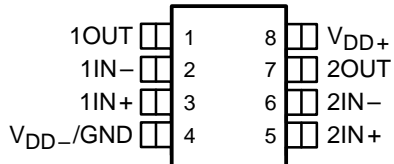
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#### AVAILABLE OPTIONS

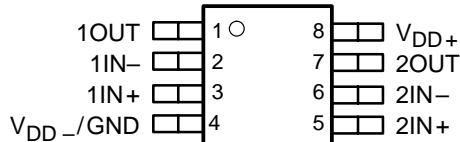
T <sub>A</sub>	V <sub>IO</sub> max AT 25°C	PACKAGED DEVICES					CHIP FORM (Y)
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	TSSOP (PW)	CERAMIC FLAT PACK (U)	
0°C to 70°C	2.5 mV	TLV2422CD	—	—	TLV2422CPWLE	—	TLV2422Y
–40°C to 85°C	950 μV 2.5 mV	TLV2422AID TLV2422ID	— —	— —	TLV2422AIPWLE —	— —	
–40°C to 125°C	950 μV 2.5 mV	TLV2422AQD TLV2422QD	— —	— —	— —	— —	
–55°C to 125°C	950 μV 2 mV	— —	TLV2422AMFK TLV2422MFK	TLV2422AMJG TLV2422MJG	— —	TLV2422AMU TLV2422MU	

The D packages are available taped and reeled. Add R suffix to device type (e.g., TLV2422CDR). The PW package is available only left-end taped and reeled. Chips are tested at 25°C.

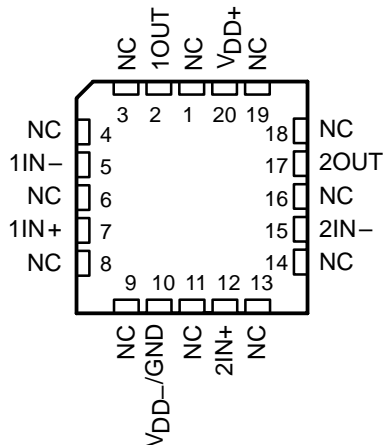
**D OR JG PACKAGE  
(TOP VIEW)**



**PW PACKAGE  
(TOP VIEW)**

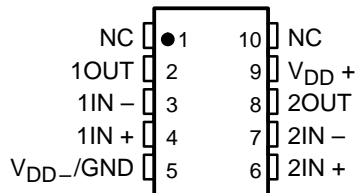


**FK PACKAGE  
(TOP VIEW)**

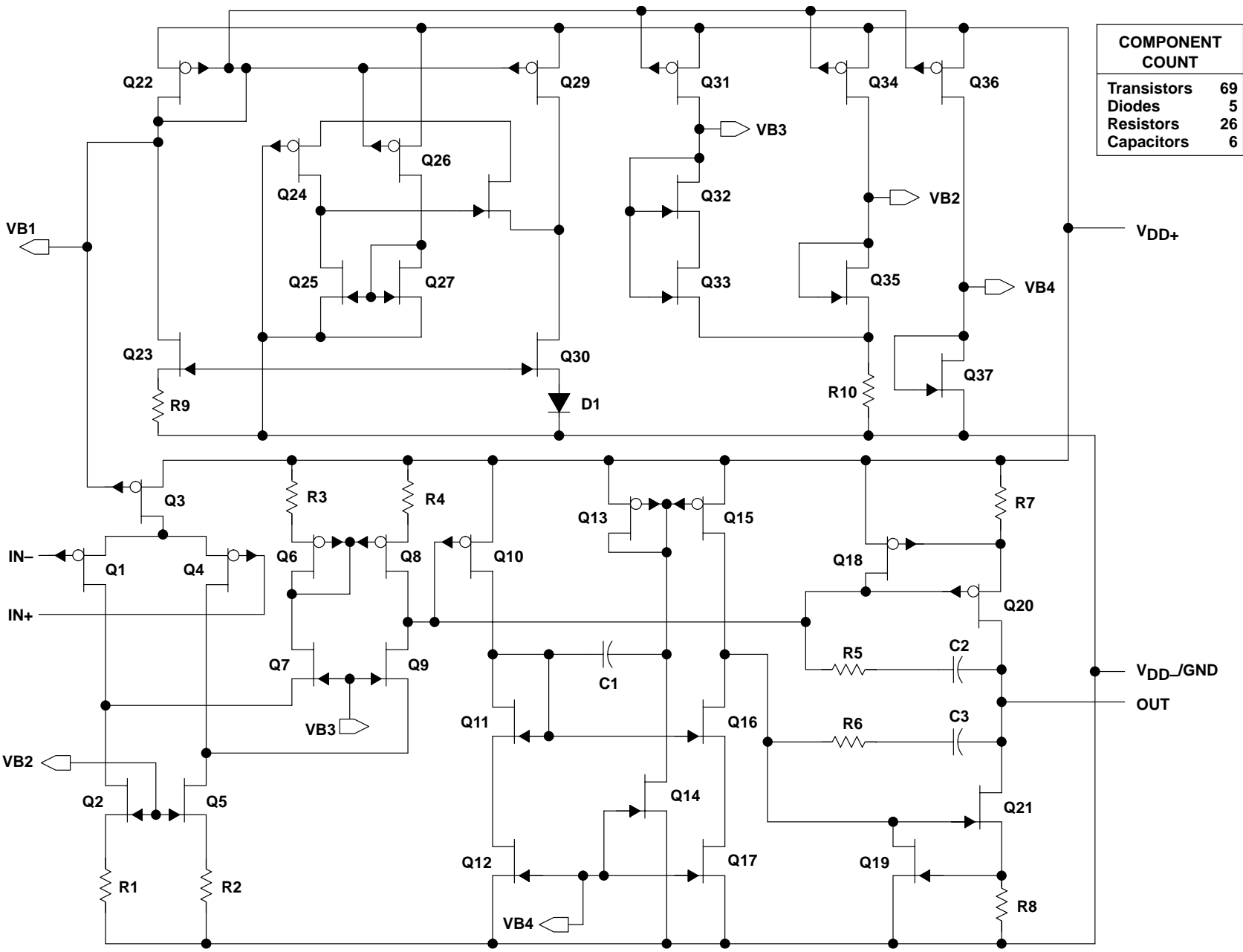


NC – No internal connection

**U PACKAGE  
(TOP VIEW)**



equivalent schematic (each amplifier)



COMPONENT COUNT	
Transistors	69
Diodes	5
Resistors	26
Capacitors	6

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage, $V_{DD}$ (see Note 1)	12 V
Differential input voltage, $V_{ID}$ (see Note 2)	$\pm V_{DD}$
Input voltage, $V_I$ (any input, see Note 1): C and I suffix	-0.3 V to $V_{DD}$
Input current, $I_I$ (each input)	$\pm 5$ mA
Output current, $I_O$	$\pm 50$ mA
Total current into $V_{DD+}$	$\pm 50$ mA
Total current out of $V_{DD-}$	$\pm 50$ mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, $T_A$ : C suffix	0°C to 70°C
I suffix	-40°C to 85°C
Q suffix	-40°C to 125°C
M suffix	-55°C to 125°C
Storage temperature range, $T_{stg}$	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between  $V_{DD+}$  and  $V_{DD-}$ .  
 2. Differential voltages are at  $IN+$  with respect to  $IN-$ . Excessive current flows if input is brought below  $V_{DD-} - 0.3$  V.  
 3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

**DISSIPATION RATING TABLE**

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
PW	525 mW	4.2 mW/°C	336 mW	273 mW	105 mW
U	675 mW	5.4 mW/°C	432 mW	350 mW	135 mW

**recommended operating conditions**

	C SUFFIX		I SUFFIX		Q SUFFIX		M SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{DD\pm}$	2.7	10	2.7	10	2.7	10	2.7	10	V
Input voltage range, $V_I$	$V_{DD-}$	$V_{DD+} - 0.8$	$V_{DD-}$	$V_{DD+} - 0.8$	$V_{DD-}$	$V_{DD+} - 0.8$	$V_{DD-}$	$V_{DD+} - 0.8$	V
Common-mode input voltage, $V_{IC}$	$V_{DD-}$	$V_{DD+} - 0.8$	$V_{DD-}$	$V_{DD+} - 0.8$	$V_{DD-}$	$V_{DD+} - 0.8$	$V_{DD-}$	$V_{DD+} - 0.8$	V
Operating free-air temperature, $T_A$	0	70	-40	85	-40	125	-55	125	°C



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**electrical characteristics at specified free-air temperature,  $V_{DD} = 3\text{ V}$  (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$T_A$ †	TLV2422C			UNIT
			MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_{IC} = 0,$ $V_O = 0,$ $V_{DD} \pm = \pm 2.5\text{ V},$ $R_S = 50\ \Omega$	25°C	300	2000	$\mu\text{V}$	
		Full range	2500			
$\alpha_{VIO}$ Temperature coefficient of input offset voltage		25°C to 70°C	2		$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 4)		25°C	0.003		$\mu\text{V}/\text{mo}$	
$I_{IO}$ Input offset current		25°C	0.5	60	$\text{pA}$	
		Full range	150			
$I_{IB}$ Input bias current		25°C	1	60	$\text{pA}$	
		Full range	150			
$V_{ICR}$ Common-mode input voltage range		$ V_{IO}  \leq 5\text{ mV},$ $R_S = 50\ \Omega$	25°C	0 to 2.5	-0.25 to 2.75	$\text{V}$
			Full range	0 to 2.2		
$V_{OH}$ High-level output voltage	$I_{OH} = -100\ \mu\text{A}$	25°C	2.97		$\text{V}$	
		25°C	2.75			
		Full range	2.5			
$V_{OL}$ Low-level output voltage	$V_{IC} = 0,$ $I_{OL} = 100\ \mu\text{A}$	25°C	0.05		$\text{V}$	
		25°C	0.2			
		Full range	0.5			
$A_{VD}$ Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V},$ $V_O = 1\text{ V to }2\text{ V}$	25°C	$R_L = 10\ \text{k}\Omega^\ddagger$		$\text{V/mV}$	
			6 10			
		Full range	3			
$r_{i(d)}$ Differential input resistance		25°C	$R_L = 1\ \text{M}\Omega^\ddagger$		$\Omega$	
			700			
$r_{i(c)}$ Common-mode input resistance		25°C	$10^{12}$		$\Omega$	
$c_{i(c)}$ Common-mode input capacitance	$f = 10\ \text{kHz}$	25°C	8		$\text{pF}$	
$z_o$ Closed-loop output impedance	$f = 100\ \text{kHz},$ $A_V = 10$	25°C	130		$\Omega$	
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }2.5\text{ V},$ $V_O = 1.5\text{ V},$ $R_S = 50\ \Omega$	25°C	70	83	$\text{dB}$	
		Full range	70			
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{DD}/\Delta V_{IO}$ )	$V_{DD} = 2.7\text{ V to }8\text{ V},$ $V_{IC} = V_{DD}/2,$ No load	25°C	80	95	$\text{dB}$	
		Full range	80			
$I_{DD}$ Supply current	$V_O = 1.5\text{ V},$ No load	25°C	100	150	$\mu\text{A}$	
		Full range	175			

† Full range is 0°C to 70°C.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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**electrical characteristics at specified free-air temperature,  $V_{DD} = 3\text{ V}$  (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$T_A$ †	TLV2422I			TLV2422AI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_{IC} = 0, V_O = 0, V_{DD} \pm = \pm 2.5\text{ V}, R_S = 50\ \Omega$	25°C	300	2000		300	950	$\mu\text{V}$	
		Full range		2500		1500			
$\alpha_{V_{IO}}$ Temperature coefficient of input offset voltage		25°C to 70°C	2			2		$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 4)		25°C	0.003			0.003		$\mu\text{V}/\text{mo}$	
$I_{IO}$ Input offset current		25°C	0.5	60		0.5	60	$\text{pA}$	
		Full range		150		150			
$I_{IB}$ Input bias current	25°C	1	60		1	60	$\text{pA}$		
	Full range		150		150				
$V_{ICR}$ Common-mode input voltage range	$ V_{IO}  \leq 5\text{ mV}, R_S = 50\ \Omega$	25°C	0 to 2.5	-0.25 to 2.75		0 to 2.5	-0.25 to 2.75	$\text{V}$	
		Full range	0 to 2.2			0 to 2.2			
$V_{OH}$ High-level output voltage	$I_{OH} = -100\ \mu\text{A}$ $I_{OH} = -500\ \mu\text{A}$	25°C	2.97			2.97		$\text{V}$	
		25°C	2.75			2.75			
		Full range	2.5			2.5			
$V_{OL}$ Low-level output voltage	$V_{IC} = 0, I_{OL} = 100\ \mu\text{A}$ $V_{IC} = 0, I_{OL} = 250\ \mu\text{A}$	25°C	0.05			0.05		$\text{V}$	
		25°C	0.2			0.2			
		Full range		0.5		0.5			
$A_{VD}$ Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}, V_O = 1\text{ V to } 2\text{ V}$ $R_L = 10\text{ k}\Omega \ddagger$ $R_L = 1\text{ M}\Omega \ddagger$	25°C	6	10		6	10	$\text{V}/\text{mV}$	
		Full range	3			3			
		25°C	700			700			
$r_{i(d)}$ Differential input resistance		25°C	$10^{12}$			$10^{12}$	$\Omega$		
$r_{i(c)}$ Common-mode input resistance		25°C	$10^{12}$			$10^{12}$	$\Omega$		
$C_{i(c)}$ Common-mode input capacitance	$f = 10\text{ kHz}$	25°C	8			8	$\text{pF}$		
$z_o$ Closed-loop output impedance	$f = 100\text{ kHz}, A_V = 10$	25°C	130			130	$\Omega$		
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to } 2.5\text{ V}, V_O = 1.5\text{ V}, R_S = 50\ \Omega$	25°C	70	83		70	83	$\text{dB}$	
		Full range	70			70			
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{DD}/\Delta V_{IO}$ )	$V_{DD} = 2.7\text{ V to } 8\text{ V}, V_{IC} = V_{DD}/2, \text{ No load}$	25°C	80	95		80	95	$\text{dB}$	
		Full range	80			80			
$I_{DD}$ Supply current	$V_O = 1.5\text{ V}, \text{ No load}$	25°C	100	150		100	150	$\mu\text{A}$	
		Full range		175		175			

† Full range is -40°C to 85°C.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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**operating characteristics at specified free-air temperature,  $V_{DD} = 3\text{ V}$**

PARAMETER		TEST CONDITIONS		$T_A$ †	TLV2422C, TLV2422I TLV2422AI			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = 1.5\text{ V to }3.5\text{ V}, R_L = 10\text{ k}\Omega\ddagger, C_L = 100\text{ pF}\ddagger$		25°C	0.01	0.02	$\text{V}/\mu\text{s}$	
				Full range	0.008			
$V_n$	Equivalent input noise voltage	f = 10 Hz		25°C	100		$\text{nV}/\sqrt{\text{Hz}}$	
		f = 1 kHz		25°C	23			
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C	2.7		$\mu\text{V}$	
		f = 0.1 Hz to 10 Hz		25°C	4			
$I_n$	Equivalent input noise current			25°C	0.6		$\text{fA}/\sqrt{\text{Hz}}$	
THD + N	Total harmonic distortion plus noise	$V_O = 0.5\text{ V to }2.5\text{ V}, f = 1\text{ kHz}, R_L = 10\text{ k}\Omega\ddagger$		25°C	$A_V = 1$	0.25%		
					$A_V = 10$	1.8%		
	Gain-bandwidth product	f = 10 kHz, $C_L = 100\text{ pF}\ddagger$	$R_L = 10\text{ k}\Omega\ddagger$	25°C	46		kHz	
BOM	Maximum output-swing bandwidth	$V_{O(PP)} = 1\text{ V}, R_L = 10\text{ k}\Omega\ddagger$	$A_V = 1, C_L = 100\text{ pF}\ddagger$	25°C	8.3		kHz	
$t_s$	Settling time	$A_V = -1, \text{ Step} = 0.5\text{ V to }2.5\text{ V}, R_L = 10\text{ k}\Omega\ddagger, C_L = 100\text{ pF}\ddagger$		25°C	To 0.1%	8.6	$\mu\text{s}$	
					To 0.01%	16		
$\phi_m$	Phase margin at unity gain	$R_L = 10\text{ k}\Omega\ddagger, C_L = 100\text{ pF}\ddagger$		25°C	62°			
	Gain margin			25°C	11			dB

† Full range for the C version is 0°C to 70°C. Full range for the I version is -40°C to 85°C.

‡ Referenced to 2.5 V

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**electrical characteristics at specified free-air temperature,  $V_{DD} = 3\text{ V}$  (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$T_A$ †	TLV2422Q, TLV2422M			TLV2422AQ, TLV2422AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_{IC} = 0,$ $V_O = 0,$ $V_{DD} \pm = \pm 1.5\text{ V},$ $R_S = 50\ \Omega$	25°C	300	2000		300	950	$\mu\text{V}$	
		Full range			2500		1800		
$\alpha_{V_{IO}}$ Temperature coefficient of input offset voltage		Full range	2			2		$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 4)		25°C	0.003			0.003		$\mu\text{V}/\text{mo}$	
$I_{IO}$ Input offset current		25°C	0.5	60		0.5	60	$\text{pA}$	
		Full range			150		150		
$I_{IB}$ Input bias current	25°C	1	60		1	60	$\text{pA}$		
	Full range			300		300			
$V_{ICR}$ Common-mode input voltage range	$ V_{IO}  \leq 5\text{ mV},$ $R_S = 50\ \Omega$	25°C	0 to 2.5	-0.25 to 2.75		0 to 2.5	-0.25 to 2.75	$\text{V}$	
		Full range	0 to 2.2			0 to 2.2			
$V_{OH}$ High-level output voltage	$I_{OH} = -100\ \mu\text{A}$ $I_{OH} = -500\ \mu\text{A}$	25°C	2.97			2.97		$\text{V}$	
		25°C	2.75			2.75			
		Full range	2.5			2.5			
$V_{OL}$ Low-level output voltage	$V_{IC} = 0,$ $I_{OL} = 100\ \mu\text{A}$ $V_{IC} = 0,$ $I_{OL} = 250\ \mu\text{A}$	25°C	0.05			0.05		$\text{V}$	
		25°C	0.2			0.2			
		Full range			0.5		0.5		
$A_{VD}$ Large-signal differential voltage amplification	$V_{IC} = 1.5\text{ V},$ $V_O = 1\text{ V to } 2\text{ V}$	25°C	$R_L = 10\ \text{k}\Omega \ddagger$		6	10	6	10	$\text{V/mV}$
			$R_L = 1\ \text{M}\Omega \ddagger$		700		700		
		Full range	2		2				
$r_{i(d)}$ Differential input resistance		25°C	$10^{12}$			$10^{12}$			$\Omega$
$r_{i(c)}$ Common-mode input resistance		25°C	$10^{12}$			$10^{12}$			$\Omega$
$C_{i(c)}$ Common-mode input capacitance	$f = 10\ \text{kHz}$	25°C	8			8			$\text{pF}$
$z_o$ Closed-loop output impedance	$f = 100\ \text{kHz},$ $A_V = 10$	25°C	130			130			$\Omega$
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR}\ \text{min},$ $V_O = 1.5\text{ V},$ $R_S = 50\ \Omega$	25°C	70	83		70	83	$\text{dB}$	
		Full range	70			70			
kSVR Supply-voltage rejection ratio ( $\Delta V_{DD}/\Delta V_{IO}$ )	$V_{DD} = 2.7\text{ V to } 8\text{ V},$ $V_{IC} = V_{DD}/2,$ No load	25°C	80	95		80	95	$\text{dB}$	
		Full range	80			80			
$I_{DD}$ Supply current	$V_O = 1.5\text{ V},$ No load	25°C	100	150		100	150	$\mu\text{A}$	
		Full range			175		175		

† Full range is  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  for Q level part,  $-55^\circ\text{C}$  to  $125^\circ\text{C}$  for M level part.

‡ Referenced to 1.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.





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operating characteristics at specified free-air temperature,  $V_{DD} = 3\text{ V}$

PARAMETER	TEST CONDITIONS	$T_A$ †	TLV2422Q, TLV2422M, TLV2422AQ, TLV2422AM			UNIT
			MIN	TYP	MAX	
SR Slew rate at unity gain	$V_O = 1.1\text{ V to }1.9\text{ V},$ $R_L = 10\text{ k}\Omega\ddagger,$ $C_L = 100\text{ pF}\ddagger$	25°C	0.01	0.02		V/ $\mu\text{s}$
		Full range	0.008			
$V_n$ Equivalent input noise voltage	$f = 10\text{ Hz}$	25°C	100		nV/ $\sqrt{\text{Hz}}$	
	$f = 1\text{ kHz}$	25°C	23			
$V_{N(PP)}$ Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$	25°C	2.7		$\mu\text{V}$	
	$f = 0.1\text{ Hz to }10\text{ Hz}$	25°C	4			
$I_n$ Equivalent input noise current		25°C	0.6		fA/ $\sqrt{\text{Hz}}$	
THD + N Total harmonic distortion plus noise	$V_O = 0.5\text{ V to }2.5\text{ V},$ $f = 1\text{ kHz},$ $R_L = 10\text{ k}\Omega\ddagger$	$A_V = 1$	0.25%			
		$A_V = 10$	1.8%			
Gain-bandwidth product	$f = 10\text{ kHz},$ $C_L = 100\text{ pF}\ddagger$	$R_L = 10\text{ k}\Omega\ddagger,$ 25°C	46		kHz	
BOM Maximum output-swing bandwidth	$V_{O(PP)} = 1\text{ V},$ $R_L = 10\text{ k}\Omega\ddagger,$	$A_V = 1,$ $C_L = 100\text{ pF}\ddagger$ 25°C	8.3		kHz	
$t_s$ Settling time	$A_V = -1,$ Step = 0.5 V to 2.5 V, $R_L = 10\text{ k}\Omega\ddagger,$ $C_L = 100\text{ pF}\ddagger$	To 0.1%	8.6		$\mu\text{s}$	
		To 0.01%	16			
$\phi_m$ Phase margin at unity gain	$R_L = 10\text{ k}\Omega\ddagger,$	25°C	62°			
		Gain margin	25°C	11		dB

† Full range is  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  for Q level part,  $-55^\circ\text{C}$  to  $125^\circ\text{C}$  for M level part.

‡ Referenced to 1.5 V

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**electrical characteristics at specified free-air temperature,  $V_{DD} = 5\text{ V}$  (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$T_A$ †	TLV2422C			UNIT
			MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_{IC} = 0,$ $V_O = 0,$ $V_{DD} \pm = \pm 2.5\text{ V},$ $R_S = 50\ \Omega$	25°C		300	2000	$\mu\text{V}$
		Full range			2500	
$\alpha V_{IO}$ Temperature coefficient of input offset voltage		25°C to 70°C		2		$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C		0.003		$\mu\text{V}/\text{mo}$
$I_{IO}$ Input offset current		25°C		0.5	60	$\text{pA}$
		Full range			150	
$I_{IB}$ Input bias current		25°C		1	60	$\text{pA}$
		Full range			150	
$V_{ICR}$ Common-mode input voltage range	$ V_{IO}  \leq 5\text{ mV},$ $R_S = 50\ \Omega$	25°C	0 to 4.5	-0.25 to 4.75	$\text{V}$	
		Full range	0 to 4.2			
$V_{OH}$ High-level output voltage	$I_{OH} = -100\ \mu\text{A}$	25°C		4.97	$\text{V}$	
		25°C		4.5 to 4.75		
		Full range		4.25		
$V_{OL}$ Low-level output voltage	$V_{IC} = 2.5\text{ V},$ $I_{OL} = 100\ \mu\text{A}$	25°C		0.04	$\text{V}$	
		25°C		0.15		
		Full range		0.5		
$A_{VD}$ Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V},$ $V_O = 1\text{ V to }4\text{ V}$	25°C	$R_L = 10\ \text{k}\Omega^\ddagger$	8 to 12	$\text{V/mV}$	
			Full range	5		
		25°C	$R_L = 1\ \text{M}\Omega^\ddagger$	1000		
$r_{i(d)}$ Differential input resistance		25°C		$10^{12}$	$\Omega$	
$r_{i(c)}$ Common-mode input resistance		25°C		$10^{12}$	$\Omega$	
$C_{i(c)}$ Common-mode input capacitance	$f = 10\ \text{kHz}$	25°C		8	$\text{pF}$	
$Z_O$ Closed-loop output impedance	$f = 100\ \text{kHz},$ $A_V = 10$	25°C		130	$\Omega$	
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }4.5\text{ V},$ $V_O = 2.5\text{ V},$ $R_S = 50\ \Omega$	25°C		70 to 90	$\text{dB}$	
		Full range		70		
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{DD}/\Delta V_{IO}$ )	$V_{DD} = 4.4\text{ V to }8\text{ V},$ $V_{IC} = V_{DD}/2,$ No load	25°C		80 to 95	$\text{dB}$	
		Full range		80		
$I_{DD}$ Supply current	$V_O = 2.5\text{ V},$ No load	25°C		100 to 150	$\mu\text{A}$	
		Full range		175		

† Full range is 0°C to 70°C.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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electrical characteristics at specified free-air temperature,  $V_{DD} = 5\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A$ †	TLV2422I			TLV2422AI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$ Input offset voltage		25°C	300	2000		300	950	$\mu\text{V}$	
		Full range		2500		1500			
$\alpha_{VIO}$ Temperature coefficient of input offset voltage		25°C to 70°C	2			2		$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 4)	$V_{IC} = 0,$ $V_O = 0,$	$V_{DD} \pm \pm 2.5\text{ V},$ $R_S = 50\ \Omega$	25°C	0.003		0.003		$\mu\text{V}/\text{mo}$	
$I_{IO}$ Input offset current		25°C	0.5	60		0.5	60	$\text{pA}$	
		Full range		150		150			
$I_{IB}$ Input bias current		25°C	1	60		1	60	$\text{pA}$	
		Full range		150		150			
$V_{ICR}$ Common-mode input voltage range	$ V_{IO}  \leq 5\text{ mV},$ $R_S = 50\ \Omega$	25°C	0 to 4.5	-0.25 to 4.75		0 to 4.5	-0.25 to 4.75	$\text{V}$	
		Full range	0 to 4.2			0 to 4.2			
$V_{OH}$ High-level output voltage	$I_{OH} = -100\ \mu\text{A}$ $I_{OH} = -1\text{ mA}$	25°C	4.97			4.97		$\text{V}$	
		25°C	4.5	4.75		4.5	4.75		
		Full range	4.25			4.25			
$V_{OL}$ Low-level output voltage	$V_{IC} = 2.5\text{ V},$ $I_{OL} = 100\ \mu\text{A}$ $V_{IC} = 2.5\text{ V},$ $I_{OL} = 500\ \mu\text{A}$	25°C	0.04			0.04		$\text{V}$	
		25°C	0.15			0.15			
		Full range		0.5			0.5		
$A_{VD}$ Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V},$ $V_O = 1\text{ V to }4\text{ V}$	$R_L = 10\text{ k}\Omega^\ddagger$	25°C	8	12		8	12	$\text{V}/\text{mV}$
			Full range	5			5		
		$R_L = 1\text{ M}\Omega^\ddagger$	25°C	1000			1000		
$r_{i(d)}$ Differential input resistance		25°C	$10^{12}$			$10^{12}$		$\Omega$	
$r_{i(c)}$ Common-mode input resistance		25°C	$10^{12}$			$10^{12}$		$\Omega$	
$c_{i(c)}$ Common-mode input capacitance	$f = 10\text{ kHz}$	25°C	8			8		$\text{pF}$	
$z_o$ Closed-loop output impedance	$f = 100\text{ kHz},$ $A_V = 10$	25°C	130			130		$\Omega$	
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }4.5\text{ V},$ $V_O = 2.5\text{ V},$ $R_S = 50\ \Omega$	25°C	70	90		70	90	$\text{dB}$	
		Full range	70			70			
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{DD}/\Delta V_{IO}$ )	$V_{DD} = 4.4\text{ V to }8\text{ V},$ $V_{IC} = V_{DD}/2,$ No load	25°C	80	95		80	95	$\text{dB}$	
		Full range	80			80			
$I_{DD}$ Supply current	$V_O = 2.5\text{ V},$ No load	25°C	100	150		100	150	$\mu\text{A}$	
		Full range		175			175		

† Full range is  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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operating characteristics at specified free-air temperature,  $V_{DD} = 5\text{ V}$

PARAMETER	TEST CONDITIONS	$T_A$ †	TLV2422C, TLV2422I TLV2422AI			UNIT
			MIN	TYP	MAX	
SR Slew rate at unity gain	$V_O = 1.5\text{ V to }3.5\text{ V},$ $C_L = 100\text{ pF}‡$	25°C	0.01	0.02		V/μs
		Full range	0.008			
$V_n$ Equivalent input noise voltage	$f = 10\text{ Hz}$	25°C	100		nV/√Hz	
	$f = 1\text{ kHz}$	25°C	18			
$V_{N(PP)}$ Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$	25°C	1.9		μV	
	$f = 0.1\text{ Hz to }10\text{ Hz}$	25°C	2.8			
$I_n$ Equivalent input noise current		25°C	0.6		fA/√Hz	
THD + N Total harmonic distortion plus noise	$V_O = 1.5\text{ V to }3.5\text{ V},$ $f = 1\text{ kHz},$ $R_L = 10\text{ k}\Omega‡$	$A_V = 1$	0.24%			
		$A_V = 10$	1.7%			
Gain-bandwidth product	$f = 10\text{ kHz},$ $C_L = 100\text{ pF}‡$	$R_L = 10\text{ k}\Omega‡,$ 25°C	52		kHz	
$B_{OM}$ Maximum output-swing bandwidth	$V_{O(PP)} = 2\text{ V},$ $R_L = 10\text{ k}\Omega‡,$	$A_V = 1,$ $C_L = 100\text{ pF}‡$ 25°C	5.3		kHz	
$t_s$ Settling time	$A_V = -1,$ Step = 1.5 V to 3.5 V, $R_L = 10\text{ k}\Omega‡,$ $C_L = 100\text{ pF}‡$	To 0.1%	8.5		μs	
		To 0.01%	15.5			
$\phi_m$ Phase margin at unity gain	$R_L = 10\text{ k}\Omega‡,$ $C_L = 100\text{ pF}‡$	25°C	66°		dB	
Gain margin		25°C	11			

† Full range for the C version is 0°C to 70°C. Full range for the I version is -40°C to 85°C.

‡ Referenced to 2.5 V



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PARAMETER	TEST CONDITIONS	$T_A$ †	TLV2422Q, TLV2422M			TLV2422AQ, TLV2422AM			UNIT	
			MIN	TYP	MAX	MIN	TYP	MAX		
$V_{IO}$ Input offset voltage		25°C	300	2000		300	950	$\mu\text{V}$		
		Full range		2500		1800				
$\alpha_{V_{IO}}$ Temperature coefficient of input offset voltage		Full range	2			2			$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 4)	$V_{IC} = 0,$ $V_O = 0,$	$V_{DD} \pm \pm 2.5\text{ V},$ $R_S = 50\ \Omega$	25°C	0.003			0.003			$\mu\text{V}/\text{mo}$
$I_{IO}$ Input offset current		25°C	0.5	60		0.5	60	$\text{pA}$		
		Full range		150		150				
$I_{IB}$ Input bias current		25°C	1	60		1	60	$\text{pA}$		
		Full range		300		300				
$V_{ICR}$ Common-mode input voltage range	$ V_{IO}  \leq 5\text{ mV},$ $R_S = 50\ \Omega$	25°C	0 to 4.5	-0.25 to 4.75		0 to 4.5	-0.25 to 4.75	V		
		Full range	0 to 4.2			0 to 4.2				
$V_{OH}$ High-level output voltage	$I_{OH} = -100\ \mu\text{A}$ $I_{OH} = -1\text{ mA}$	25°C	4.97			4.97			V	
		25°C	4.75			4.75				
		Full range	4.5			4.5				
$V_{OL}$ Low-level output voltage	$V_{IC} = 2.5\text{ V},$ $I_{OL} = 100\ \mu\text{A}$ $V_{IC} = 2.5\text{ V},$ $I_{OL} = 500\ \mu\text{A}$	25°C	0.04			0.04			V	
		25°C	0.15			0.15				
		Full range	0.5			0.5				
$A_{VD}$ Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V},$ $V_O = 1\text{ V to }4\text{ V}$	$R_L = 10\text{ k}\Omega^\ddagger$	25°C	8	12		8	12	V/mV	
			Full range	3			3			
		$R_L = 1\text{ M}\Omega^\ddagger$	25°C	1000			1000			
$r_{i(d)}$ Differential input resistance		25°C	$10^{12}$			$10^{12}$			$\Omega$	
$r_{i(c)}$ Common-mode input resistance		25°C	$10^{12}$			$10^{12}$			$\Omega$	
$c_{i(c)}$ Common-mode input capacitance	$f = 10\text{ kHz}$	25°C	8			8			$\text{pF}$	
$z_o$ Closed-loop output impedance	$f = 100\text{ kHz},$ $A_V = 10$	25°C	130			130			$\Omega$	
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR}\text{ min},$ $V_O = 2.5\text{ V},$ $R_S = 50\ \Omega$	25°C	70	90		70	90	dB		
		Full range	70			70				
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{DD}/\Delta V_{IO}$ )	$V_{DD} = 4.4\text{ V to }8\text{ V},$ $V_{IC} = V_{DD}/2,$ No load	25°C	80	95		80	95	dB		
		Full range	80			80				
$I_{DD}$ Supply current	$V_O = 2.5\text{ V},$ No load	25°C	100	150		100	150	$\mu\text{A}$		
		Full range	175			175				

† Full range is  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  for Q level part,  $-55^\circ\text{C}$  to  $125^\circ\text{C}$  for M level part.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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operating characteristics at specified free-air temperature,  $V_{DD} = 5\text{ V}$

PARAMETER	TEST CONDITIONS	$T_A$ †	TLV2422Q, TLV2422M, TLV2422AQ, TLV2422AM			UNIT
			MIN	TYP	MAX	
SR Slew rate at unity gain	$V_O = 1.5\text{ V to }3.5\text{ V},$ $R_L = 10\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡	25°C	0.01	0.02		V/ $\mu$ s
		Full range	0.008			
$V_n$ Equivalent input noise voltage	$f = 10\text{ Hz}$	25°C	100		nV/ $\sqrt{\text{Hz}}$	
	$f = 1\text{ kHz}$	25°C	18			
$V_{N(PP)}$ Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$	25°C	1.9		$\mu$ V	
	$f = 0.1\text{ Hz to }10\text{ Hz}$	25°C	2.8			
$I_n$ Equivalent input noise current		25°C	0.6		fA/ $\sqrt{\text{Hz}}$	
THD + N Total harmonic distortion plus noise	$V_O = 1.5\text{ V to }3.5\text{ V},$ $f = 1\text{ kHz},$ $R_L = 10\text{ k}\Omega$ ‡	$A_V = 1$	0.24%			
		$A_V = 10$	1.7%			
Gain-bandwidth product	$f = 10\text{ kHz},$ $C_L = 100\text{ pF}$ ‡	$R_L = 10\text{ k}\Omega$ ‡, 25°C	52		kHz	
BOM Maximum output-swing bandwidth	$V_{O(PP)} = 2\text{ V},$ $R_L = 10\text{ k}\Omega$ ‡,	$A_V = 1,$ $C_L = 100\text{ pF}$ ‡	25°C	5.3		kHz
$t_s$ Settling time	$A_V = -1,$ Step = 1.5 V to 3.5 V, $R_L = 10\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡	To 0.1%	25°C	8.5		$\mu$ s
		To 0.01%		15.5		
$\phi_m$ Phase margin at unity gain	$R_L = 10\text{ k}\Omega$ ‡,	$C_L = 100\text{ pF}$ ‡	25°C	66°		
Gain margin			25°C	11		

† Full range is  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  for Q level part,  $-55^\circ\text{C}$  to  $125^\circ\text{C}$  for M level part.

‡ Referenced to 2.5 V



## TYPICAL CHARACTERISTICS

### Table of Graphs

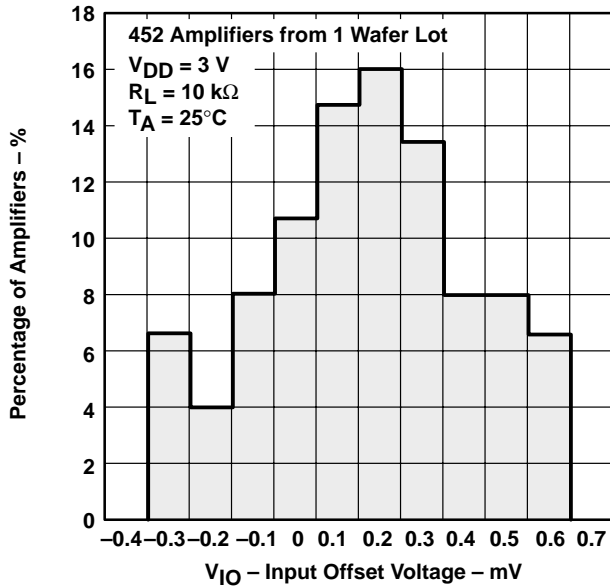
			FIGURE
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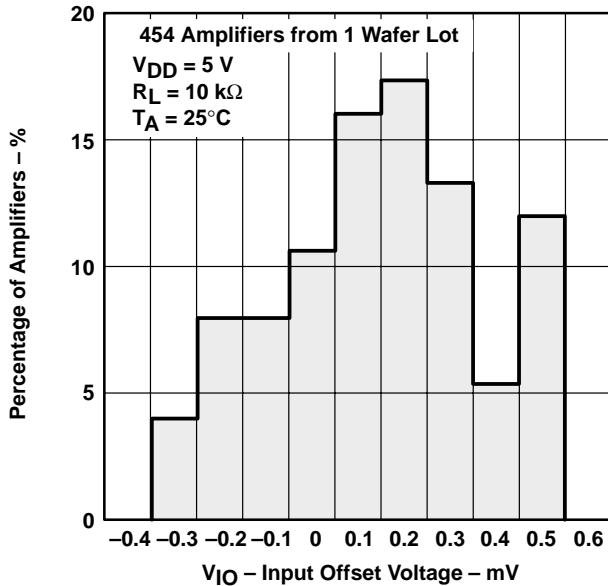
**TYPICAL CHARACTERISTICS**

**DISTRIBUTION OF TLV2422  
 INPUT OFFSET VOLTAGE**



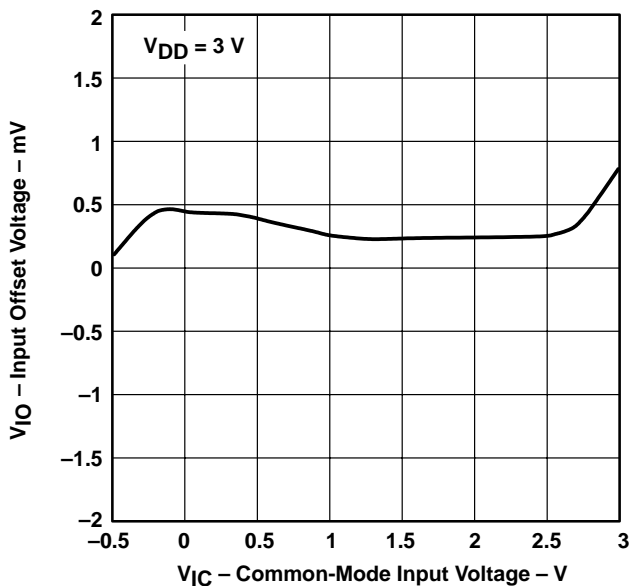
**Figure 2**

**DISTRIBUTION OF TLV2422  
 INPUT OFFSET VOLTAGE**



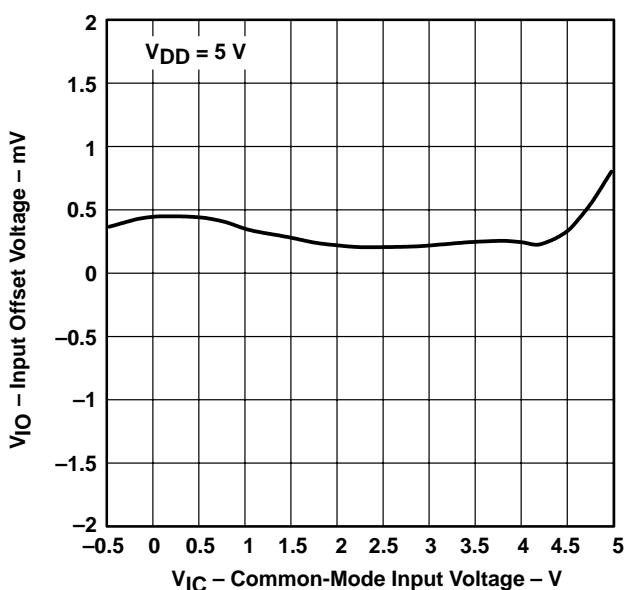
**Figure 3**

**INPUT OFFSET VOLTAGE  
 vs  
 COMMON-MODE INPUT VOLTAGE**



**Figure 4**

**INPUT OFFSET VOLTAGE  
 vs  
 COMMON-MODE INPUT VOLTAGE**

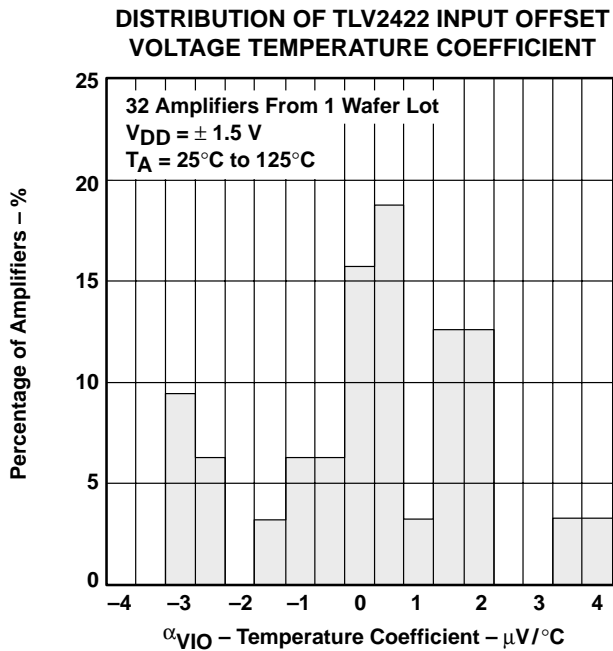


**Figure 5**

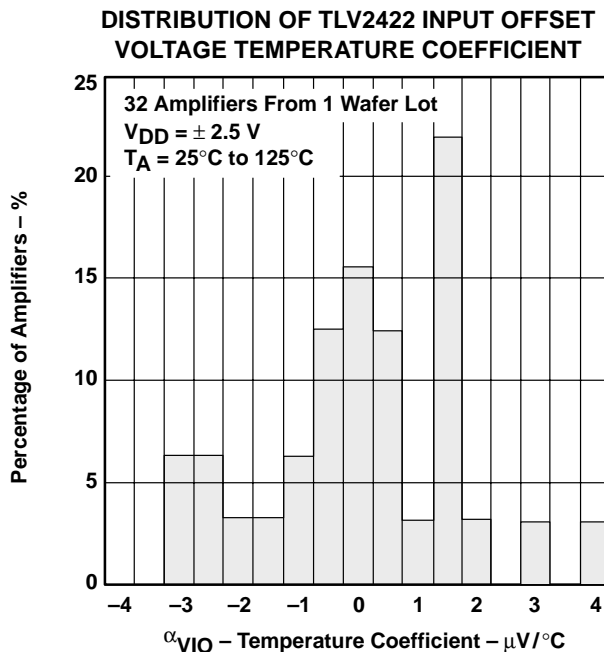




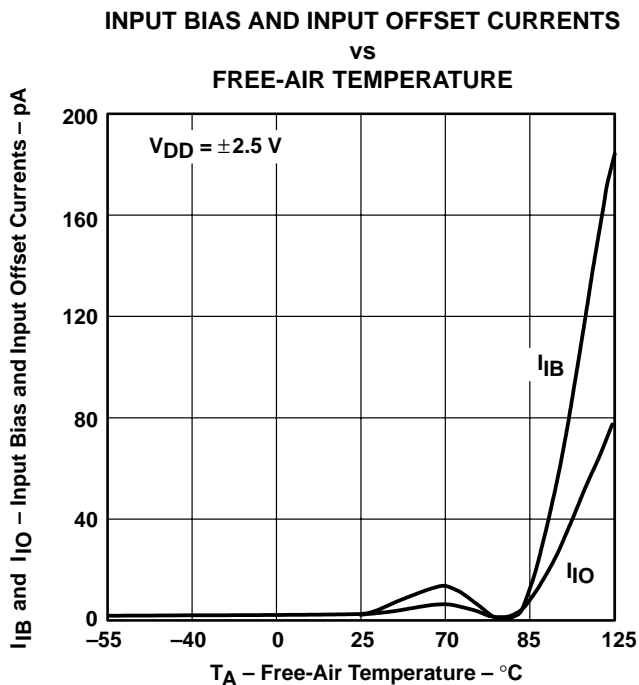
**TYPICAL CHARACTERISTICS**



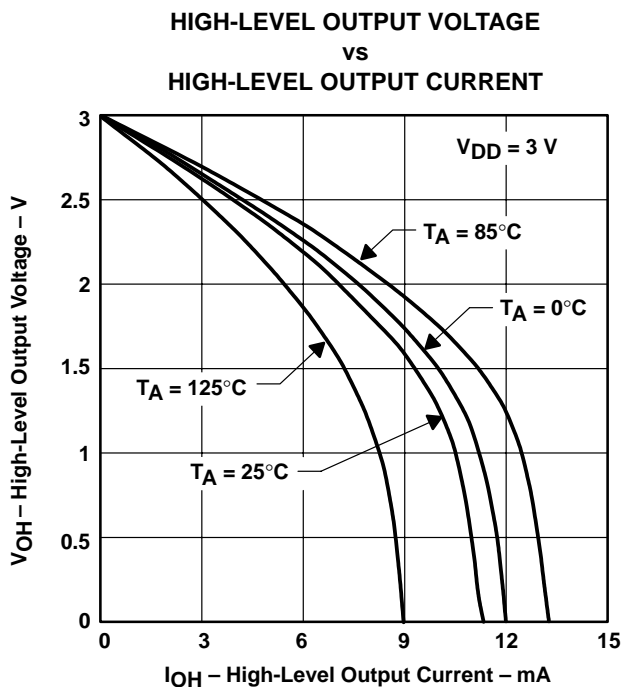
**Figure 6**



**Figure 7**

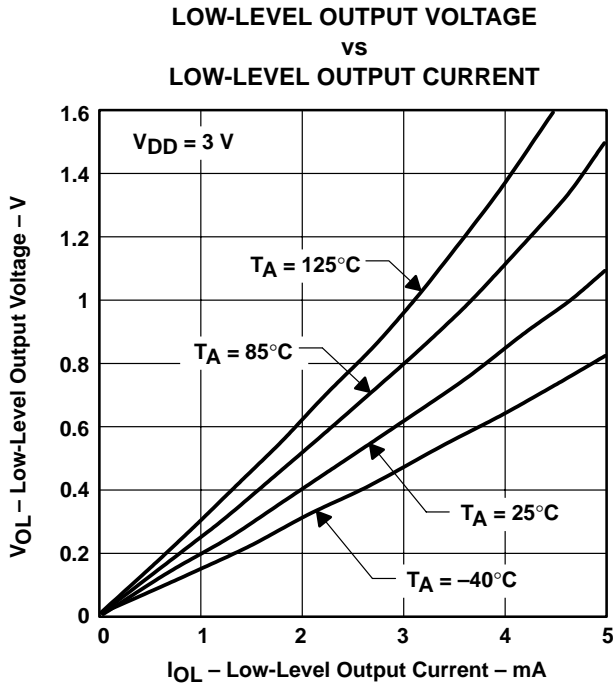


**Figure 8**

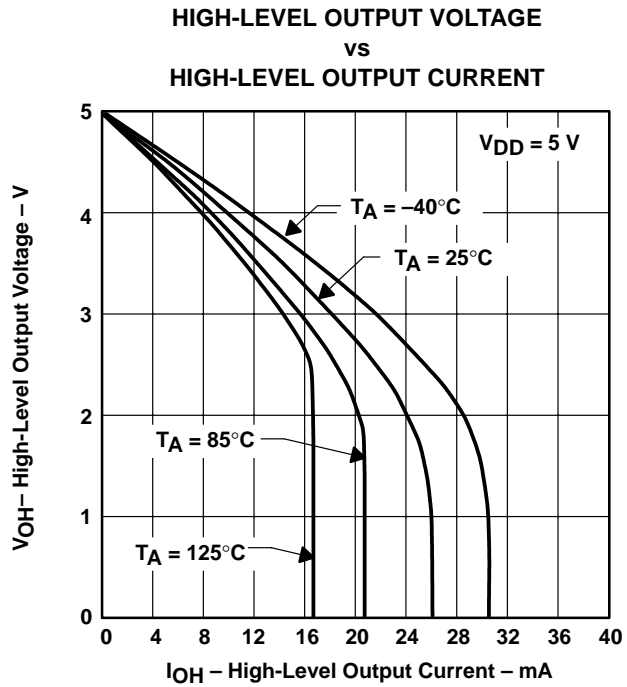


**Figure 9**

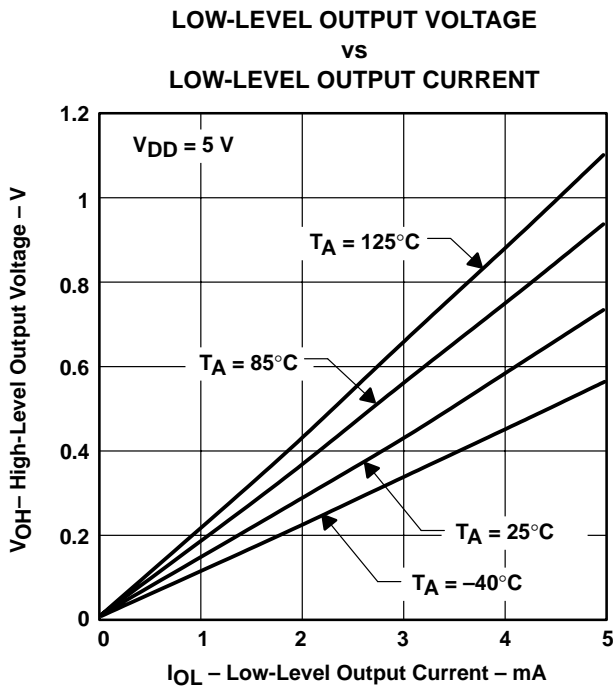
**TYPICAL CHARACTERISTICS**



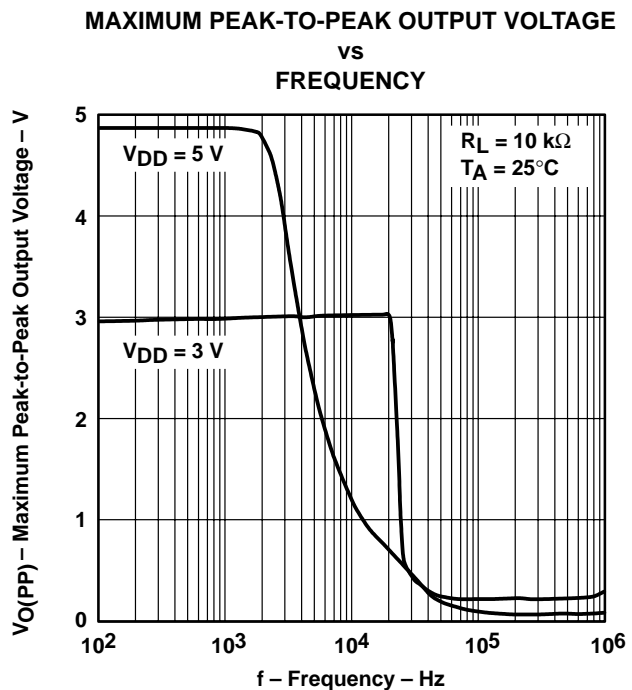
**Figure 10**



**Figure 11**



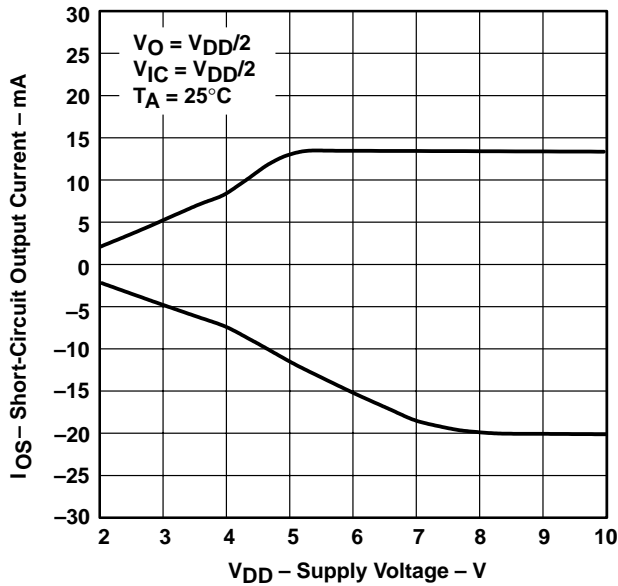
**Figure 12**



**Figure 13**

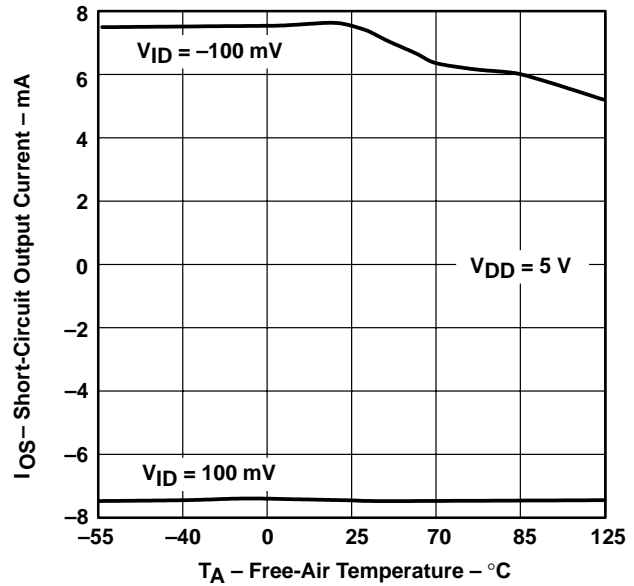
**TYPICAL CHARACTERISTICS**

**SHORT-CIRCUIT OUTPUT CURRENT  
vs  
SUPPLY VOLTAGE**



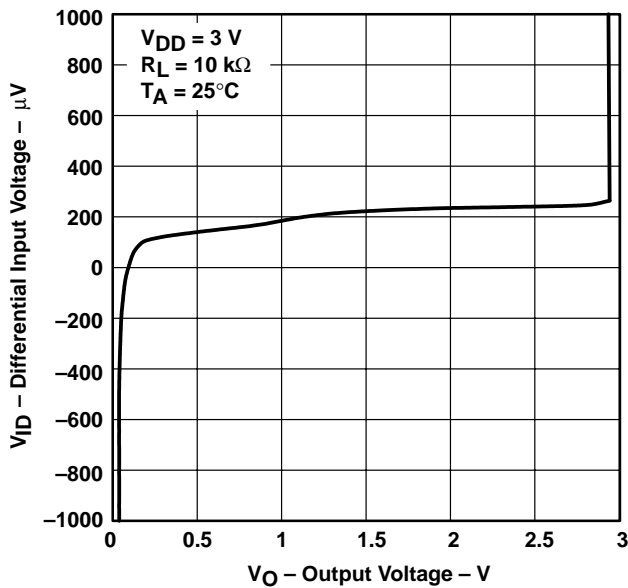
**Figure 14**

**SHORT-CIRCUIT OUTPUT CURRENT  
vs  
FREE-AIR TEMPERATURE**



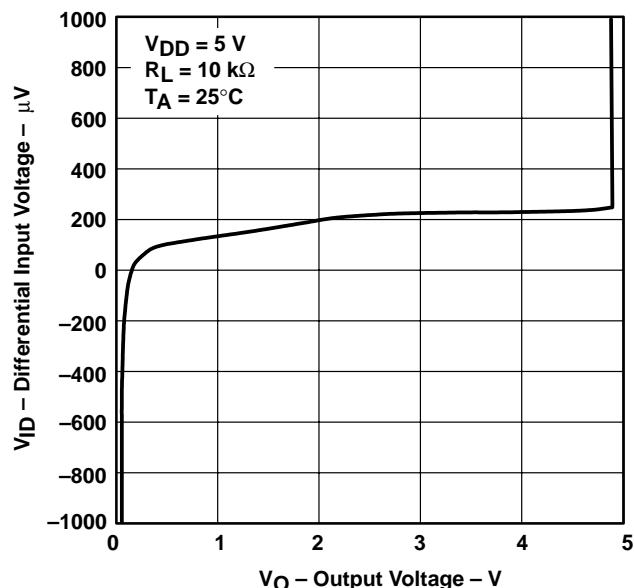
**Figure 15**

**DIFFERENTIAL INPUT VOLTAGE  
vs  
OUTPUT VOLTAGE**



**Figure 16**

**DIFFERENTIAL INPUT VOLTAGE  
vs  
OUTPUT VOLTAGE**



**Figure 17**

TYPICAL CHARACTERISTICS

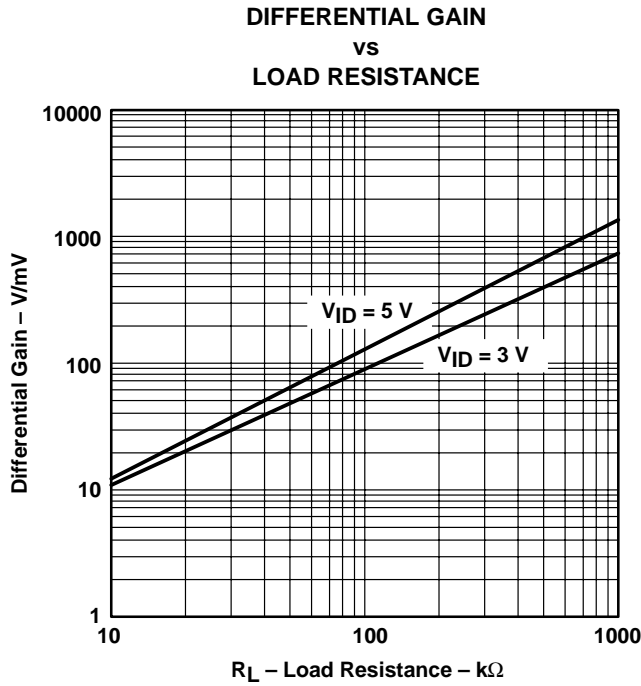


Figure 18

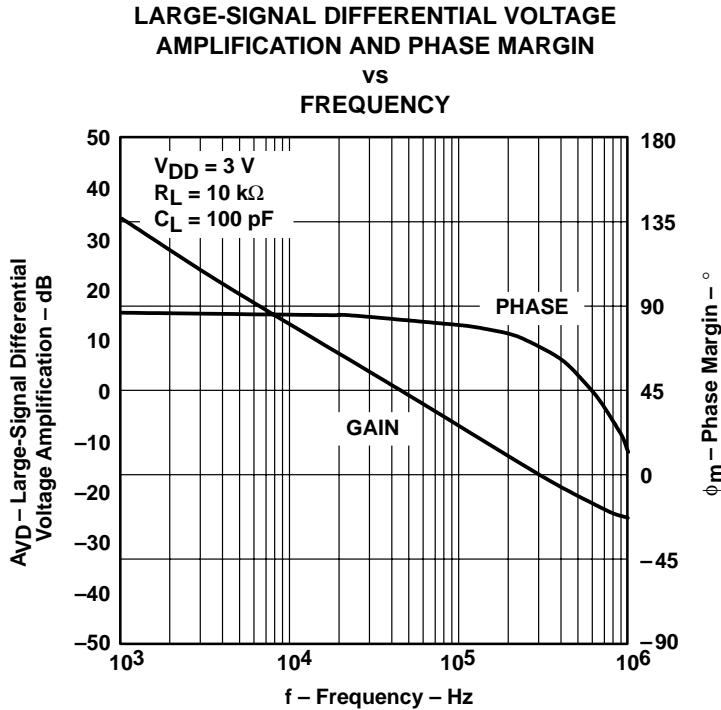
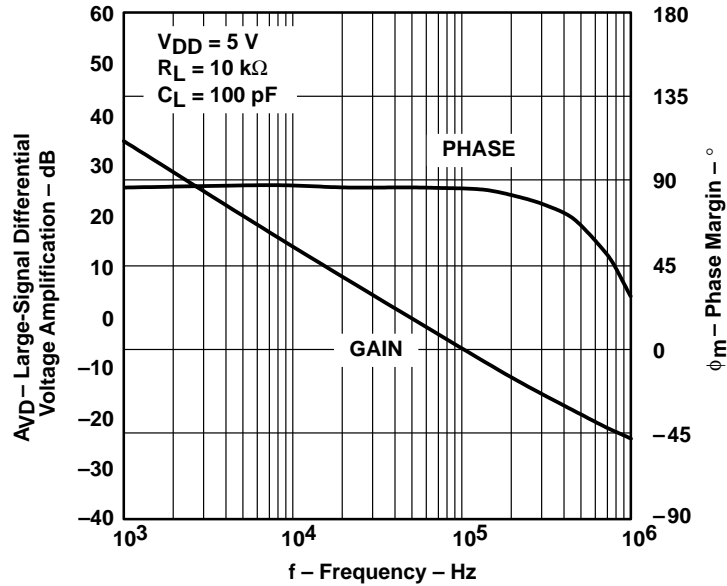


Figure 19

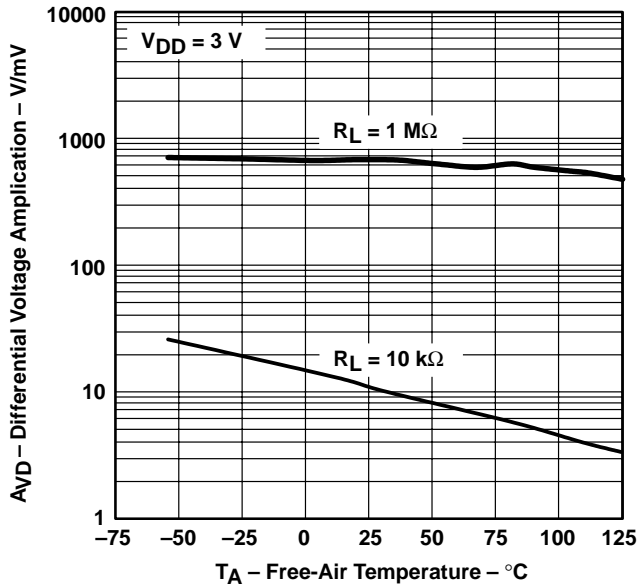
**TYPICAL CHARACTERISTICS**

**LARGE-SIGNAL DIFFERENTIAL VOLTAGE  
AMPLIFICATION AND PHASE MARGIN**

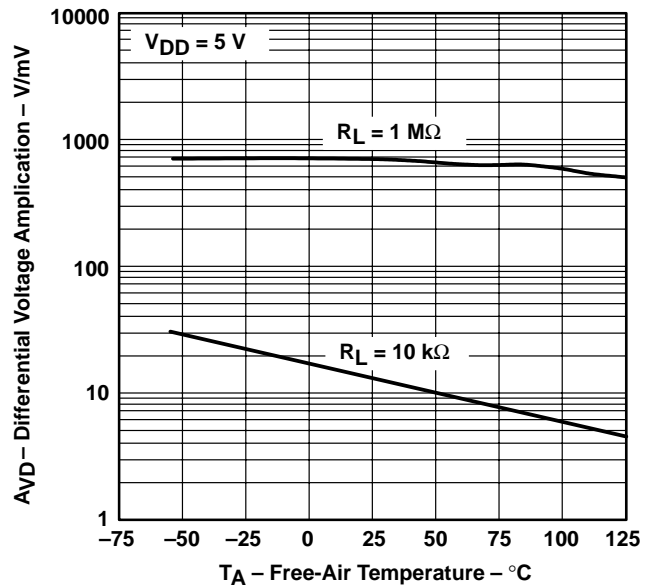
vs  
**FREQUENCY**



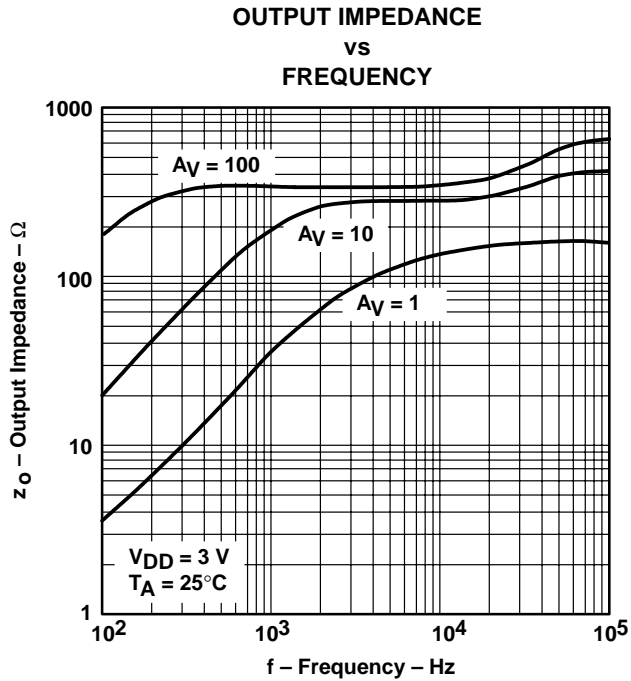
**DIFFERENTIAL VOLTAGE AMPLIFICATION  
vs  
FREE-AIR TEMPERATURE**



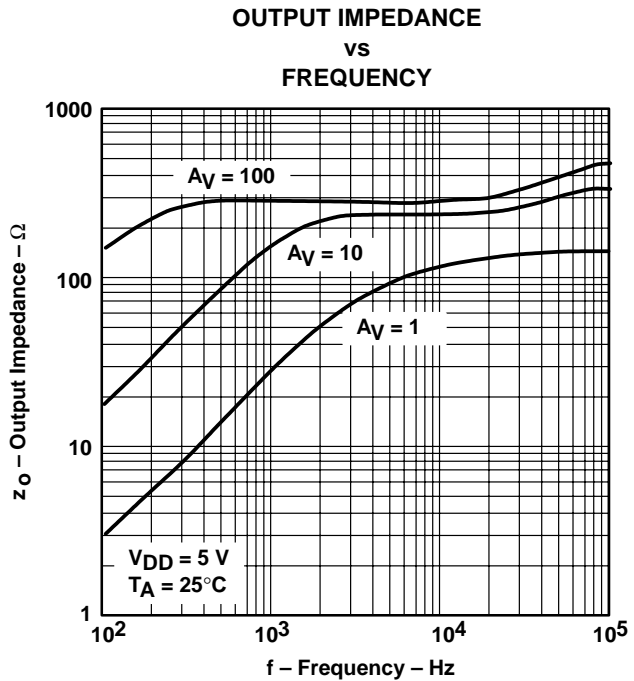
**DIFFERENTIAL VOLTAGE AMPLIFICATION  
vs  
FREE-AIR TEMPERATURE**



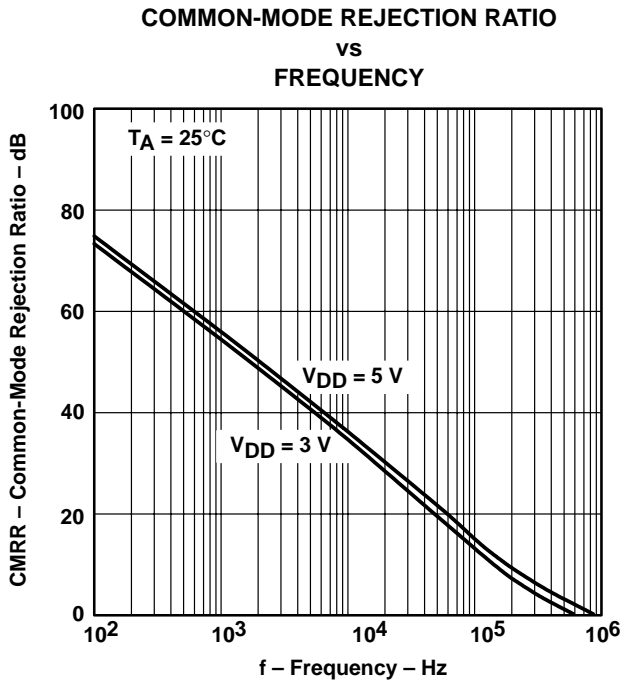
**TYPICAL CHARACTERISTICS**



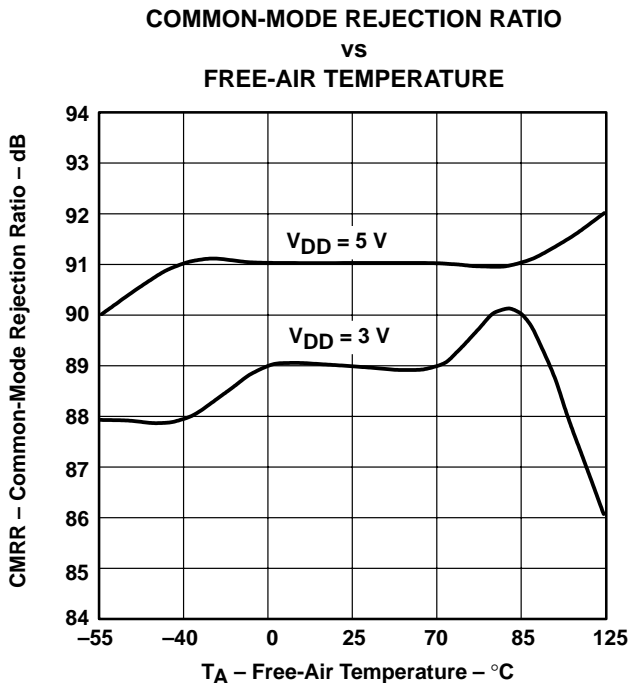
**Figure 23**



**Figure 24**



**Figure 25**



**Figure 26**

TYPICAL CHARACTERISTICS

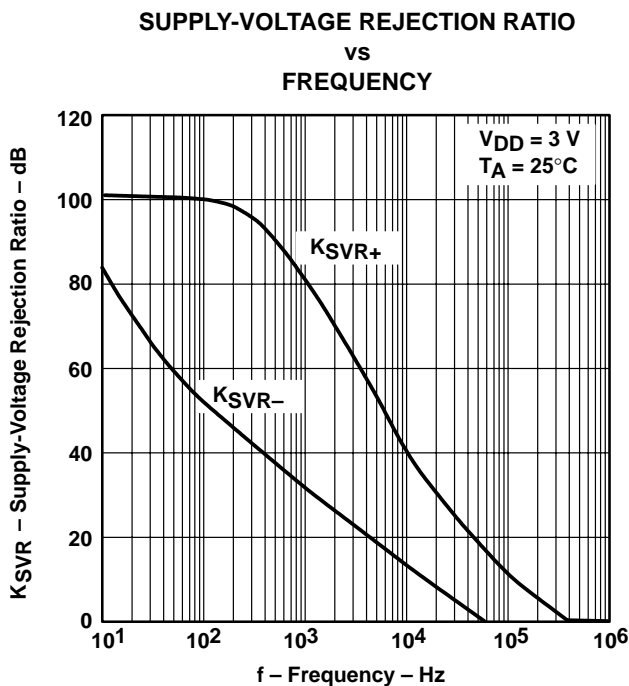


Figure 27

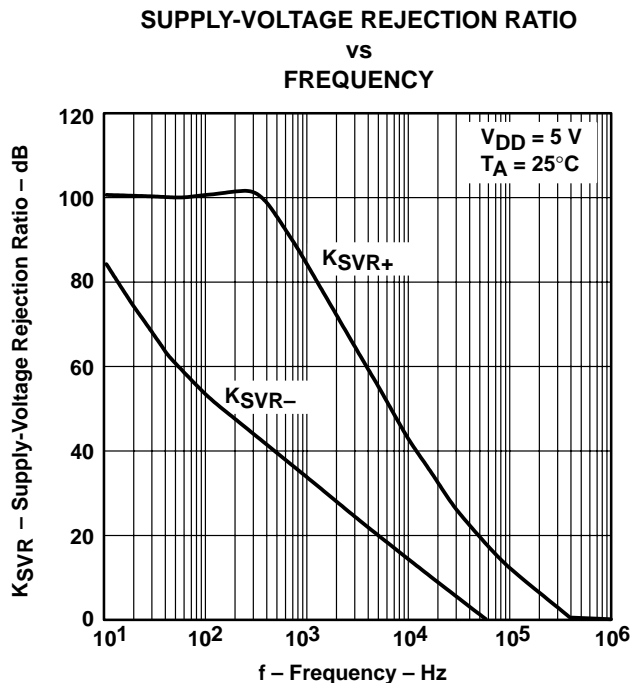


Figure 28

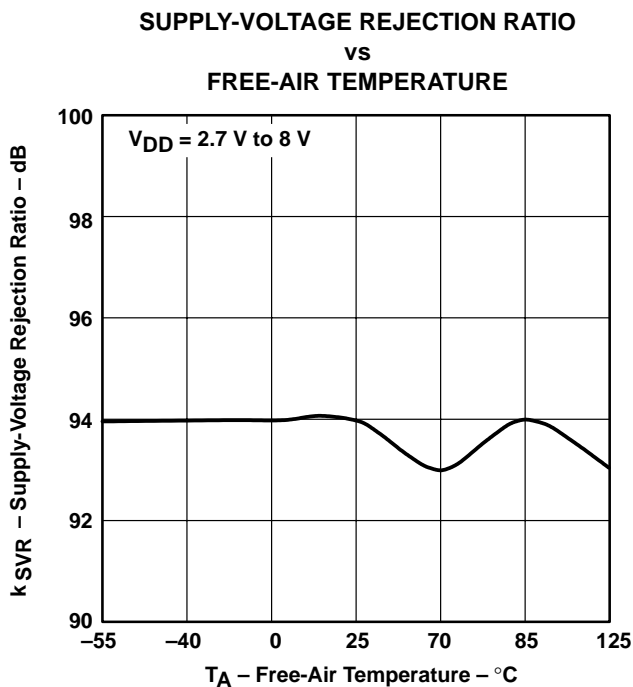


Figure 29

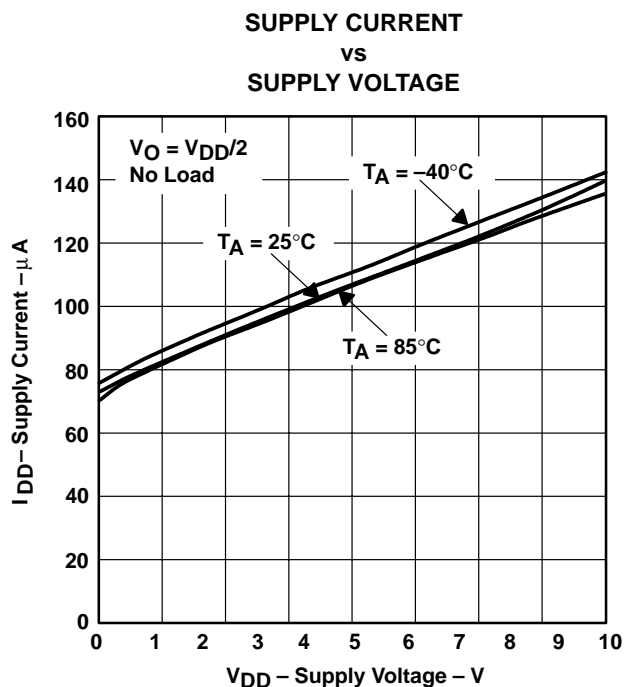
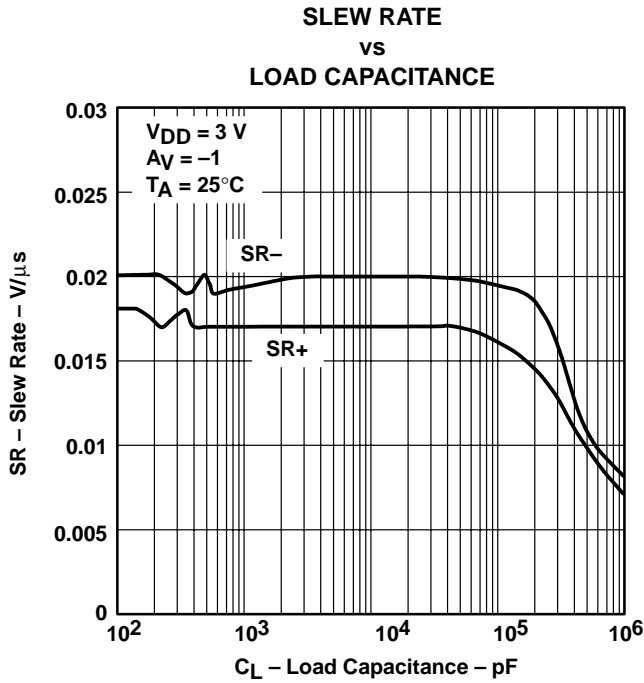
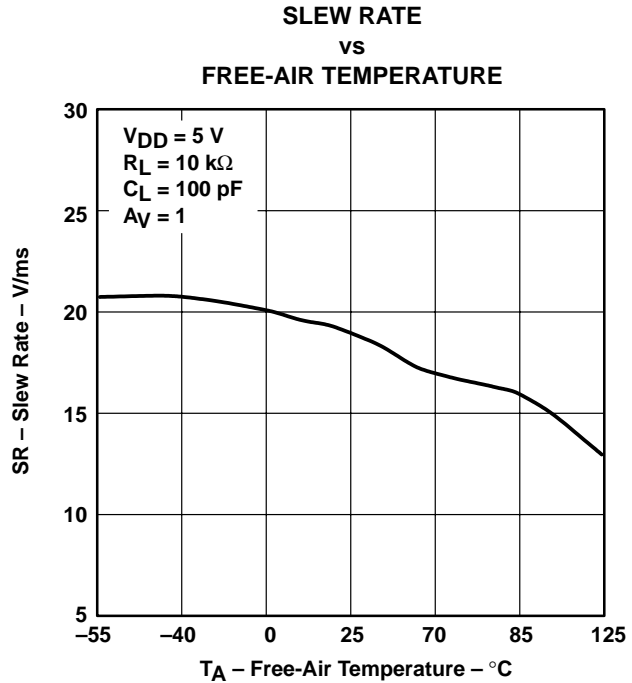


Figure 30

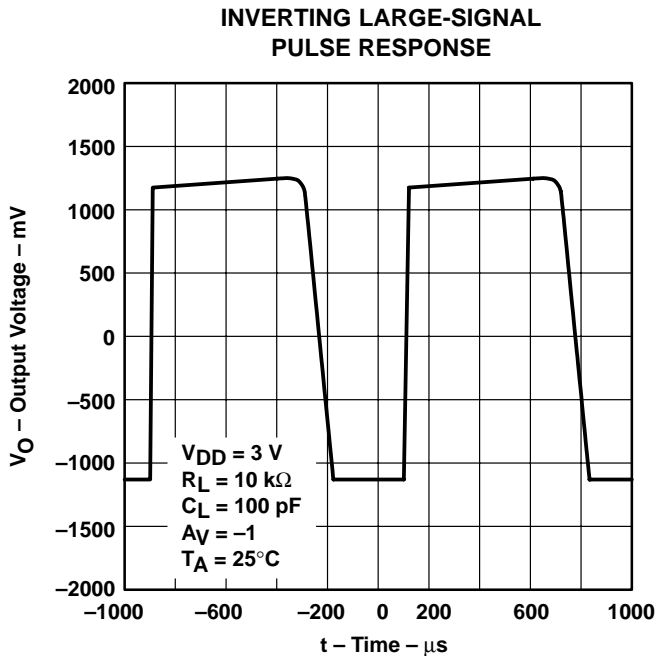
**TYPICAL CHARACTERISTICS**



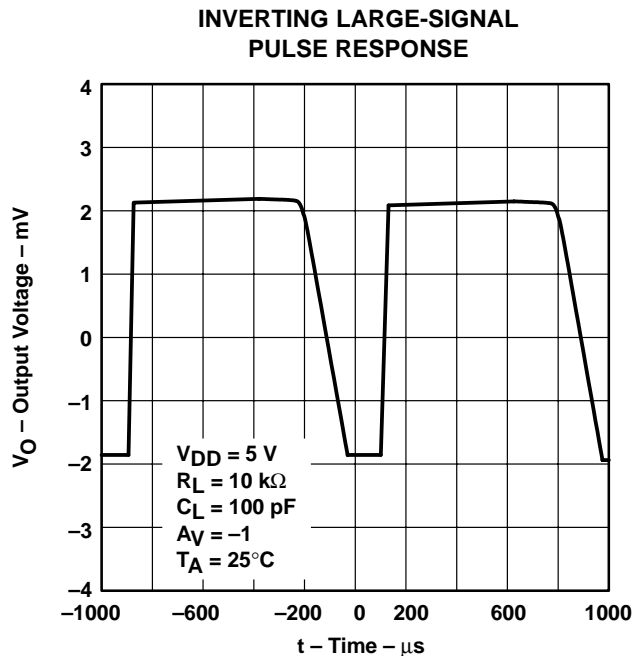
**Figure 31**



**Figure 32**



**Figure 33**



**Figure 34**



TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER LARGE-SIGNAL  
PULSE RESPONSE

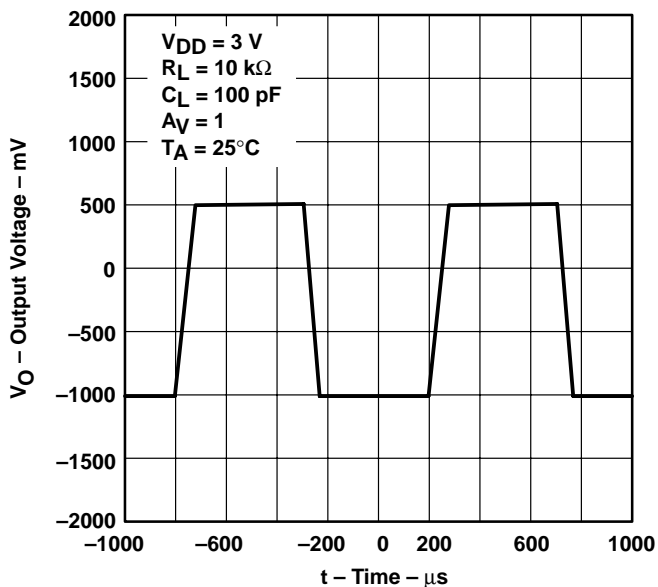


Figure 35

VOLTAGE-FOLLOWER LARGE-SIGNAL  
PULSE RESPONSE

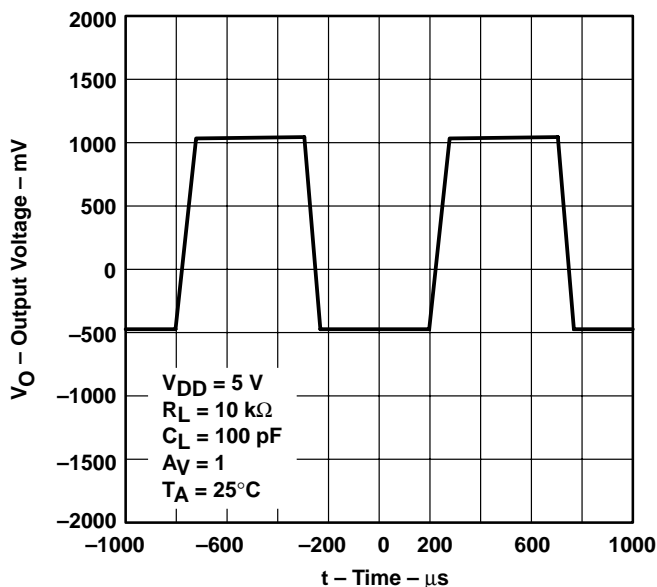


Figure 36

INVERTING SMALL-SIGNAL  
PULSE RESPONSE

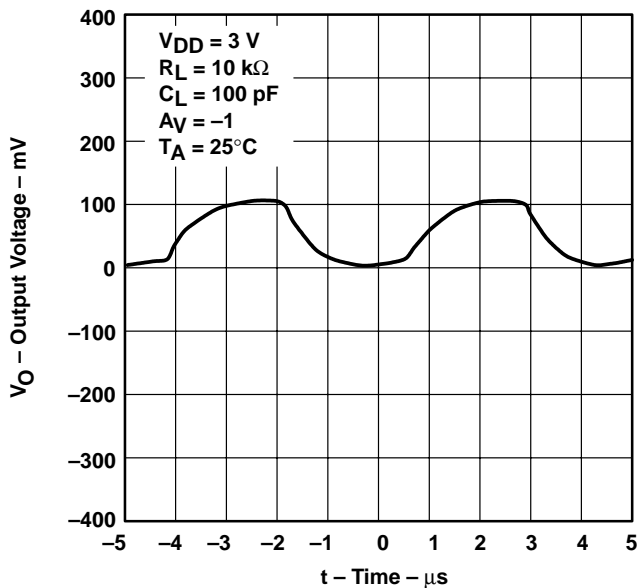


Figure 37

INVERTING SMALL-SIGNAL  
PULSE RESPONSE

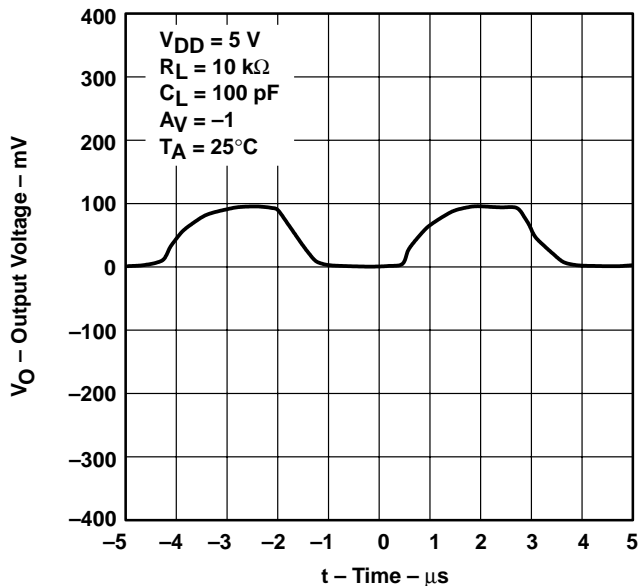


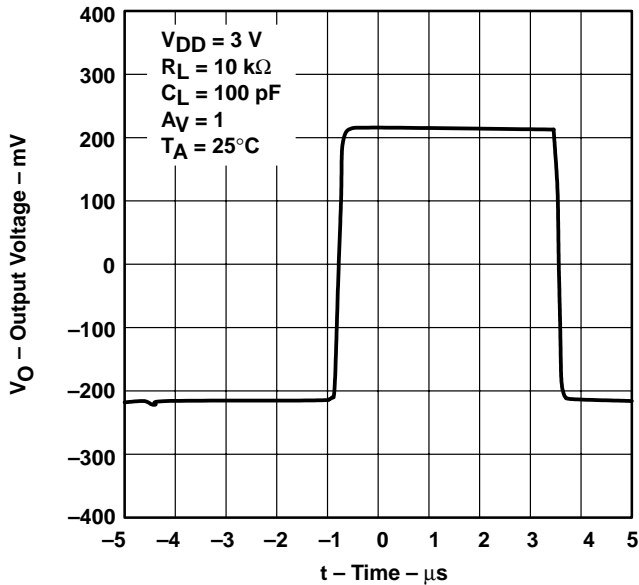
Figure 38

**TLV2422, TLV2422A**  
**Advanced LinCMOS™ RAIL-TO-RAIL OUTPUT**  
**WIDE-INPUT-VOLTAGE MICROPOWER DUAL OPERATIONAL AMPLIFIERS**

SLOS199C – SEPTEMBER 1997 – REVISED APRIL 2001

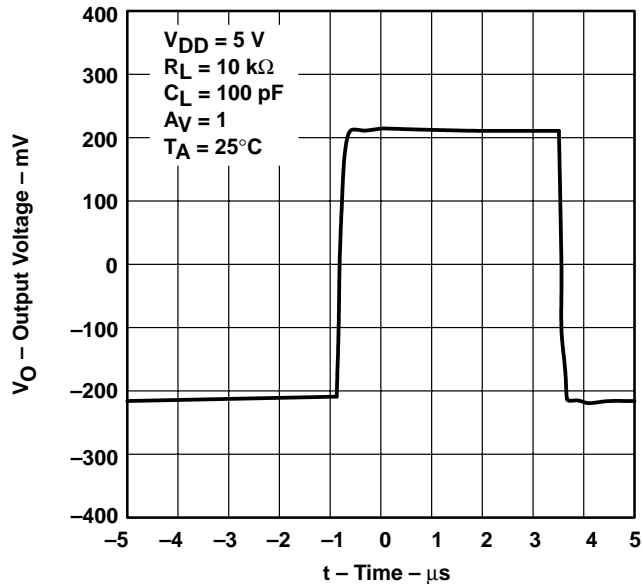
**TYPICAL CHARACTERISTICS**

**VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE**



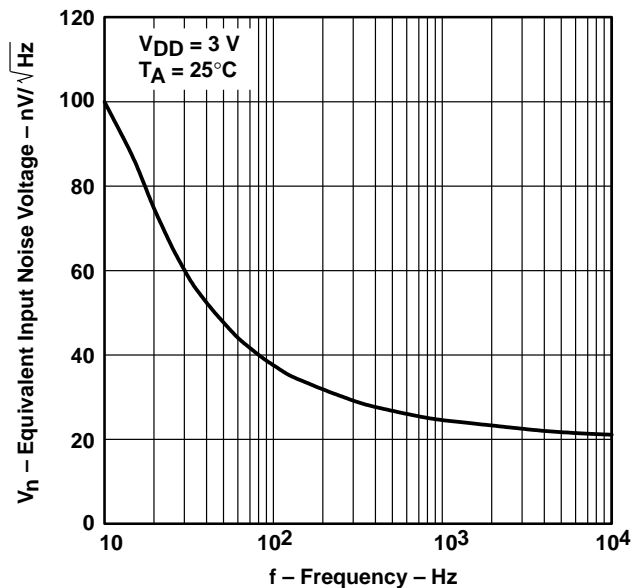
**Figure 39**

**VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE**



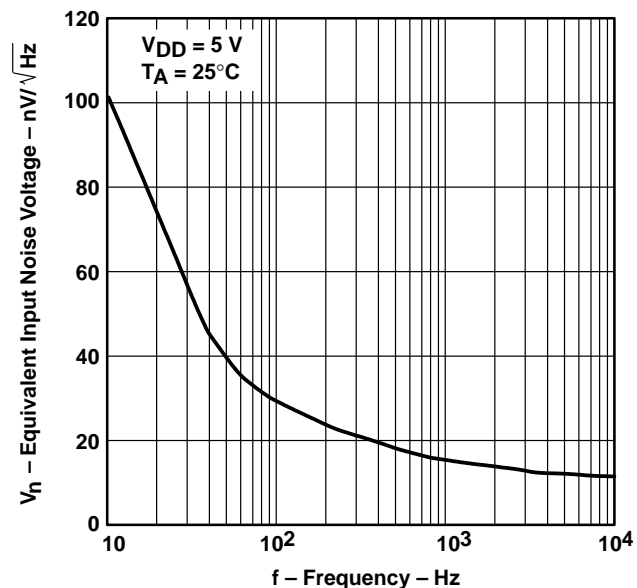
**Figure 40**

**EQUIVALENT INPUT NOISE VOLTAGE VS FREQUENCY**



**Figure 41**

**EQUIVALENT INPUT NOISE VOLTAGE VS FREQUENCY**

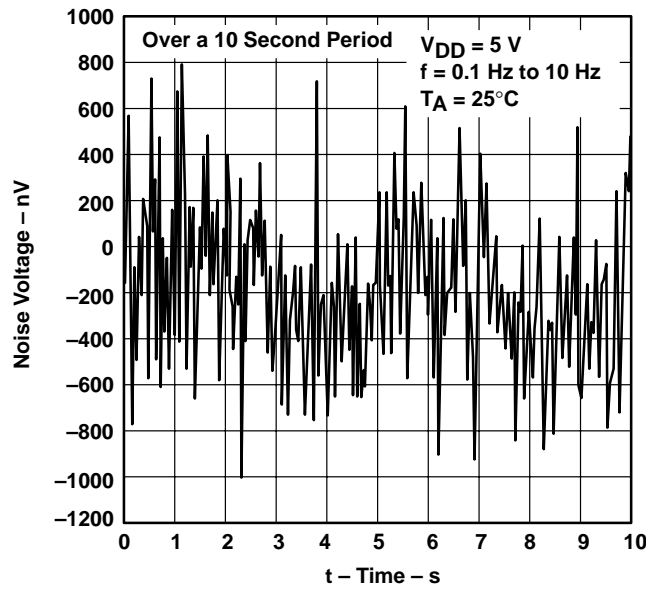


**Figure 42**



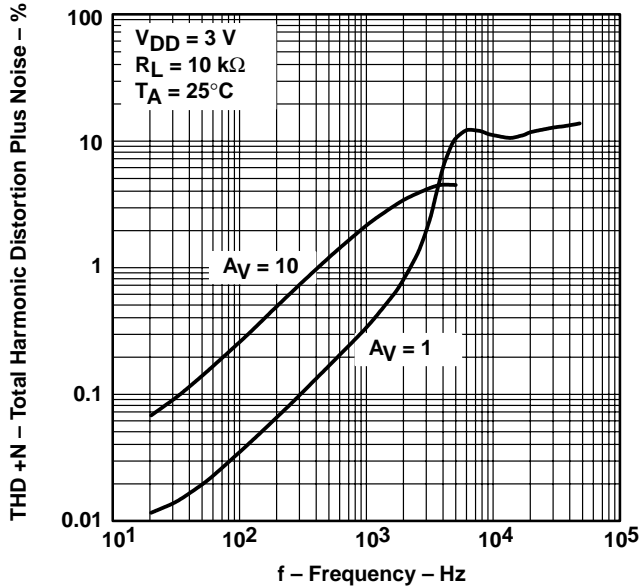
**TYPICAL CHARACTERISTICS**

**NOISE VOLTAGE OVER A 10-SECOND PERIOD**



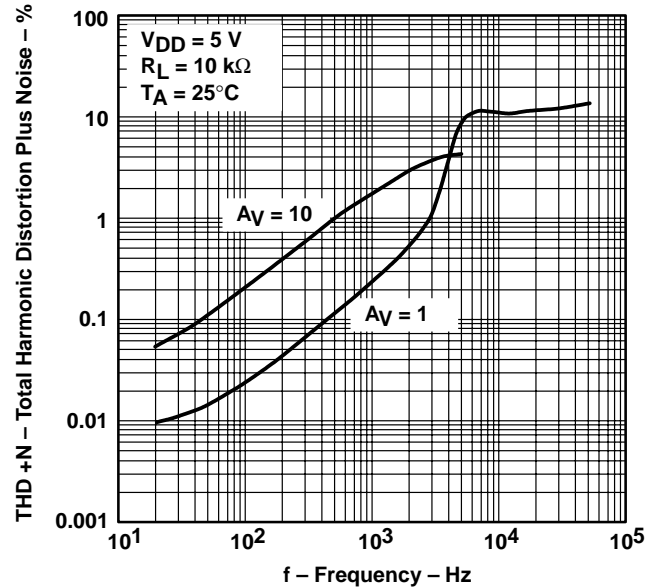
**Figure 43**

**TOTAL HARMONIC DISTORTION PLUS NOISE  
vs  
FREQUENCY**



**Figure 44**

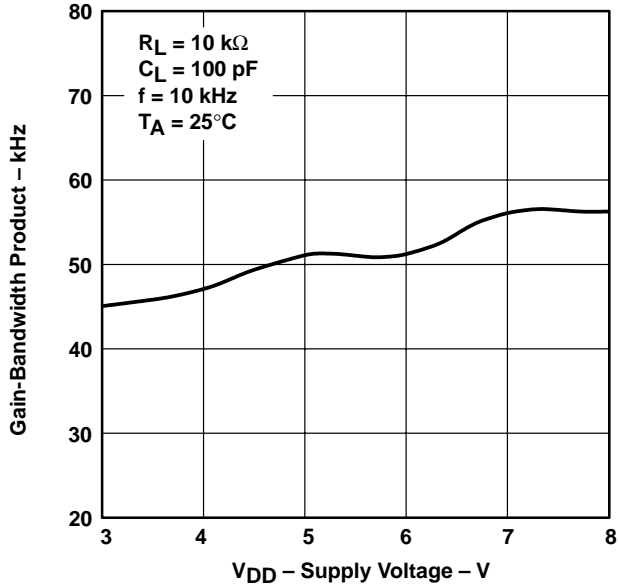
**TOTAL HARMONIC DISTORTION PLUS NOISE  
vs  
FREQUENCY**



**Figure 45**

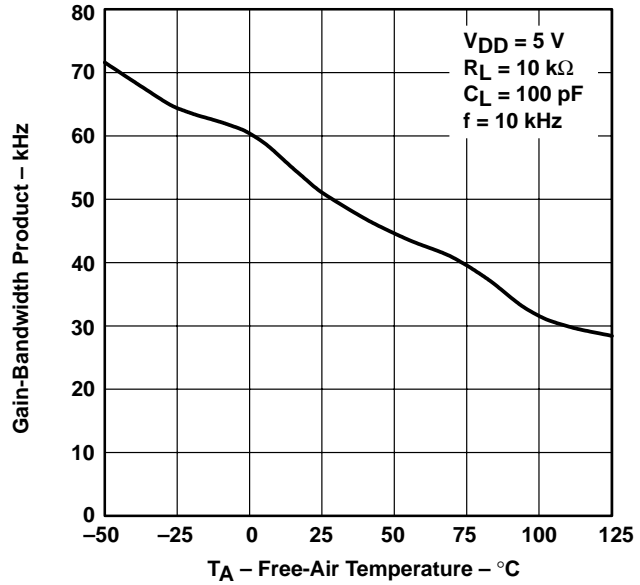
**TYPICAL CHARACTERISTICS**

**GAIN-BANDWIDTH PRODUCT**  
**vs**  
**SUPPLY VOLTAGE**



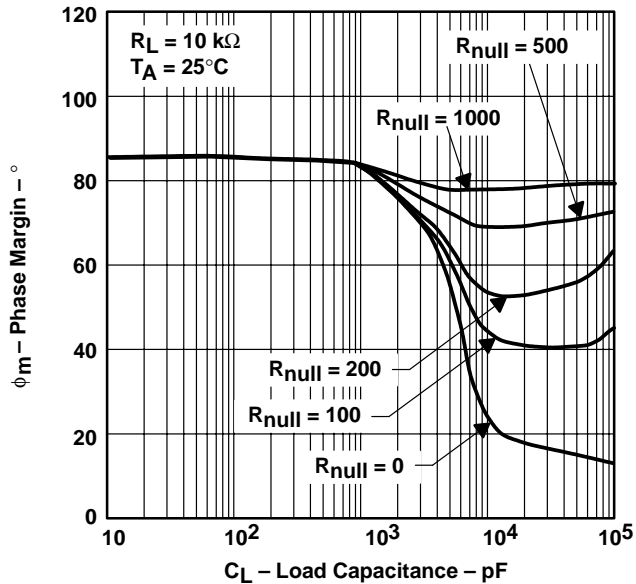
**Figure 46**

**GAIN-BANDWIDTH PRODUCT**  
**vs**  
**FREE-AIR TEMPERATURE**



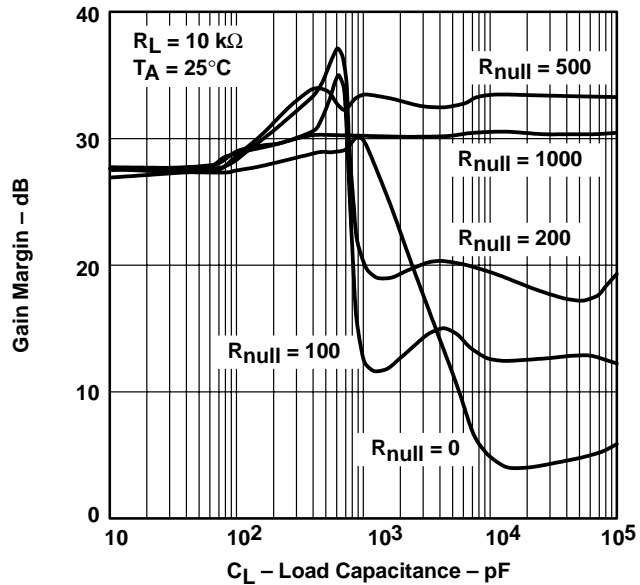
**Figure 47**

**PHASE MARGIN**  
**vs**  
**LOAD CAPACITANCE**



**Figure 48**

**GAIN MARGIN**  
**vs**  
**LOAD CAPACITANCE**



**Figure 49**

TYPICAL CHARACTERISTICS

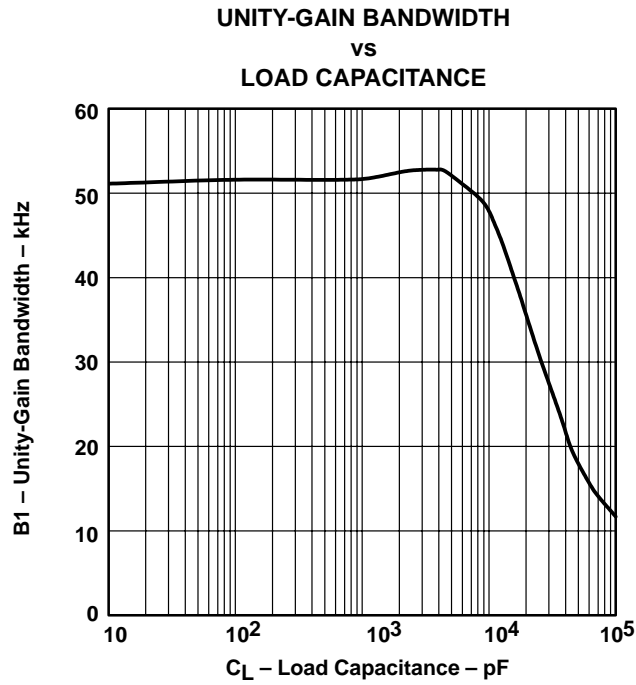


Figure 50

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9751401QHA	ACTIVE	CFP	U	10	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9751401QHA TLV2422M	<a href="#">Samples</a>
TLV2422AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2422AI	<a href="#">Samples</a>
TLV2422AIPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2422AI	<a href="#">Samples</a>
TLV2422CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	2422C	<a href="#">Samples</a>
TLV2422ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2422I	<a href="#">Samples</a>
TLV2422IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2422I	<a href="#">Samples</a>
TLV2422MUB	ACTIVE	CFP	U	10	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9751401QHA TLV2422M	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF TLV2422, TLV2422M :**

- Catalog : [TLV2422](#)
  
- Automotive : [TLV2422-Q1](#), [TLV2422-Q1](#)
  
- Military : [TLV2422M](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
  
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
  
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2422AIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV2422IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2422AIPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
TLV2422IDR	SOIC	D	8	2500	340.5	338.1	20.6

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9751401QHA	U	CFP	10	25	506.98	26.16	6220	NA
TLV2422AID	D	SOIC	8	75	505.46	6.76	3810	4
TLV2422AID	D	SOIC	8	75	507	8	3940	4.32
TLV2422CD	D	SOIC	8	75	505.46	6.76	3810	4
TLV2422CD	D	SOIC	8	75	507	8	3940	4.32
TLV2422ID	D	SOIC	8	75	505.46	6.76	3810	4
TLV2422ID	D	SOIC	8	75	507	8	3940	4.32
TLV2422MUB	U	CFP	10	25	506.98	26.16	6220	NA





D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

### NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW0008A



**PACKAGE OUTLINE**  
**TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

# EXAMPLE BOARD LAYOUT

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



# EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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