TEXAS INSTRUMENTS

TLV2460-Q1, TLV2460A-Q1, TLV2461-Q1, TLV2461A-Q1
TLV2462-Q1, TLV2462A-Q1, TLV2463-Q1, TLV2463A-Q1, TLV2464A-Q1

SGLS008G – MARCH 2003 – REVISED FEBRUARY 2018

TLV246xx-Q1 Low-Power Rail-to-Rail Input/Output Operational Amplifiers With Shutdown

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C6
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model C = 200 pF, R = 0)
- Rail-to-Rail Output Swing
- Gain Bandwidth Product: 6.4 MHz
- Output Drive Capability: ±80-mA
- Supply Current: 500 μA/Channel
- Input Noise Voltage: 11 nV/√Hz
- Slew Rate: 1.6 V/μs
- Micropower Shutdown Mode (TLV2460-Q1 and TLV2463-Q1): 0.3 μA/Channel
- Universal Operational Amplifier EVM
- Available in Single, Dual, and Quad Versions

2 Applications

- Clusters
- Telematics
- HEV/EV and Powertrains
- DC-to-DC Inverters
- Power Steering
- Lighting Modules
- Battery Management Systems

3 Description

The devices in the TLV246x-Q1 family of low-power rail-to-rail input/output operational amplifiers are designed for battery management systems in HEV/EV and Powertrain, and lighting and roof module systems in body and lighting applications. The input common-mode voltage range extends beyond the supply rails for maximum dynamic range in low-voltage systems. The amplifier output has rail-to-rail performance with high-output-drive capability, solving one of the limitations of older rail-to-rail input/output operational amplifiers. This rail-to-rail dynamic range and high output drive make the TLV246x-Q1 designed for buffering analog-to-digital converters.

The operational amplifier has 6.4-MHz bandwidth and a 1.6-V/μs slew rate with only 500-μA supply current, which provides good ac performance with low-power consumption. Devices are available with an optional shutdown terminal, which places the amplifier in an ultra-low supply-current mode (I_{DD} = 0.3 μA per channel). While in shutdown, the operational amplifier output is placed in a high-impedance state. DC applications are designed with an input noise voltage of 11 nV/√Hz and input offset voltage of 100 μV.

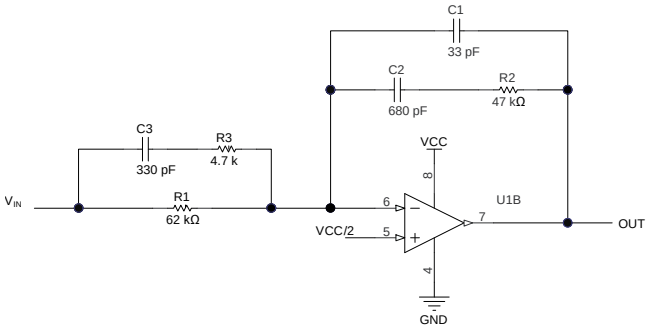
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV246x-Q1, TLV246xA-Q1	TSSOP (8)	4.40 mm × 3.00 mm
TLV2462-Q1, TLV2462A-Q1	SOIC (8)	3.91 mm × 4.90 mm
	TSSOP (8)	4.40 mm × 3.00 mm
	VSSOP (8)	3.00 mm × 3.00 mm
TLV246x-Q1, TLV246xA-Q1	TSSOP (14)	4.40 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) For all available device options, see the *Mechanical, Packaging, and Orderable Information*.

Typical Application



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (December 2015) to Revision G — **Page**

- Updated data sheet text to latest data sheet and translation standards ... 1
- Deleted "Input Offset Voltage: 100 µV" bullet from *Features* section ... 1
- Deleted "Universal Operational Amplifier EVM" bullet from *Features* section ... 1
- Deleted TLV2464 device from document ... 1
- Deleted *Device Comparison* table ... 4
- Reformatted *Thermal Information* tables and table notes ... 6
- Changed I_{IO} and I_{IB} unit from pA to nA in *Electrical Characteristics: V_{DD} = 3 V* table ... 8
- Changed I_{IO} and I_{IB} unit from pA to nA in *Electrical Characteristics: V_{DD} = 5 V* table ... 9
- Reformatted document references in *Related Documentation* section ... 32

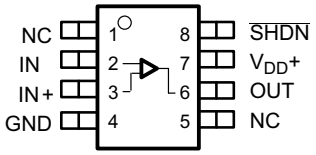
Changes from Revision E (October 2012) to Revision F — **Page**

- Added AEC-Q100 bulleted items ... 1
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted D package from TLV2460-Q1, TLV2461-Q1, TLV2463-Q1, and TLV2464A-Q1 and added TLV246xA-Q1 device number to pin drawings ... 4
- Deleted table note 3 reference to JESD 51-5 from *Absolute Maximum Ratings* table ... 6

Changes from Revision D (September 2010) to Revision E **Page**

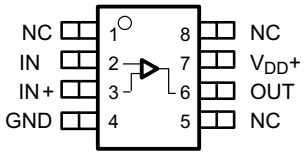
5 Pin Configuration and Functions

TLV2460-Q1, TLV2460A-Q1 PW Package
8-Pin TSSOP
Top View



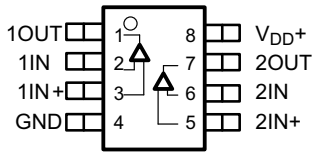
NC- no internal connection

TLV2461-Q1, TLV2461A-Q1 PW Package
8-Pin TSSOP
Top View



NC- no internal connection

TLV2462-Q1, TLV2462A-Q1 D, DGK, or PW Package
8-Pin SOIC, TSSOP, or VSSOP
Top View

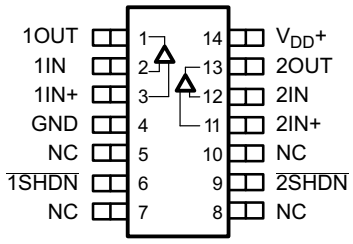


NC – No internal connection

Pin Functions

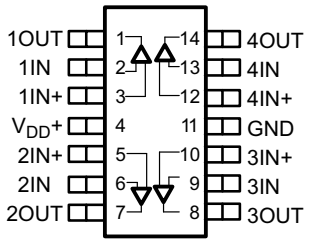
PIN				I/O	DESCRIPTION
NAME	TLV2460-Q1, TLV2460A-Q1	TLV2461-Q1, TLV2461A-Q1	TLV2462-Q1, TLV2462A-Q1		
1IN	—	—	2	I	Inverting input, channel 1
1IN+	—	—	3	I	Noninverting input, channel 1
1OUT	—	—	1	O	Output, channel 1
2IN	—	—	6	I	Inverting input, channel 2
2IN+	—	—	5	I	Noninverting input, channel 2
2OUT	—	—	7	O	Output, channel 2
IN	2	2	—	I	Inverting input
IN+	3	3	—	I	Noninverting input
GND	4	4	4	—	Negative (lowest) supply
NC	1, 5	1, 5, 8	—	—	No internal connection
OUT	6	6	—	O	Output
$\overline{SHDN}$	8	—	—	I	Shutdown
$V_{DD}+$	7	7	8	—	Positive (highest) supply

TLV2463-Q1, TLV2463A-Q1 PW Package
14-Pin TSSOP
Top View



NC – No internal connection

TLV2463-Q1, TLV2463A-Q1 PW Package
14-Pin TSSOP
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	TLV2463-Q1, TLV2463A-Q1	TLV2464A-Q1		
1IN	2	2	I	Inverting input, channel 1
1IN+	3	3	I	Noninverting input, channel 1
1OUT	1	1	O	Output, channel 1
$\overline{1SHDN}$	6	—	I	Shutdown for channel 1
2IN	12	6	I	Inverting input, channel 2
2IN+	11	5	I	Noninverting input, channel 2
2OUT	13	7	O	Output, channel 2
$\overline{2SHDN}$	9	—	I	Shutdown for channel 2
3N	—	9	I	Inverting input, channel 3
3IN+	—	10	I	Noninverting input, channel 3
3OUT	—	8	O	Output, channel 3
4IN	—	13	I	Inverting input, channel 4
4IN+	—	12	I	Noninverting input, channel 4
4OUT	—	14	O	Output, channel 4
IN	—	—	I	Inverting input
IN+	—	—	I	Noninverting input
GND	4	11	—	Negative (lowest) supply
NC	5, 7, 8, 10	—	—	No internal connection
OUT	—	—	O	Output
$\overline{SHDN}$	—	—	I	Shutdown
V_{DD}+	14	4	—	Positive (highest) supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Supply voltage (2), V_{DD}		6	V
Differential input voltage, V_{ID}	–0.2	V_{DD} + 0.2	V
Input current (any input), I_I	–200	200	mA
Output current, I_O	–175	175	mA
Total input current (into V_{DD+}), I_I		175	mA
Total output current (out of GND), I_O		175	mA
Operating free-air temperature, T_A	–40	125	°C
Maximum junction temperature, T_J		150	°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds		260	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to GND.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{DD}	Supply voltage	Single-supply	2.7	6	V
		Split-supply	±1.35	±3	
V_{ICR}	Common-mode input voltage range (1)		–0.2	V_{DD} + 0.2	V
T_A	Operating free-air temperature		–40	125	°C
	Shutdown on and off voltage level (1)	V_{IH}	2		V
		V_{IL}		0.7	

(1) Relative to voltage on the GND terminal of the device

6.4 Thermal Information: TLV2460x-Q1

THERMAL METRIC (1)		TLV2460x-Q1 PW (TSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	185.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	69	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	114.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	112.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Thermal Information: TLV2461x-Q1

THERMAL METRIC[1]		TLV2461x-Q1 PW (TSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	185.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	69	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	114.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	112.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Thermal Information: TLV2462-Q1

THERMAL METRIC[1]		TLV2462-Q1 D (SOIC) 8 PINS	TLV2462-Q1 DGK (VSSOP) 8 PINS	TLV2462-Q1 PW (TSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	120.1	179.3	183.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	68.3	71.1	67	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60.4	100.4	112.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	20.6	10.7	9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	59.9	98.8	110.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.7 Thermal Information: TLV2462A-Q1

THERMAL METRIC[1]		TLV2462A-Q1 D (SOIC) 8 PINS	TLV2462A-Q1 PW (TSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	120.1	185.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	68.3	69	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60.4	114.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	20.6	9.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	59.9	112.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.8 Thermal Information: TLV2463x-Q1

THERMAL METRIC[1]		TLV2463x-Q1 PW (TSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	185.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	69	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	114.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	112.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.9 Electrical Characteristics: V_{DD} = 3 V

at specified free-air temperature, V_{DD} = 3 V, (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{DD} = 3 V, V_{IC} = 1.5 V, V_O = 1.5 V, R_S = 50 Ω	TLV246x-Q1	T_A = 25°C		100	2000	µV
				Full range[1]			2200	
			TLV246xA-Q1	T_A = 25°C		150	1500	
				Full range[1]			1700	
α_{VIO}	Temperature coefficient of input offset voltage	V_{DD} = 3 V, V_{IC} = 1.5 V, V_O = 1.5 V, R_S = 50 Ω				2		µV/°C
I_{IO}	Input offset current	V_{DD} = 3 V, V_{IC} = 1.5 V, V_O = 1.5 V, R_S = 50 Ω		T_A = 25°C		2.8	7	nA
				Full range[1]			75	
I_{IB}	Input bias current	V_{IC} = 1.5 V, V_O = 1.5 V, R_S = 50 Ω		T_A = 25°C		4.4	14	nA
				Full range[1]			75	
V_{OH}	High-level output voltage	I_O = –2.5 mA		T_A = 25°C		2.9		V
				Full range[1]	2.8			
		I_O = –10 mA		T_A = 25°C		2.7		
				Full range[1]	2.5			
V_{OL}	Low-level output voltage	V_{IC} = 1.5 V, I_{OL} = 2.5 mA		T_A = 25°C		0.1		V
				Full range[1]			0.2	
		V_{IC} = 1.5 V, I_{OL} = 10 mA		T_A = 25°C		0.3		
				Full range[1]			0.5	
I_{OS}	Short circuit output current	Sourcing		T_A = 25°C		50		mA
				Full range[1]	20			
		Sinking		T_A = 25°C		40		
				Full range	20			
I_O	Output current	Measured 1 V from rail		T_A = 25°C		±40		mA
A_{VD}	Large-signal differential voltage amplification	R_L = 10 kΩ		T_A = 25°C	90	105		dB
				Full range[1]	89			
$r_{i(d)}$	Differential input resistance			T_A = 25°C		10^9		Ω
$c_{i(o)}$	Common-mode input capacitance	f = 10 kHz		T_A = 25°C		7		pF
z_o	Closed-loop output impedance	f = 100 kHz, A_V = 10		T_A = 25°C		33		Ω
CMRR	Common-mode rejection ratio	V_{ICR} = 0 V to 3 V, R_S = 50 Ω		T_A = 25°C	66	80		dB
				Full range[1]	60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}$ / ΔV_{IO})	V_{DD} = 2.7 V to 6 V, V_{IC} = V_{DD} / 2; no load		T_A = 25°C	80	85		dB
				Full range[1]	75			
		V_{DD} = 3 V to 5 V, V_{IC} = V_{DD} / 2; no load		T_A = 25°C	85	95		
				Full range[1]	80			
I_{DD}	Supply current (per channel)	V_O = 1.5 V; no load		T_A = 25°C		0.5	0.575	mA
				Full range[1]			0.9	
$I_{DD(SHDN)}$	Supply current in shutdown (TLV2460-Q1, TLV2463-Q1)	$\overline{SHDN}$ < 0.7 V, per channel in shutdown		T_A = 25°C		0.3		µA
				Full range[1]			2.5	

(1) Full range is –40°C to +125°C.

6.10 Electrical Characteristics: V_{DD} = 5 V

at specified free-air temperature, V_{DD} = 5 V, (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{DD} = 5 V, V_{IC} = 2.5 V, V_O = 2.5 V, R_S = 50 Ω	TLV246x-Q1	T_A = 25°C		150	2000	µV
				Full range[1]			2200	
			TLV246xA-Q1	T_A = 25°C		150	1500	
				Full range[1]			1700	
α_{VIO}	Temperature coefficient of input offset voltage	V_{DD} = 5 V, V_{IC} = 2.5 V, V_O = 2.5 V, R_S = 50 Ω				2		µV/°C
I_{IO}	Input offset current	V_{DD} = 5 V, V_{IC} = 2.5 V, V_O = 2.5 V, R_S = 50 Ω		T_A = 25°C		0.3	7	nA
				Full range[1]			60	
I_{IB}	Input bias current	V_{DD} = 5 V, V_{IC} = 2.5 V, V_O = 2.5 V, R_S = 50 Ω		T_A = 25°C		1.3	14	nA
				Full range[1]			60	
V_{OH}	High-level output voltage	I_O = –2.5 mA		T_A = 25°C		4.9		V
				Full range[1]	4.8			
		I_O = –10 mA	TLV246x-Q1, TLV246xA-Q1	T_A = 25°C		4.8		
				Full range[1]	4.7			
			TLV2462QDGKRQ1	T_A = 25°C		4.8		
				Full range[1]	4.4			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V, I_{OL} = 2.5 mA		T_A = 25°C		0.1		V
				Full range[1]			0.2	
		V_{IC} = 2.5 V, I_{OL} = 10 mA		T_A = 25°C		0.2		
				Full range[1]			0.3	
I_{OS}	Short circuit output current	Sourcing		T_A = 25°C		145		mA
				Full range[1]	60			
		Sinking		T_A = 25°C		100		
				Full range[1]	60			
I_O	Output current	Measured 1 V from rail		T_A = 25°C		±80		mA
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, R_L = 10 kΩ, V_O = 1 V to 4 V		T_A = 25°C	92	109		dB
				Full range[1]	90			
$r_{i(d)}$	Differential input resistance			T_A = 25°C		10^9		Ω
$c_{i(o)}$	Common-mode input capacitance	f = 10 kHz		T_A = 25°C		7		pF
z_o	Closed-loop output impedance	f = 100 kHz, A_V = 10		T_A = 25°C		29		Ω
CMRR	Common-mode rejection ratio	V_{ICR} = 0 V to 5 V, R_S = 50 Ω		T_A = 25°C	71	85		dB
				Full range[1]	60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}$ / ΔV_{IO})	V_{DD} = 2.7 V to 6 V, V_{IC} = V_{DD} / 2; no load		T_A = 25°C	80	85		dB
				Full range[1]	75			
		V_{DD} = 3 V to 5 V, V_{IC} = V_{DD} / 2; no load		T_A = 25°C	85	95		
				Full range[1]	80			
I_{DD}	Supply current (per channel)	V_O = 2.5 V; no load		T_A = 25°C		0.55	0.65	mA
				Full range[1]			1	

(1) Full range is –40°C to +125°C.

Electrical Characteristics: V_{DD} = 5 V (continued)

at specified free-air temperature, V_{DD} = 5 V, (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{DD(SHDN)}$	Supply current in shutdown (TLV2460-Q1, TLV2463-Q1)	$\overline{SHDN}$ < 0.7 V, Per channel in shutdown	T_A = 25°C		1		μA
			Full range[1]			3	

6.11 Operating Characteristics: V_{DD} = 3 V

V_{DD} = 3 V , at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_{O(PP)}$ = 2 V C_L = 160 pF R_L = 10 kΩ		T_A = 25°C	1	1.6		V/μs
				Full range[1]	0.8			
V_n	Equivalent input noise voltage	f = 100 Hz		T_A = 25°C		16		nV/√Hz
		f = 1 kHz				11		
I_n	Equivalent input noise current	f = 1 kHz		T_A = 25°C		0.13		pA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 2 V R_L = 10 kΩ, f = 1 kHz	A_V = 1	T_A = 25°C		0.006%		
			A_V = 10			0.02%		
			A_V = 100			0.08%		
$t_{(on)}$	Amplifier turn-on time	A_V = 1 R_L = 10 kΩ	Both channels	T_A = 25°C		7.6		μs
			Channel 1 only, Channel 2 on			7.65		
$t_{(off)}$	Amplifier turn-off time	A_V = 1 R_L = 10 kΩ	Both channels	T_A = 25°C		333		ns
			Channel 1 only, Channel 2 on			328		
			Channel 2 only, Channel 1 on			329		
	Gain-bandwidth product	f = 10 kHz C_L = 160 pF R_L = 10 kΩ		T_A = 25°C		5.2		MHz
t_s	Settling time	$V_{(STEP)PP}$ = 2 V A_V = –1 C_L = 10 pF R_L = 10 kΩ	0.1%	T_A = 25°C		1.47		μs
			0.01%			1.78		
		$V_{(STEP)PP}$ = 2 V A_V = –1 C_L = 56 pF R_L = 10 kΩ	0.1%			1.77		
			0.01%			1.98		
φ_m	Phase margin at unity gain	R_L = 10 kΩ C_L = 160 pF		T_A = 25°C		44		°
	Gain margin	R_L = 10 kΩ C_L = 160 pF		T_A = 25°C		7		dB

(1) Full range is –40°C to +125°C.

6.12 Operating Characteristics: V_{DD} = 5 V

V_{DD} = 5 V, at specified free-air temperature, (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_{O(PP)}$ = 2 V C_L = 160 pF R_L = 10 kΩ		T_A = 25°C	1	1.6		V/μs
				Full range(1)	0.8			
V_n	Equivalent input noise voltage	f = 100 Hz		T_A = 25°C		14		nV/√Hz
		f = 1 kHz				11		
I_n	Equivalent input noise current	f = 100 Hz		T_A = 25°C		0.13		pA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 4 V R_L = 10 kΩ f = 10 kHz	A_V = 1	T_A = 25°C		0.004%		
			A_V = 10			0.01%		
			A_V = 100			0.04%		
$t_{(on)}$	Amplifier turn-on time	A_V = 1 R_L = 10 kΩ	Both channels	T_A = 25°C		7.6		μs
			Channel 1 only, Channel 2 on			7.65		
			Channel 2 only, Channel 1 on			7.25		
$t_{(off)}$	Amplifier turn-off time	A_V = 1 R_L = 10 kΩ	Both channels	T_A = 25°C		333		ns
			Channel 1 only, Channel 2 on			328		
			Channel 2 only, Channel 1 on			329		
	Gain-bandwidth product	f = 10 kHz C_L = 160 pF R_L = 10 kΩ		T_A = 25°C		6.4		MHz
t_s	Settling time	$V_{(STEP)PP}$ = 2 V A_V = –1 C_L = 10 pF R_L = 10 kΩ	0.1%	T_A = 25°C		1.53		μs
			0.01%			1.83		
		$V_{(STEP)PP}$ = 2 V A_V = –1 C_L = 56 pF R_L = 10 kΩ	0.1%			3.13		
			0.01%			3.33		
φ_m	Phase margin at unity gain	R_L = 10 kΩ C_L = 160 pF		T_A = 25°C		45		°
	Gain margin	R_L = 10 kΩ C_L = 160 pF		T_A = 25°C		7		dB

(1) Full range is –40°C to +125°C.

6.13 Typical Characteristics

CONDITION STATEMENT TBD

Table 1. Table of Graphs

GRAPH TITLE		FIGURE
V_{IO}	Input offset voltage vs common-mode input voltage	1, 2
I_{IB}	Input bias current vs free-air temperature	3, 4
I_{IO}	Input offset current vs free-air temperature	3, 4
V_{OH}	High-level output voltage vs high-level output current	5, 6
V_{OL}	Low-level output voltage vs low-level output current	7, 8
$V_{O(PP)}$	Maximum peak-to-peak output voltage vs frequency	9, 10
	Open-loop gain vs frequency	11, 12
	Phase vs frequency	11, 12
A_{VD}	Differential voltage amplification vs load resistance	13
	Capacitive load vs load resistance	14
z_o	Output impedance vs frequency	15, 16
CMRR	Common-mode rejection ratio vs frequency	17
k_{SVR}	Supply-voltage rejection ratio vs frequency	18, 19
I_{DD}	Supply current vs supply voltage	20
	Supply current vs free-air temperature	21
	Amplifier turnon characteristics	22
	Amplifier turnoff characteristics	23
	Supply current turnon	24
	Supply current turnoff	25
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SR	Slew rate vs load capacitance	27
V_n	Equivalent input noise voltage vs frequency	28, 29
	Equivalent input noise voltage vs common-mode input voltage	30, 31
THD	Total harmonic distortion vs frequency	32, 33
THD + N	Total harmonic distortion plus noise vs peak-to-peak signal amplitude	34, 35
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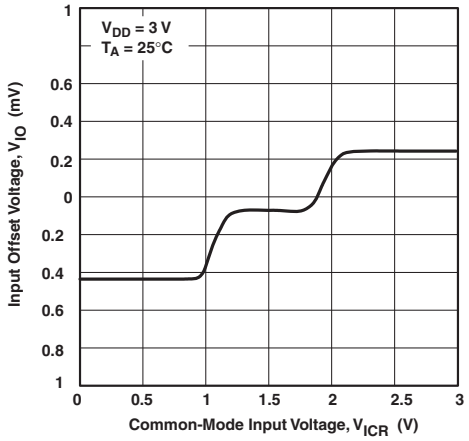
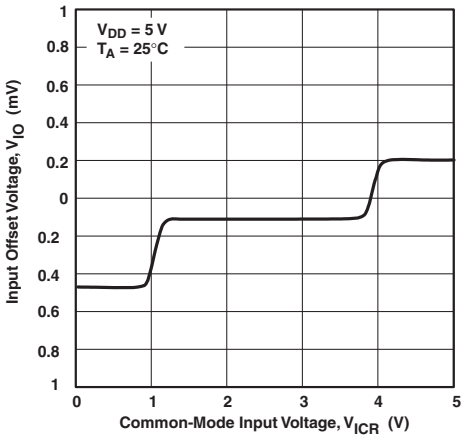
	Phase margin vs load capacitance	36
	Phase margin vs free-air temperature	37
	Gain-bandwidth product vs supply voltage	38
	Gain-bandwidth product vs free-air temperature	39
	Large signal follower	40, 41
	Small signal follower	42, 43
	Inverting large signal	44, 45
	Inverting small signal	46, 47



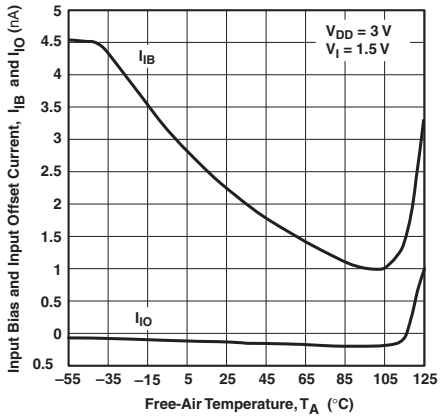
V_{DD} = 3 V

Figure 1. Input Offset Voltage vs Common-Mode Input Voltage



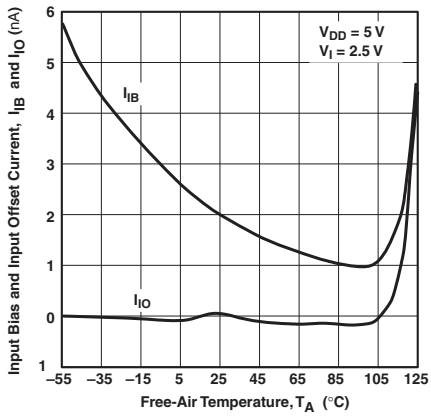
V_{DD} = 5 V

Figure 2. Input Offset Voltage vs Common-Mode Input Voltage



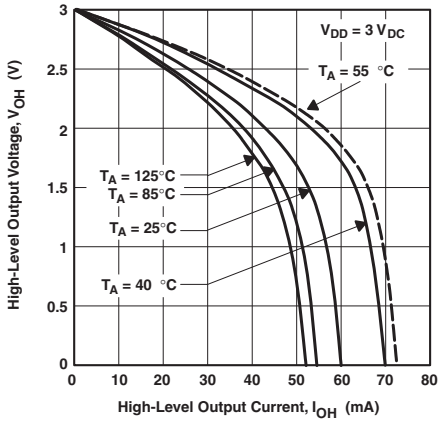
V_{DD} = 3 V

Figure 3. Input Bias and Input Offset Current vs Free-Air Temperature



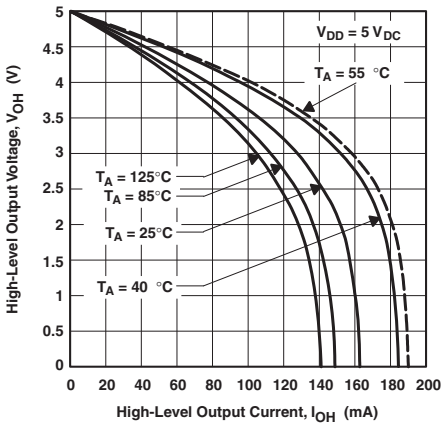
V_{DD} = 5 V

Figure 4. Input Bias and Input Offset Current vs Free-Air Temperature



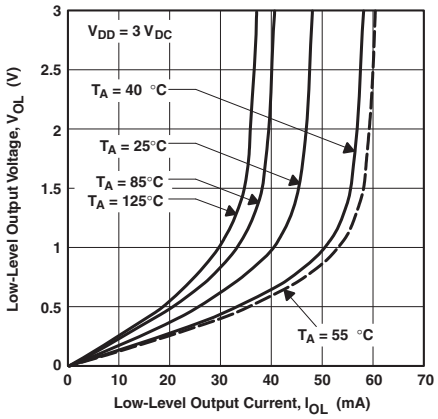
V_{DD} = 3 V_{DC}

Figure 5. High-Level Output Voltage vs High-Level Output Current



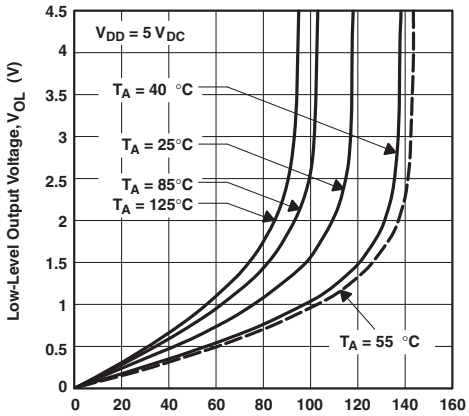
V_{DD} = 5 V_{DC}

Figure 6. High-Level Output Voltage vs High-Level Output Current



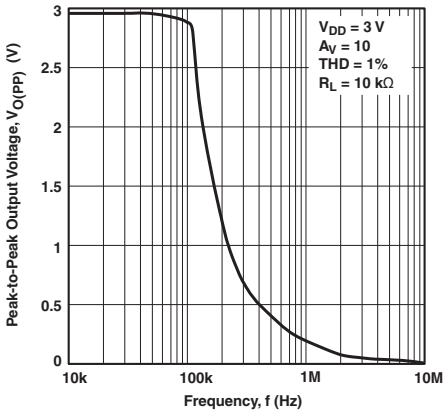
V_{DD} = 3 V_{DC}

Figure 7. Low-Level Output Voltage vs Low-Level Output Current



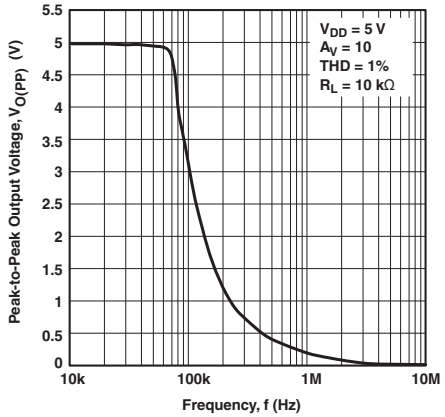
V_{DD} = 5 V_{DC}

Figure 8. Low-level Output Voltage vs Low-Level Output Current



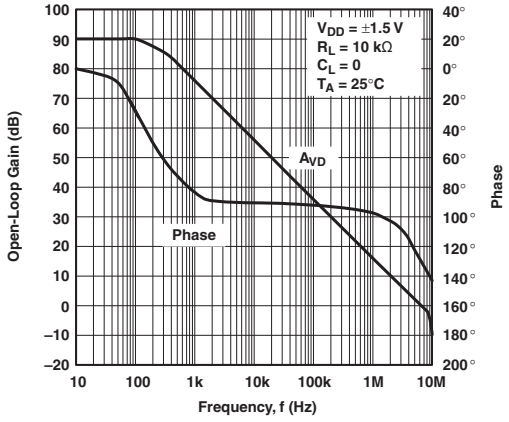
V_{DD} = 3 V

Figure 9. Peak-to-Peak Output Voltage vs Frequency



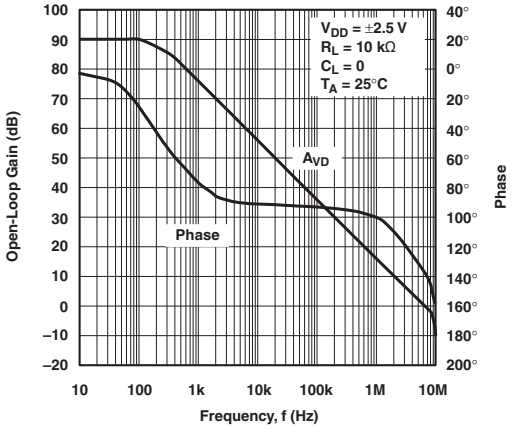
V_{DD} = 5 V

Figure 10. Peak-to-Peak Output Voltage vs Frequency



V_{DD} = ±1.5 V

Figure 11. Open-Loop Gain and Phase vs Frequency



V_{DD} = ±2.5 V

Figure 12. Open-Loop Gain and Phase vs Frequency

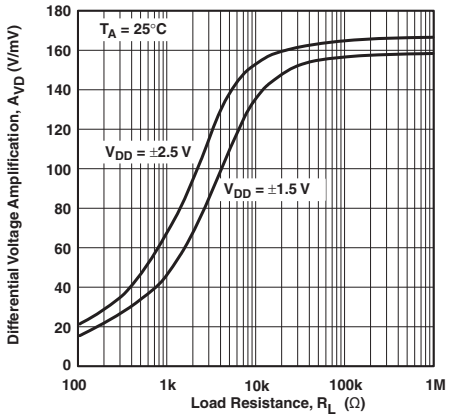


Figure 13. Differential Voltage Amplification vs Load Resistance

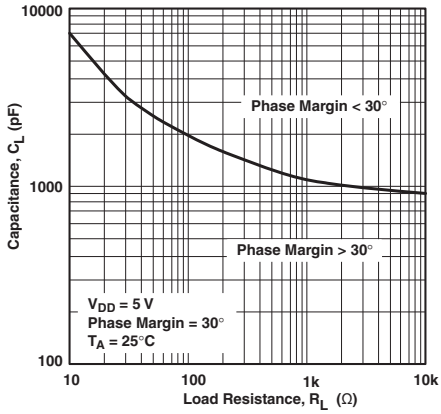
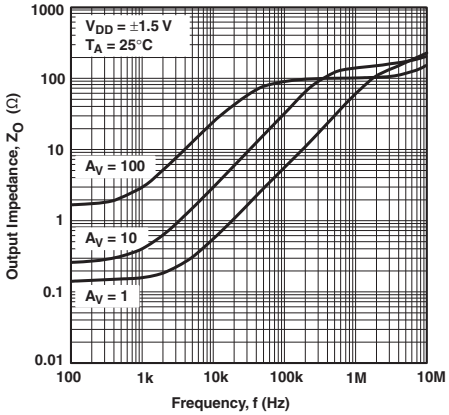
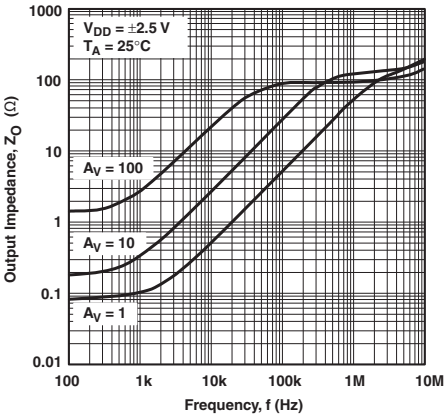


Figure 14. Capacitive Load vs Load Resistance



V_{DD} = ±1.5 V

Figure 15. Output Impedance vs Frequency



V_{DD} = ±2.5 V

Figure 16. Output Impedance vs Frequency

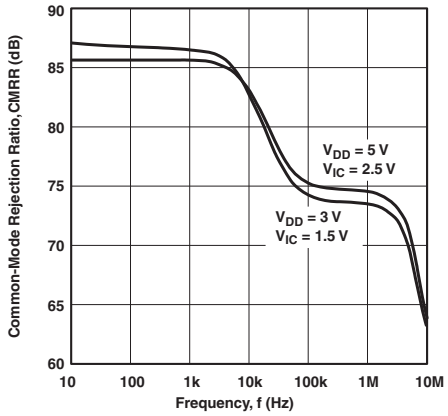
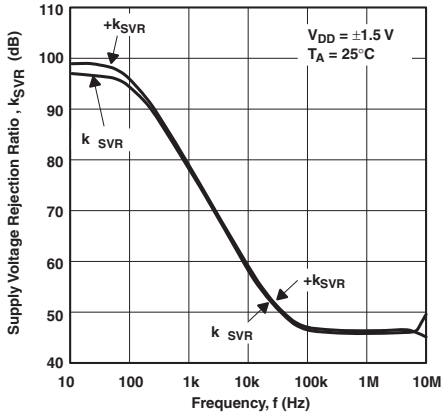
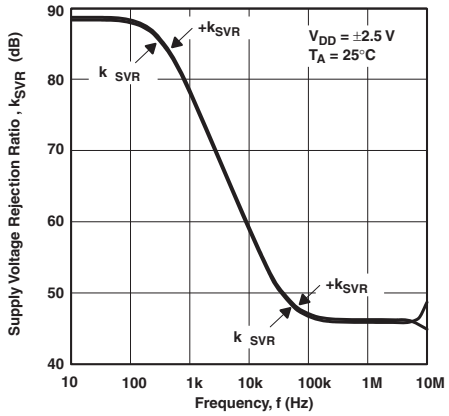


Figure 17. Common-Mode Rejection Ratio vs Frequency



V_{DD} = ±1.5 V

Figure 18. Supply-Voltage Rejection Ratio vs Frequency



V_{DD} = ±2.5 V

Figure 19. Supply-Voltage Rejection Ratio vs Frequency

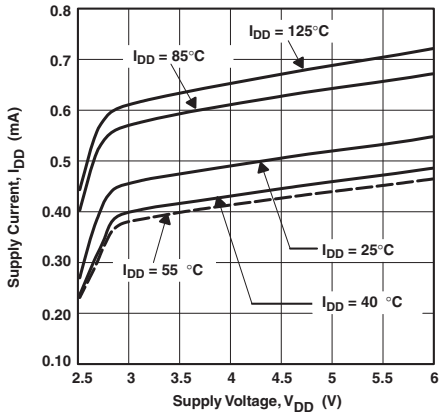


Figure 20. Supply Current vs Supply Voltage

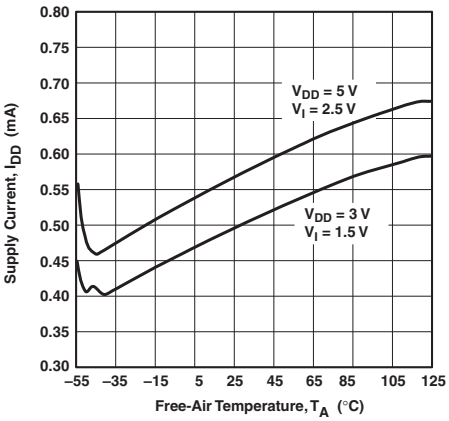


Figure 21. Supply Current vs Free-Air Temperature

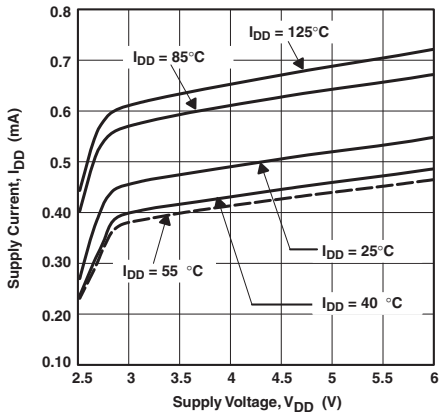


Figure 22. Amplifier With a Shutdown Pulse Turnon Characteristics

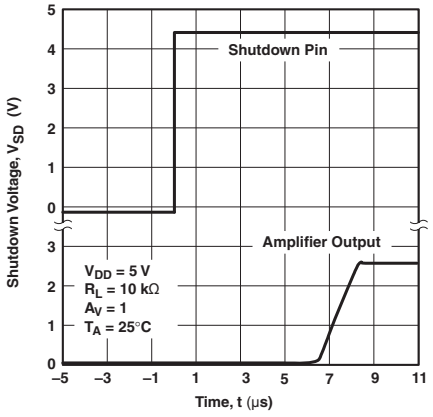


Figure 23. Amplifier With a Shutdown Pulse Turnoff Characteristics

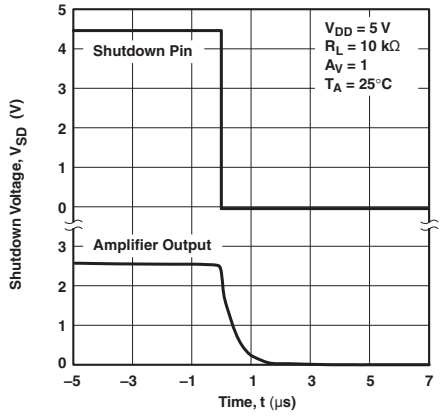


Figure 24. Supply Current With a Shutdown Pulse Turnon Characteristics

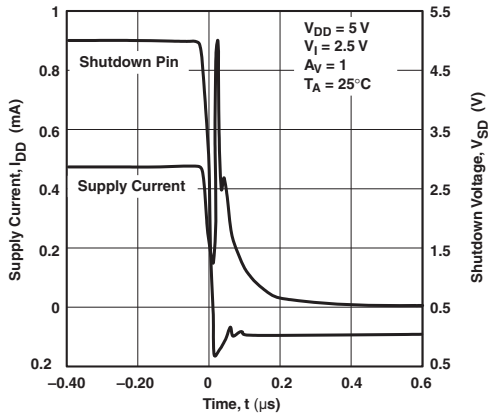


Figure 25. Turnoff Supply Current With a Shutdown Pulse

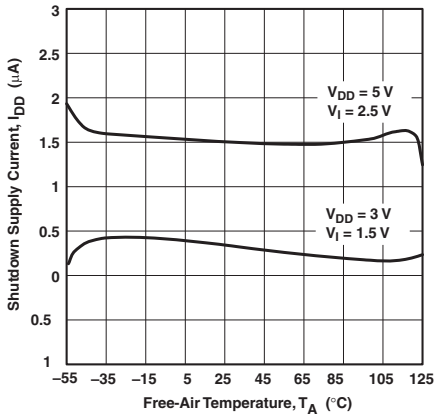


Figure 26. Shutdown Supply Current vs Free-Air Temperature

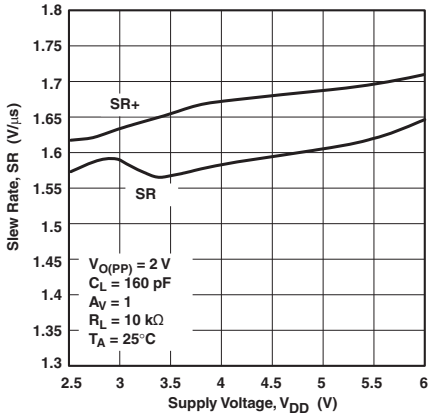


Figure 27. Slew Rate vs Supply Voltage

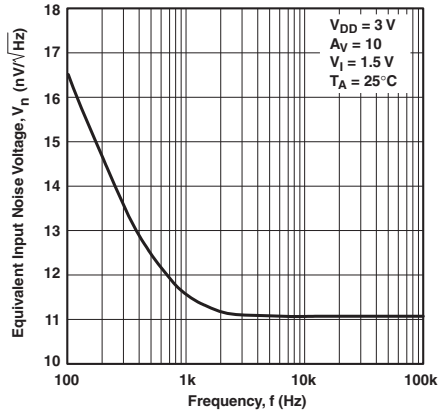


Figure 28. Equivalent Input Noise Voltage vs Frequency

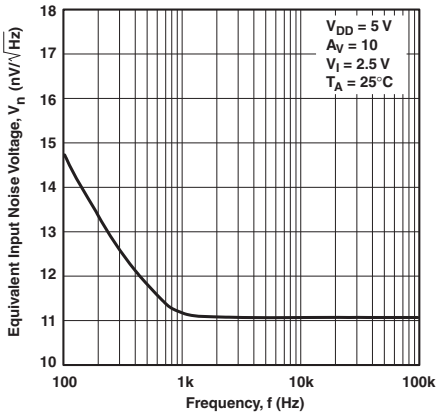


Figure 29. Equivalent Input Noise Voltage vs Frequency

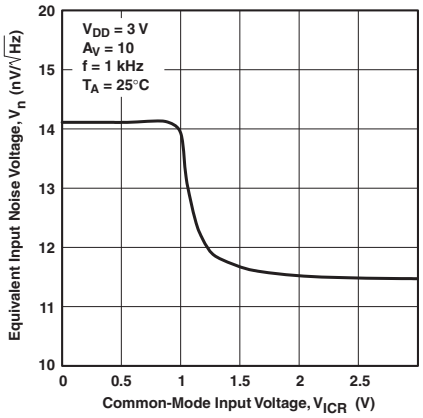


Figure 30. Equivalent Input Noise Voltage vs Common-Mode Input Voltage

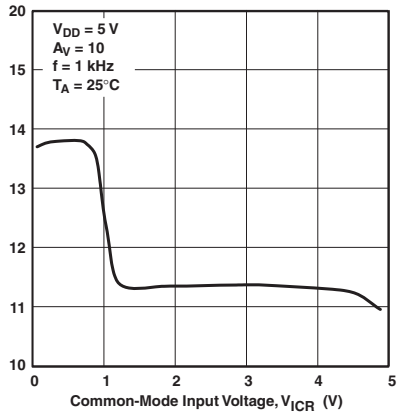
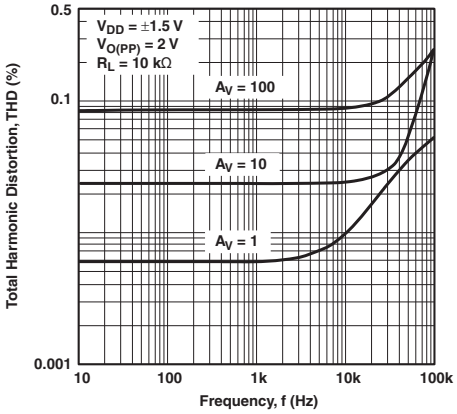
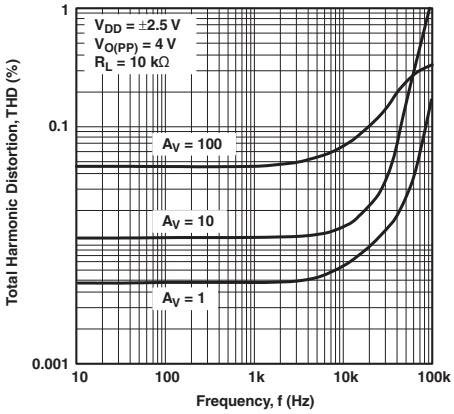


Figure 31. Equivalent Input Noise Voltage vs Common-Mode Input Voltage



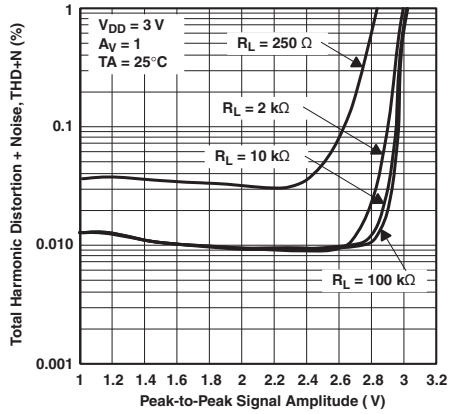
V_{DD} = ±1.5 V

Figure 32. Total Harmonic Distortion vs Frequency



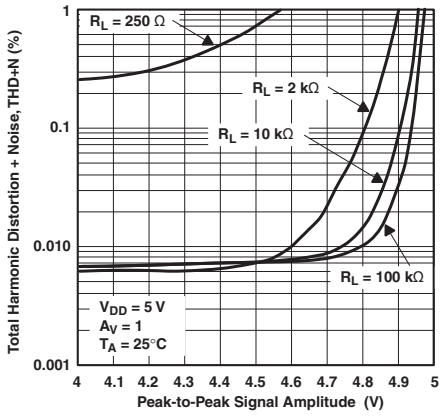
V_{DD} = ±2.5 V

Figure 33. Total Harmonic Distortion vs Frequency



V_{DD} = 3 V

Figure 34. Total Harmonic Distortion Plus Noise vs Peak-to-Peak Signal Amplitude



V_{DD} = 5 V

Figure 35. Total Harmonic Distortion Plus Noise vs Peak-to-Peak Signal Amplitude

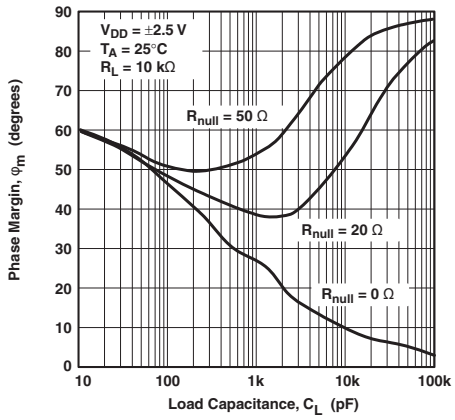


Figure 36. Phase Margin vs Load Capacitance

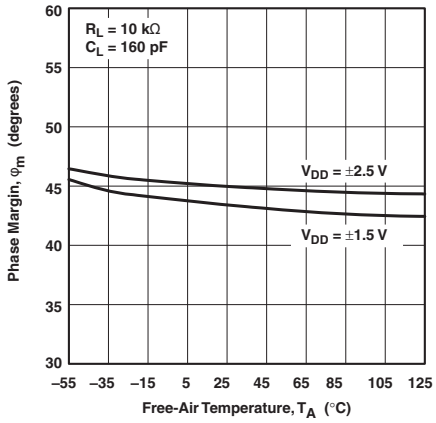


Figure 37. Phase Margin vs Free-Air Temperature

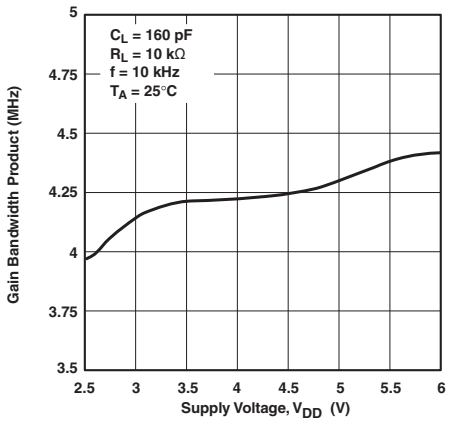


Figure 38. Gain Bandwidth Product vs Supply Voltage

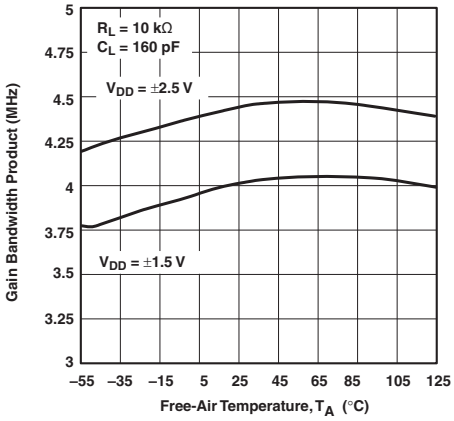
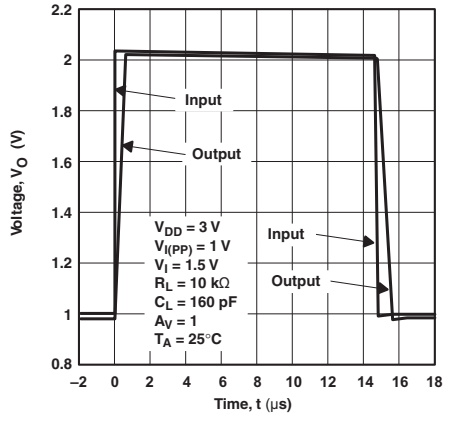
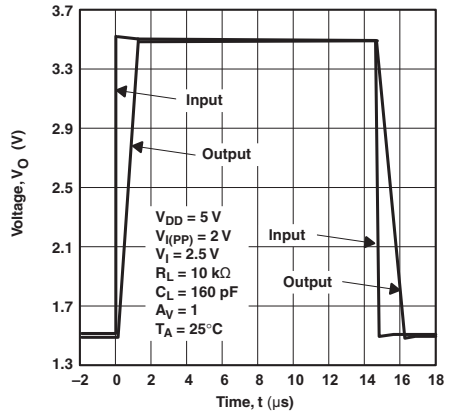


Figure 39. Gain Bandwidth Product vs Free-Air Temperature



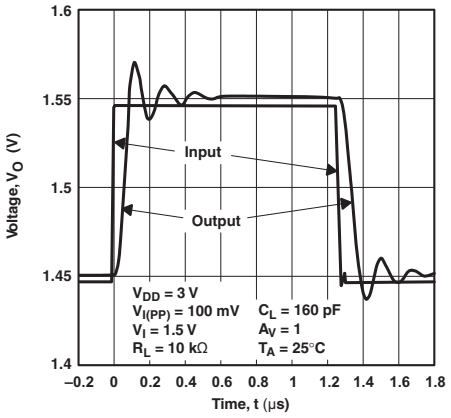
V_{DD} = 3 V

Figure 40. Large Signal Follower



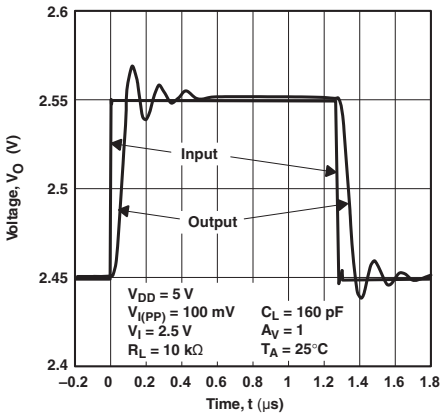
V_{DD} = 5 V

Figure 41. Large Signal Follower



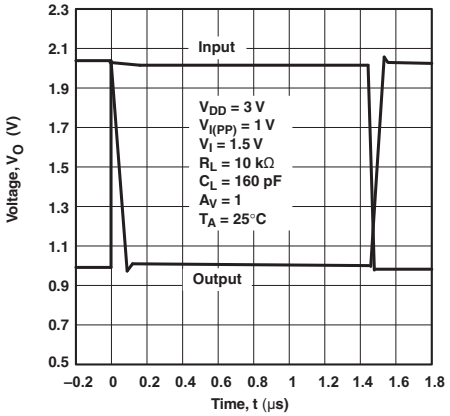
V_{DD} = 3 V

Figure 42. Small Signal Follower



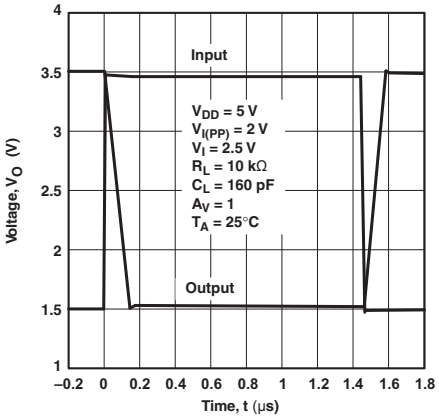
V_{DD} = 5 V

Figure 43. Small Signal Follower



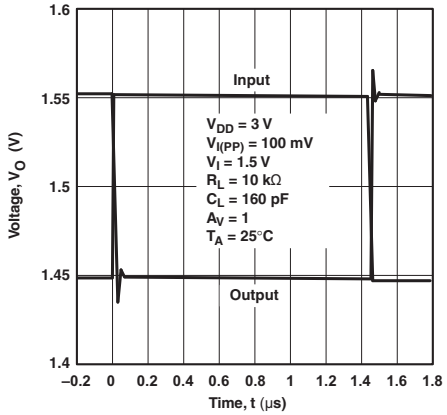
V_{DD} = 3 V

Figure 44. Inverting Large Signal



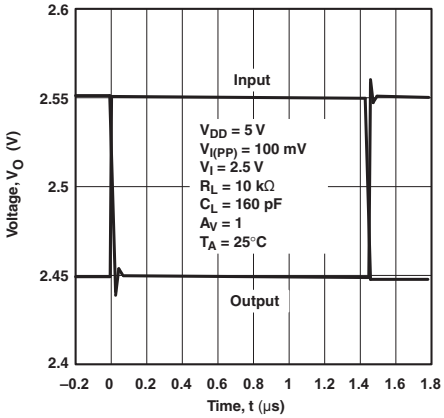
V_{DD} = 5 V

Figure 45. Inverting Large Signal



V_{DD} = 3 V

Figure 46. Inverting Small Signal



V_{DD} = 5 V

Figure 47. Inverting Small Signal

7 Parameter Measurement Information

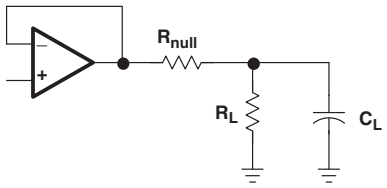


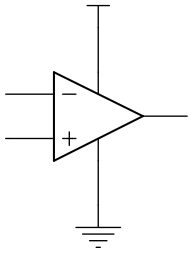
Figure 48. Capacitive Load Drive

8 Detailed Description

8.1 Overview

The TLV246x-Q1 family of devices are low-power rail-to-rail input and output operational amplifiers. The input common-mode voltage range extends beyond the supply rails for maximum dynamic range in a low-voltage system. The amplifier output has rail-to-rail performance with high drive capability, solving one of the limitations of older rail-to-rail input and output operational amplifiers

8.2 Functional Block Diagram



8.3 Feature Description

The TLV246x-Q1 family features 6.4-MHz bandwidth and voltage noise of 11 nV/√Hz with performance rated from 2.7 V to 6 V across an automotive temperature range (–40ºC to +125ºC). This family is designed for a wide range of automotive applications.

8.3.1 Driving a Capacitive Load

When the amplifier configuration is in this manner, capacitive loading directly on the output decreases the phase margin of the device leading to high-frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, TI recommends placing a resistor in series (R_{NULL}) with the output of the amplifier; see Figure 49. A minimum value of 20 Ω works well for most applications.

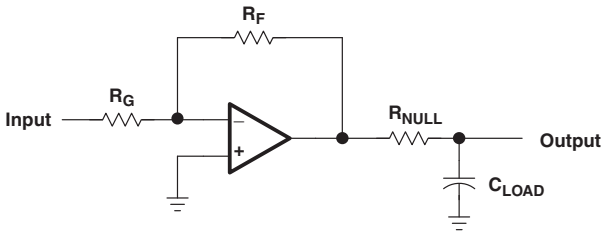
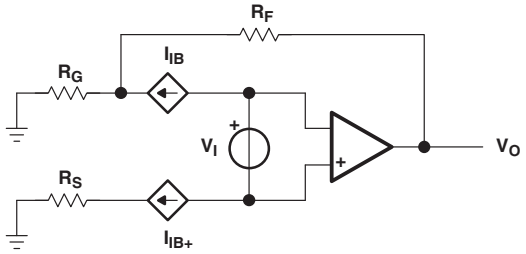


Figure 49. Driving a Capacitive Load

Feature Description (continued)

8.3.2 Offset Voltage

The output offset voltage (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input-bias currents (I_{IB}) times the corresponding gains. Use the schematic and formula in Figure 50 to calculate the output offset voltage.

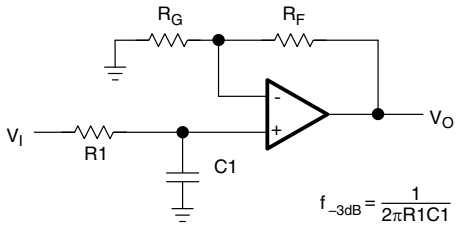


$$V_{OO} = V_{IO}\left(1+\left(\frac{R_F}{R_G}\right)\right) \pm I_{IB} + R_S\left(1+\left(\frac{R_F}{R_G}\right)\right) \pm I_{IB-}R_F$$

Figure 50. Output Offset Voltage Model

8.3.3 General Configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. To limit bandwidth, place an RC filter at the noninverting terminal of the amplifier (see Figure 51).



$$\frac{V_O}{V_I} = \left(1+\frac{R_F}{R_G}\right)\left(\frac{1}{1+sR1C1}\right)$$

Figure 51. Single-Pole Low-Pass Filter

If even more attenuation is required, a multiple pole filter is required. Use a Sallen-Key filter for this task; see Figure 52. For best results, the amplifier must have a bandwidth that is eight to ten times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.

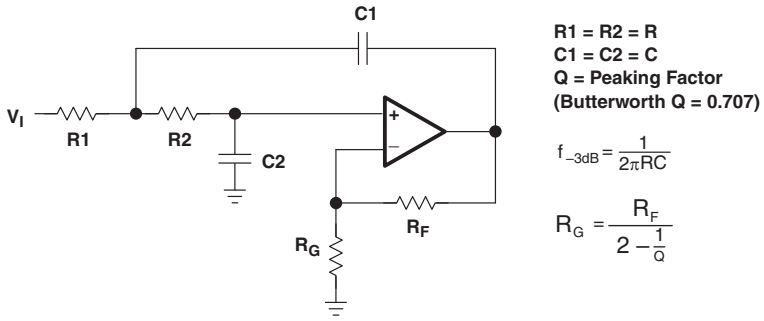


Figure 52. 2-Pole Low-Pass Sallen-Key Filter

Feature Description (continued)

8.3.4 General Power Dissipation Considerations

For a given θ_{JA} value, the maximum power dissipation is shown in Figure 53 and is calculated by Equation 1:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}}\right) \quad (1)$$

Where:

- P_D = Maximum power dissipation of TLV246x-Q1 (watts)
- T_{MAX} = Absolute maximum junction temperature (150°C)
- T_A = Ambient free-air temperature (°C)
- $\theta_{JA} = \theta_{JC} + \theta_{CA}$
- θ_{JC} = Thermal coefficient from junction to case
- θ_{CA} = Thermal coefficient from case to ambient air (°C/W)

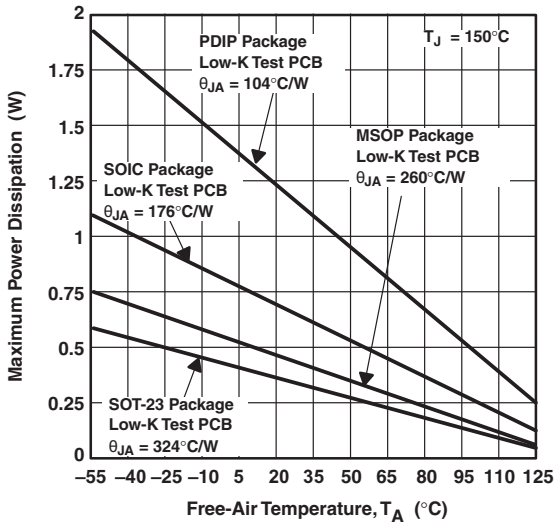


Figure 53. Maximum Power Dissipation vs Free-Air Temperature

8.4 Device Functional Modes

The TLV2461-Q1, TLV2462-Q1, and TLV2464A-Q1 devices power on when the supply is connected. These devices can operate with a single supply or dual supplies, depending on the application. The devices are in their full performance once the supply is above the recommended value. The TLV2460-Q1 and TLV2463-Q1 devices feature a shutdown mode, which reduces the quiescent current to 0.3 μA in shutdown mode.

8.4.1 Shutdown Function

Two members of the TLV246x-Q1 family (TLV2460-Q1 and TLV2463-Q1) feature a shutdown terminal that conserves battery life in portable applications. When the shutdown terminal is tied low, the supply current is reduced to 0.3 μA per channel, the amplifier is disabled and the outputs are placed in a high-impedance mode. To enable the amplifier, leave the shutdown terminal floating or pull the shutdown terminal high. When the shutdown terminal is left floating, take care to ensure that parasitic leakage current at the shutdown terminal does not inadvertently place the operational amplifier into shutdown. The shutdown terminal threshold is always referenced to V_{DD} / 2. As a result, when operating the device with split-supply voltages (for example, ±2.5 V), the shutdown terminal must be pulled to V_{DD}– (not GND) to disable the operational amplifier.

The output of the amplifier with a shutdown pulse is shown in Figure 22, Figure 23, Figure 24, and Figure 25. The amplifier is powered with a single 5-V supply and configured as a noninverting configuration with a gain of 5. The amplifier turnon and turnoff times are measured from the 50% point of the shutdown pulse to the 50% point of the output waveform. The times for the single, dual, and quad are listed in the data tables.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Most DC-to-DC converters use output-filter ceramic capacitors with very low equivalent series resistance (ESR). This causes a double pole at the resonance frequency $\frac{1}{2\pi\sqrt{LC}}$.

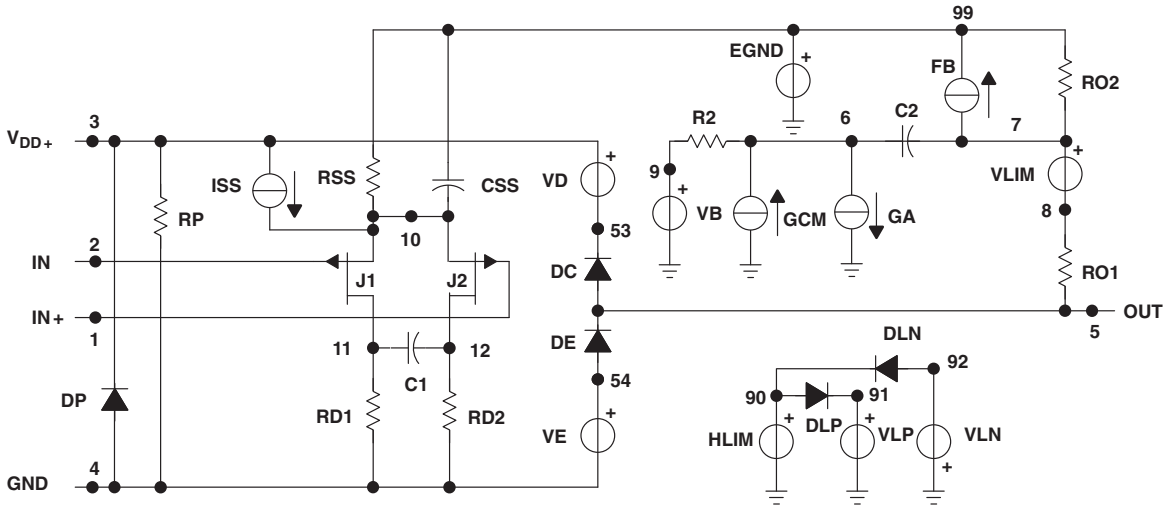
To achieve an adequate bandwidth and phase margin for the DC-to-DC converter, the device requires compensation around the $\frac{1}{2\pi\sqrt{LC}}$ resonance frequency. To achieve this, configure the error amplifier as type-3 compensation. The TLV2426x-Q1 series features a wide bandwidth UGBD of 6 MHz with rail-to-rail output for increased dynamic range. These features are designed for DC-to-DC loop compensation with any LC filter.

9.1.1 Macromodel Information

Macromodel information provided was derived using Microsim Parts™ Release 8, the model generation software used with Microsim PSpice™. The Boyle macromodel (1) and subcircuit in Figure 54 are generated using the TLV246x-Q1 typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters are generated to a tolerance of 20% (in most cases):

(1) G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers," *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit




```
.SUBCKT TLV246X   1 2 3 4 5
C1      11    12    2.46034E-12
C2      6     7     10.0000E-12
CSS     10    99    443.21E-15
DC      5     53    DY
DE      54    5     DY
DLP     90    91    DX
DLN     92    90    DX
DP      4     3     DX
EGND    99    0     POLY (2) (3,0) (4,0) 0 .5 .5
FB      7     99    POLY (5) VB VC VE VLP
+ VLN 0 21.600E6 – 1E3 1E3 22E6 – 22E6
GA      6     0     11      12 345.26E- 6
GCM     0     6     10      99 15.4226E- 9
ISS     10    4     DC 18.850E- 6
HLIM    90    0     VLIM 1K
J1      11    2     10 JX1
J2      12    1     10 JX2
R2      6     9     100.00E3
RD1     3     11    2.8964E3
RD2     3     12    2.8964E3
R01     8     5     5.6000
R02     7     99    6.2000
RP      3     4     8.9127
RSS     10    99    10.610E6
VB      9     0     DC 0
VC      3     53    DC .7836
VE      54    4     DC .7436
VLIM    7     8     DC 0
VLP     91    0     DC 117
VLN     0     92    DC 117
.MODEL DX D (IS=800.00E–18)
.MODEL DY D (IS=800.00E–18 Rs = 1m Cjo=10p)
.MODEL JX1 NJF (IS=1.0000E–12 BETA=6.3239E–3
+ VTO=–1)
.MODEL JX2 NJF (IS=1.0000E–12 BETA=6.3239E–3
+ VTO=–1)
.ENDS
```

```
.subckt TLV_246Y 1 2 3 4 5 6
c1      11    12    2.4603E-12
c2      72    7     10.000E-12
css     10    99    443.21E-15
dc      70    53    dy
de      54    70    dy
dlp     90    91    dx
dln     92    90    dx
dp      4     3     dx
egnd    99    0     poly(2) (3,0) (4,0) 0 .5 .5
fb      7     99    poly(5) vb vc ve vlp vln 0
21.600E6 – 1E3 1E3 22E6 – 22E6
ga      72    0     11 12 345.26E- 6
gcm     0     72    10 99 15.422E- 9
iss     74    4     dc 18.850E- 6
hlim    90    0     vlim 1K
j1      11    2     10 jx1
j2      12    1     10 jx2
r2      72    9     100.00E3
rd1     3     11    2.8964E3
rd2     3     12    2.8964E3
ro1     8     70    5.6000
ro2     7     99    6.2000
rp      3     71    8.9127
rss     10    99    10.610E6
rs1     6     4     1G
rs2     6     4     1G
rs3     6     4     1G
rs4     6     4     1G
s1      71    4     6 4 s1x
s2      70    5     6 4 s1x
s3      10    74    6 4 s1x
s4      74    4     6 4 s2x
vb      9     0     dc 0
vc      3     53    dc .7836
ve      54    4     dc .7436
vlim    7     8     dc 0
vlp     91    0     dc 117
vln     0     92    dc 117
.model dx D(Is=800.00E–18)
.model dy D(Is=800.00E–18 Rs=1m Cjo=10p)
.model jx1 NJF(Is=1.0000E–12 Beta=6.3239E–3 Vto=–1)
.model jx2 NJF(Is=1.0000E–12 Beta=6.3239E–3 Vto=–1)
.model s1x VSWITCH(Roff=1E8 Ron=1.0 Voff=2.5 Von=0.0)
.model s2x  VSWITCH(Roff=1E8 Ron=1.0 Voff=0 Von=2.5)
.ends
```

Figure 54. Boyle Macromodel and Sub-Circuit

9.2 Typical Application

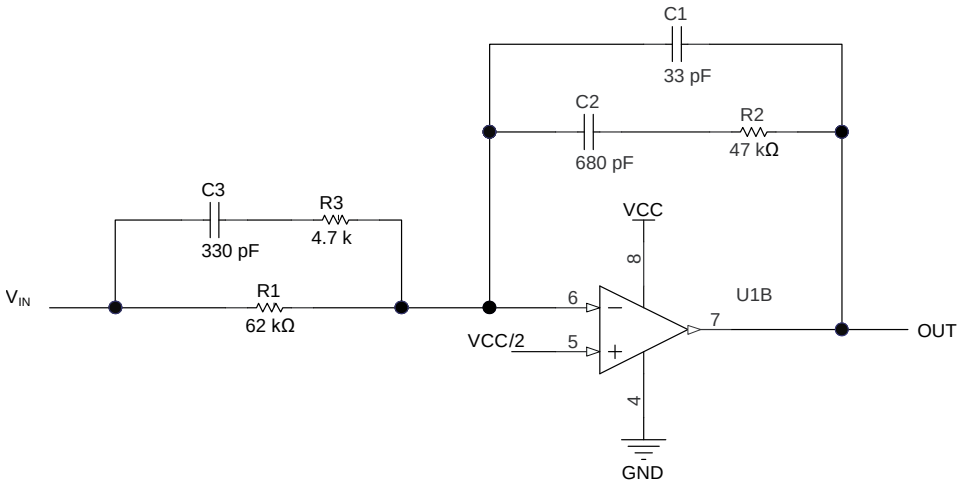


Figure 55. Typical Operational Amplifier Application

9.2.1 Design Requirements

See Table 2 for design requirements.

Table 2. Recommended Design Parameters

PARAMETER	VALUE
Supply voltage	5 V
Reference voltage	2.5 V
Input voltage	2.5 V DC and maximum ripple 40 mV peak-to-peak
Capacitors	Better than X5R
Resistors	Better than 2% tolerance

9.2.2 Detailed Design Procedure

The following section shows the detailed design procedure. See Equation 2 for the type-3 compensation gain.

$$\text{Type 3 Compensation Gain} = \frac{(1 + R2C2s)\,(1 + (R1 + R3)C3s)}{R1(C1 + C2)s\left(1 + R2\,\frac{C1C2}{C1 + C2}s\right)(1 + R3Cs)} \quad (2)$$

Type-3 compensation poles and zeros are shown in the preferred asymptotic graph; see Figure 56. Relocate the compensation poles and zeroes by changing the values of the resistors and capacitors according to the compensation requirement. The operational amplifier cannot achieve the preferred case because of the open-loop gain and phase limitation of the amplifier.

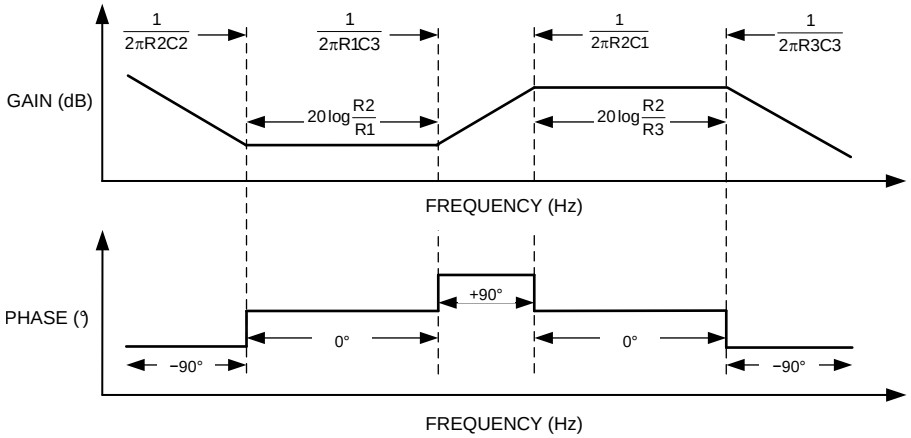


Figure 56. Preferred Asymptotic Graph

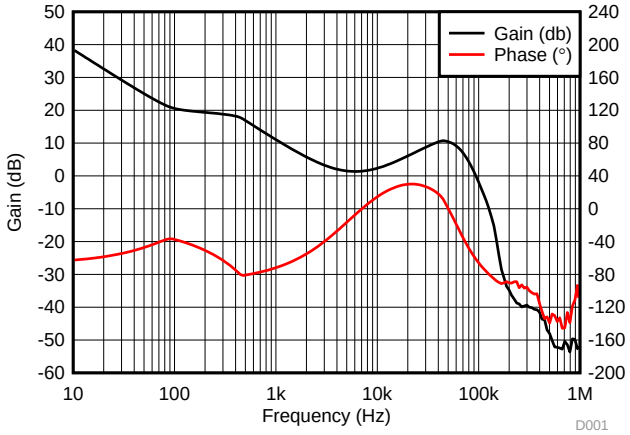
The poles and zeros are calculated assuming C2 >> C1 and R1 >> R3. This assumption is correct because the C1 and R3 components set the high frequencies.

This TLV226x-Q1 device type-3 compensation circuit design boosts the gain and phase for the DC-to-DC converter around 30-KHz resonance frequencies. This corresponds to 1 µH and 22 µF for the output filter.

The operational amplifier is configured as type-2 compensation by omitting the C3 capacitor. Type-2 compensates the DC-to-DC converter with an output capacitor with a series resistor ESR; see Equation 3.

$$\text{Type 2 Compensation Gain} = \frac{(1 + R2C2s)}{R1(C1 + C2)\ s\ (1 + R2\frac{C1C2}{C1 + C2}\ s)} \quad (3)$$

9.2.3 Application Curve



Frequency: 10 Hz to 1 MHz Gain boost = 12 dB around 30 KHz Phase boost = 30º around 30 KHz

Figure 57. Gain and Phase Plot

10 Power Supply Recommendations

The TLV246X-Q1 family of devices operation specification is from 2.7 V to 6 V for a single power supply and ±1.35 V to ±3 V for dual power supplies.

TI recommends placing a 0.1-µF bypass capacitor close to the power supply pins to reduce errors coupling in from noisy or high-impedance power supplies.

11 Layout

11.1 Layout Guidelines

To achieve the levels of high performance of the TLV246x-Q1, follow proper printed-circuit board design techniques. A general set of guidelines is shown in the following list.

- TI recommends using a ground plane on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane is removed to minimize the stray capacitance.
- Use a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor must always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor must be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer must strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- TI does not recommend using sockets. The additional lead inductance in the socket pins often leads to stability problems. For best implementation, solder surface-mount packages directly to the printed circuit board.
- Optimum high performance is achieved when stray series inductance is minimized. The circuit layout must be made as compact as possible, which minimizes the length of all trace runs. Take care to pay attention to the inverting input of the amplifier; keep the length as short as possible. This minimizes stray capacitance at the input of the amplifier.
- TI recommends using surface mount passive components for high performance amplifier circuits. Stray series inductance is reduced because of the low lead inductance of surface mount components.. The small size of surface-mount components leads to a compact layout, which minimizes stray inductance and capacitance. TI recommends that lead lengths be kept as short as possible if leaded components are used.

11.2 Layout Example

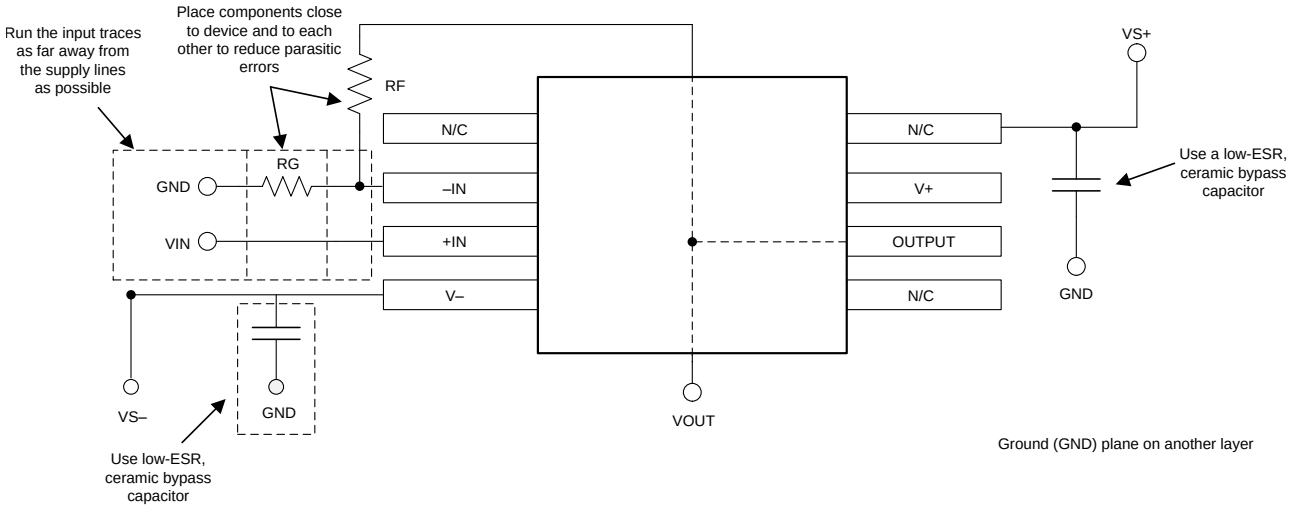


Figure 58. Operational Amplifier Board Layout for Noninverting Configuration

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *An audio circuit collection, Part 1*
- G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, “Macromodeling of Integrated Circuit Operational Amplifiers,” *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TLV2460-Q1	Click here	Click here	Click here	Click here	Click here
TLV2461-Q1	Click here	Click here	Click here	Click here	Click here
TLV2462-Q1	Click here	Click here	Click here	Click here	Click here
TLV2463-Q1	Click here	Click here	Click here	Click here	Click here
TLV2460A-Q1	Click here	Click here	Click here	Click here	Click here
TLV2461A-Q1	Click here	Click here	Click here	Click here	Click here
TLV2462A-Q1	Click here	Click here	Click here	Click here	Click here
TLV2463A-Q1	Click here	Click here	Click here	Click here	Click here
TLV2464A-Q1	Click here	Click here	Click here	Click here	Click here

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV2460AQPWRG4Q1	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2460AQ
TLV2461AQPWRG4Q1	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2461AQ
TLV2462AQDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2462AQ
TLV2462AQDRQ1.Z	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2462AQ
TLV2462AQPWRG4Q1	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2462AQ
TLV2462AQPWRQ1	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2462AQ
TLV2462QDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QVM
TLV2462QDGKRQ1.Z	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QVM
TLV2462QDRG4Q1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2462Q1
TLV2462QDRG4Q1.Z	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2462Q1
TLV2462QDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2462Q1
TLV2462QDRQ1.Z	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2462Q1
TLV2462QPWRG4Q1	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2462Q1
TLV2462QPWRG4Q1.Z	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2462Q1
TLV2463AQPWRG4Q1	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2463AQ1
TLV2463AQPWRG4Q1.Z	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2463AQ1
TLV2464AQPWRG4Q1	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2464AQ
TLV2464AQPWRQ1	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2464AQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV2460A-Q1, TLV2461A-Q1, TLV2462-Q1, TLV2462A-Q1, TLV2463A-Q1, TLV2464A-Q1 :

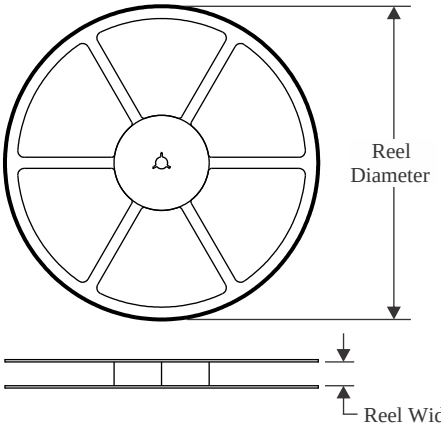
- Catalog : TLV2460A, TLV2461A, TLV2462, TLV2462A, TLV2463A, TLV2464A
- Enhanced Product : TLV2462A-EP, TLV2464A-EP
- Military : TLV2462M, TLV2462AM, TLV2463AM

NOTE: Qualified Version Definitions:

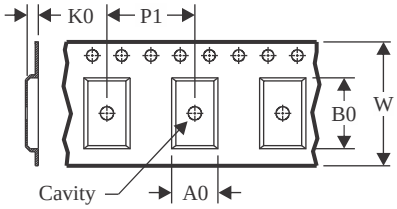
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

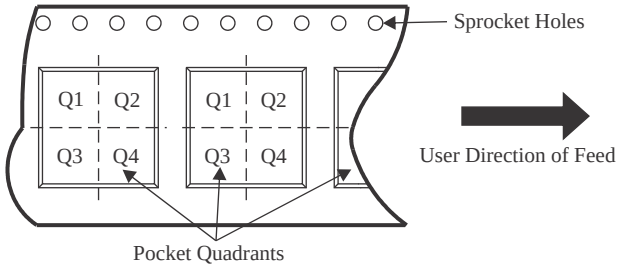


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

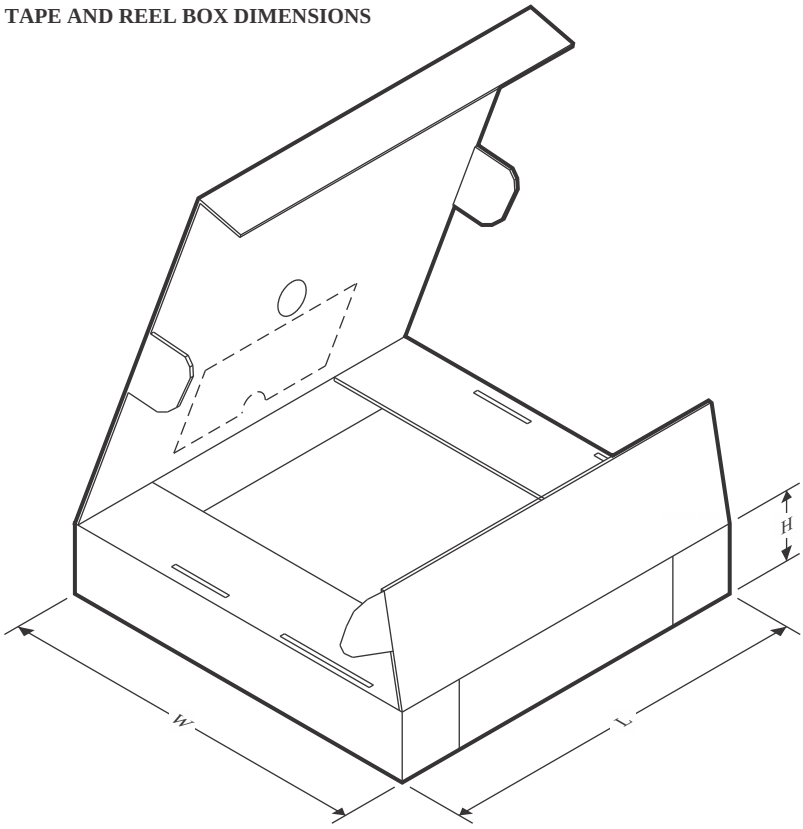
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2460AQPWRG4Q1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV2461AQPWRG4Q1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV2462AQPWRG4Q1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV2462AQPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV2462QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2462QPWRG4Q1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV2463AQPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2464AQPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2464AQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

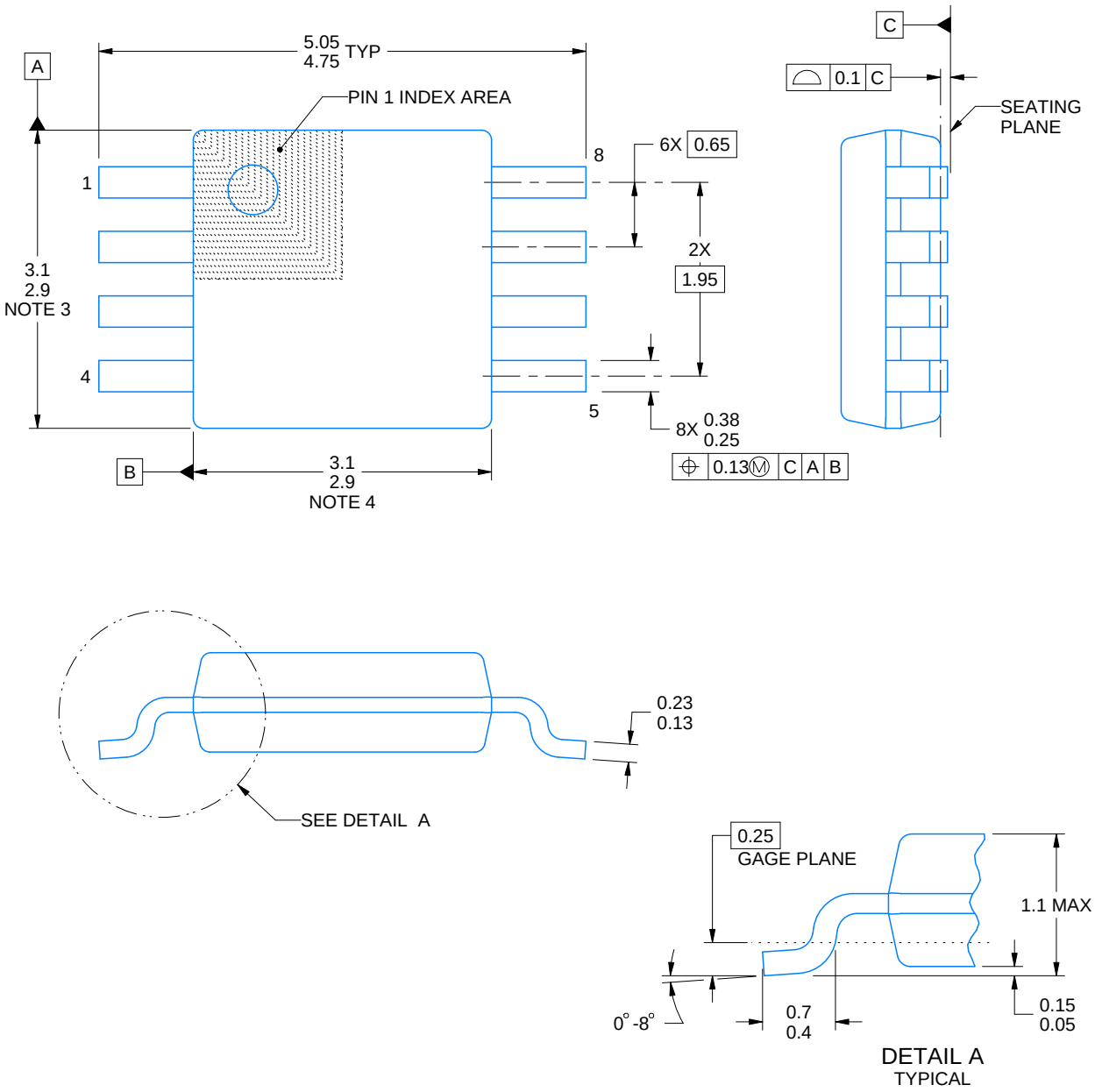
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2460AQPWRG4Q1	TSSOP	PW	8	2000	367.0	367.0	35.0
TLV2461AQPWRG4Q1	TSSOP	PW	8	2000	367.0	367.0	35.0
TLV2462AQPWRG4Q1	TSSOP	PW	8	2000	367.0	367.0	35.0
TLV2462AQPWRQ1	TSSOP	PW	8	2000	356.0	356.0	35.0
TLV2462QDGKRQ1	VSSOP	DGK	8	2500	346.0	346.0	29.0
TLV2462QPWRG4Q1	TSSOP	PW	8	2000	367.0	367.0	35.0
TLV2463AQPWRG4Q1	TSSOP	PW	14	2000	367.0	367.0	35.0
TLV2464AQPWRG4Q1	TSSOP	PW	14	2000	367.0	367.0	35.0
TLV2464AQPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

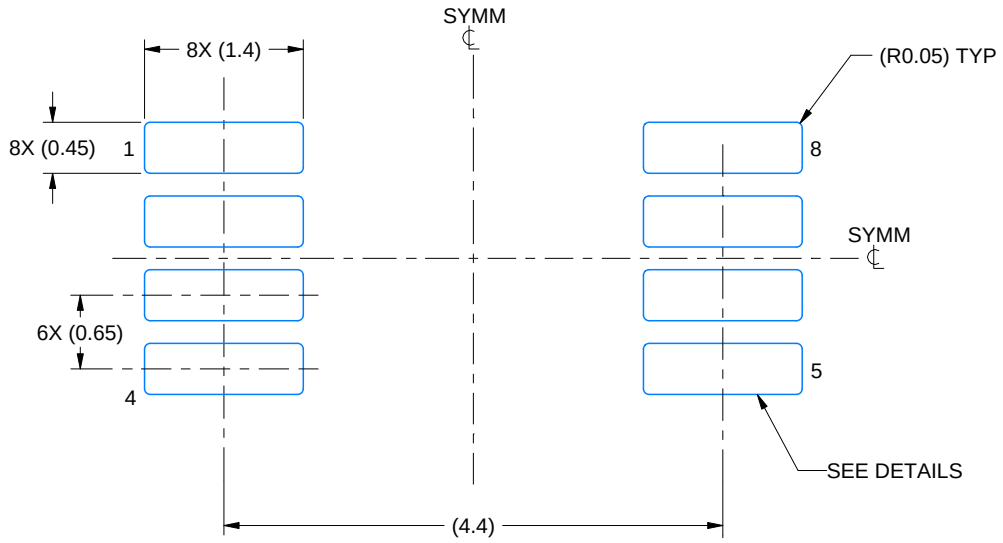
SMALL OUTLINE PACKAGE



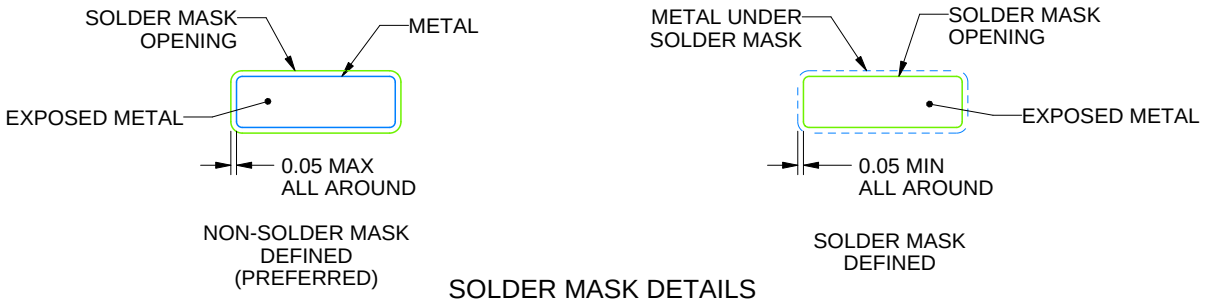
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

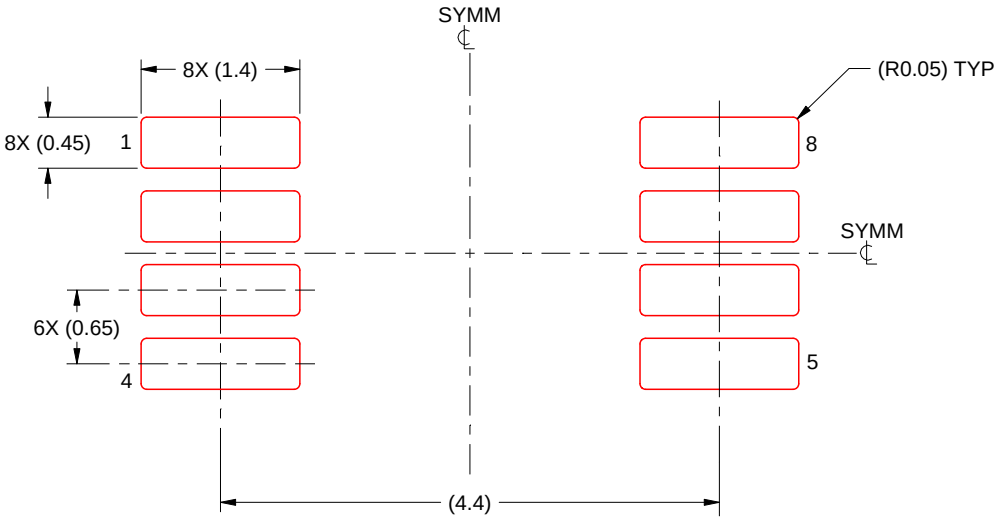


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

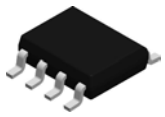


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

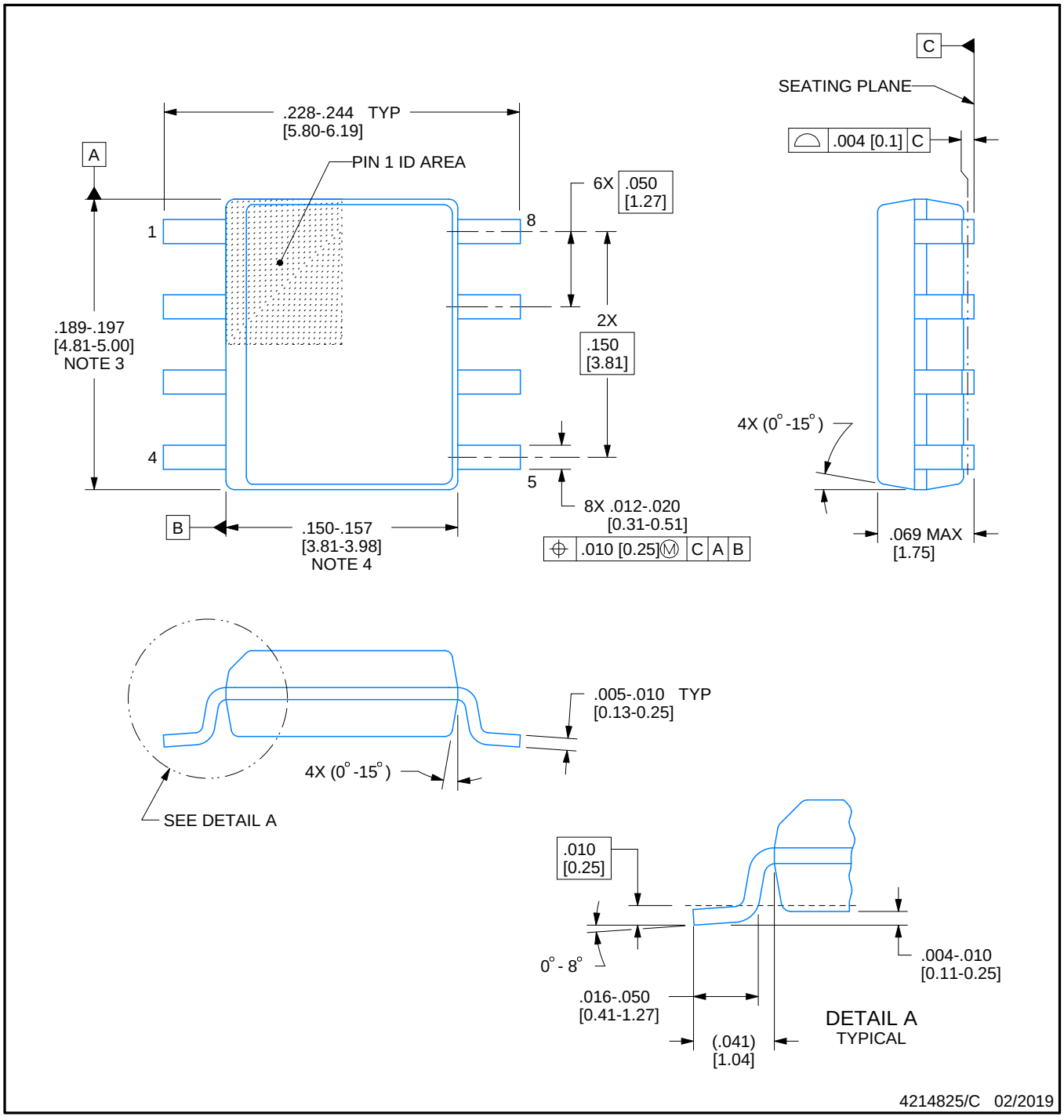


PACKAGE OUTLINE

D0008A

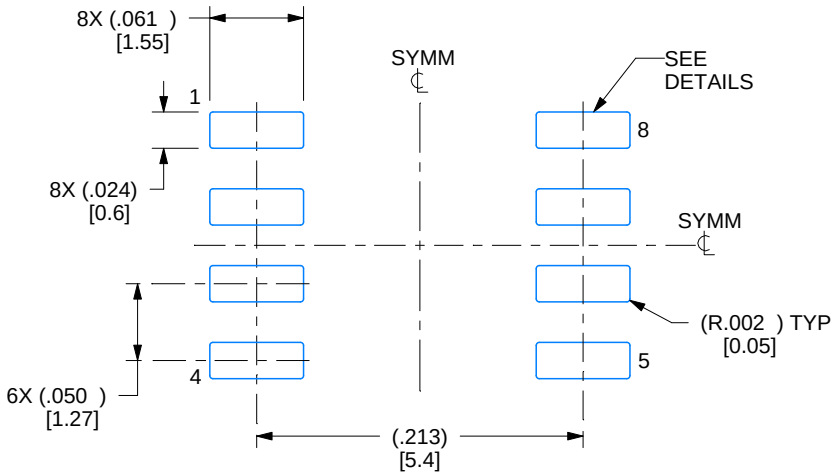
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

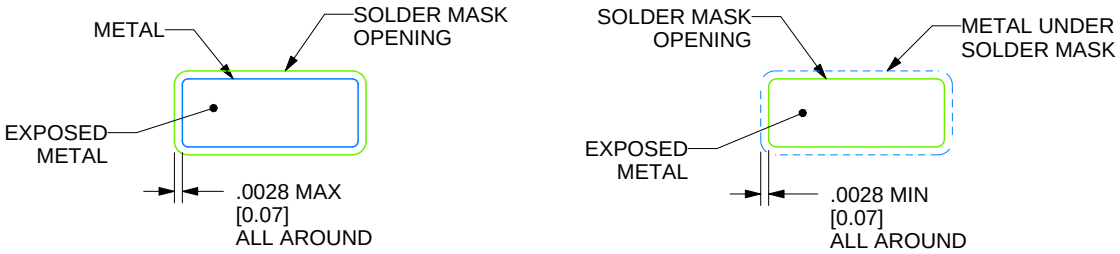


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

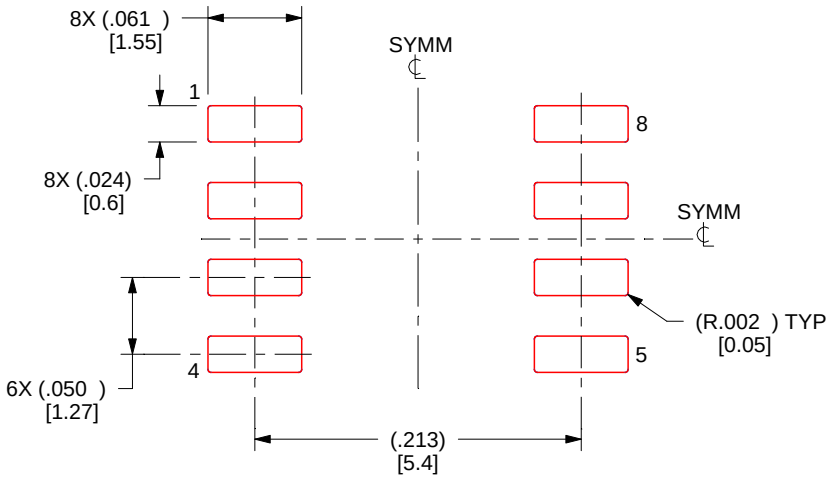
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

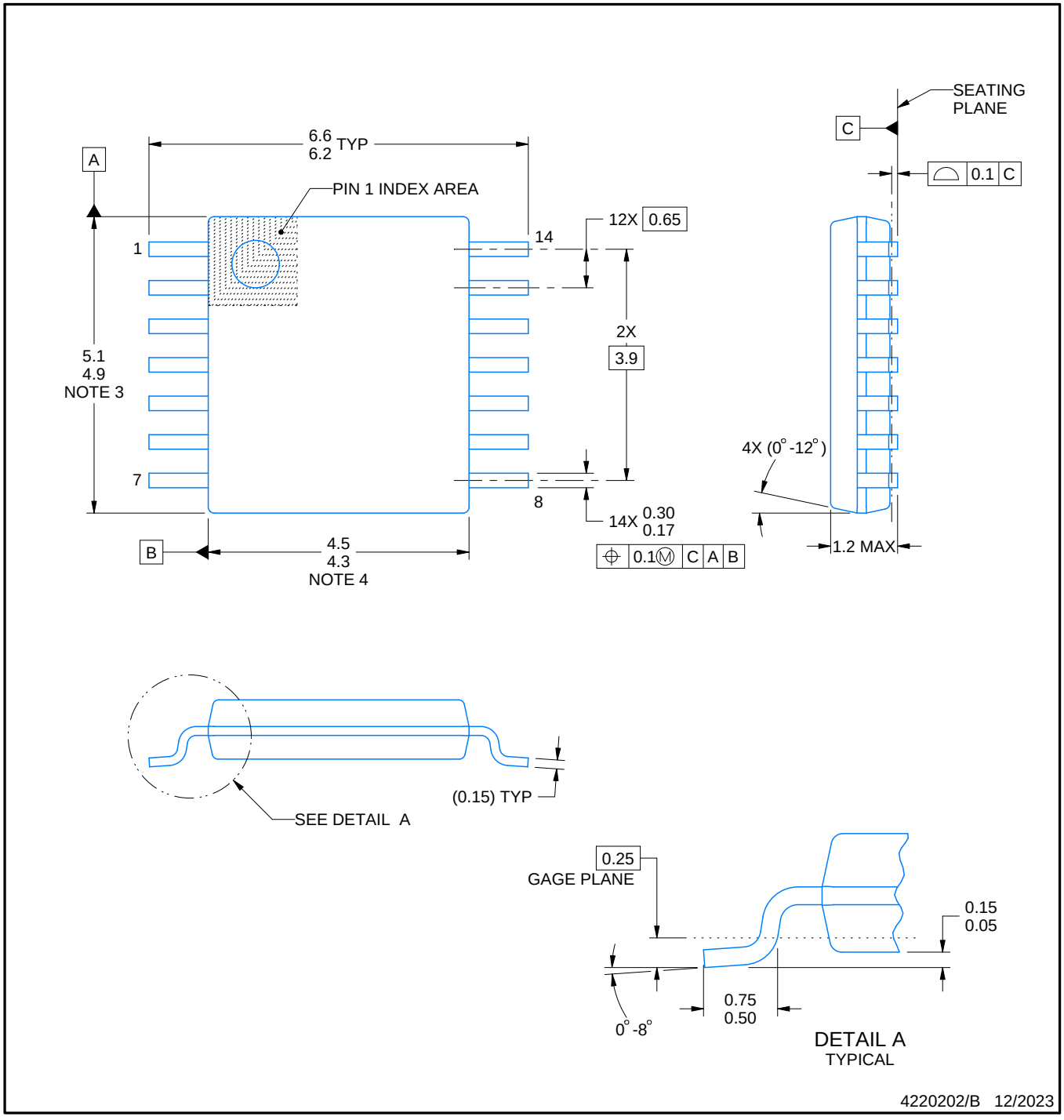
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

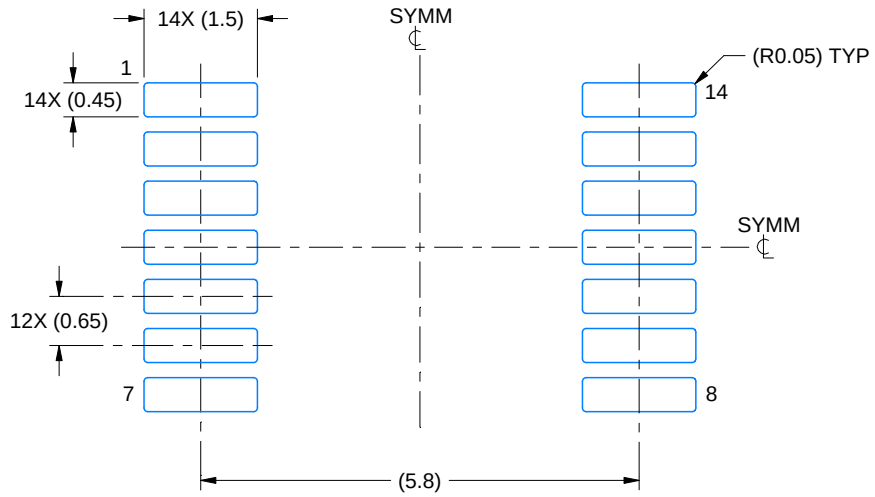
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

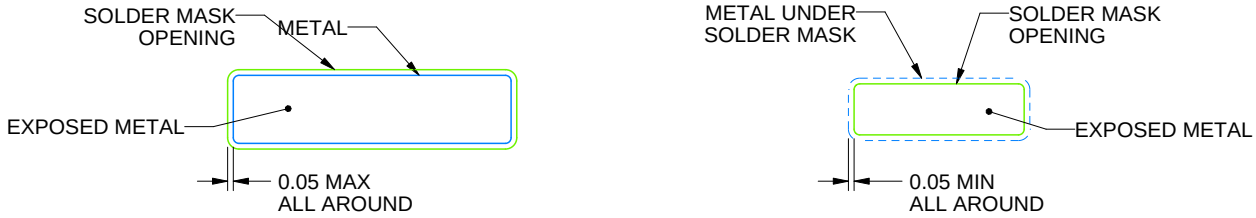


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

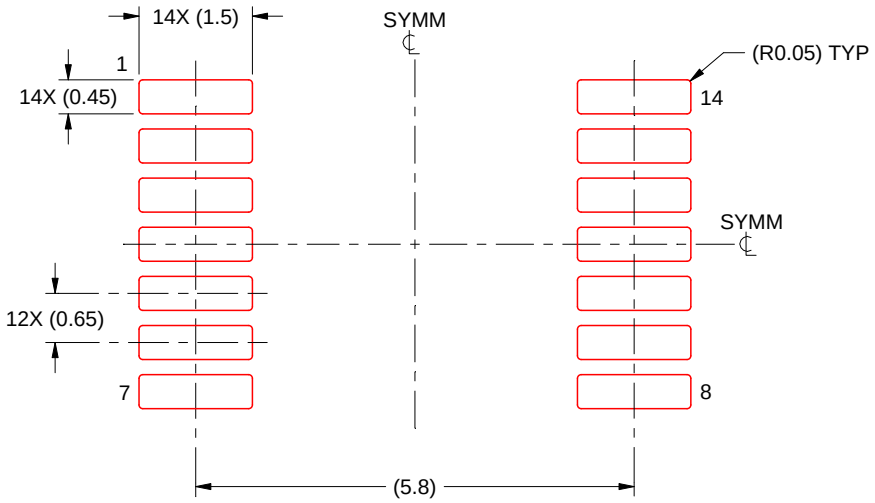


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

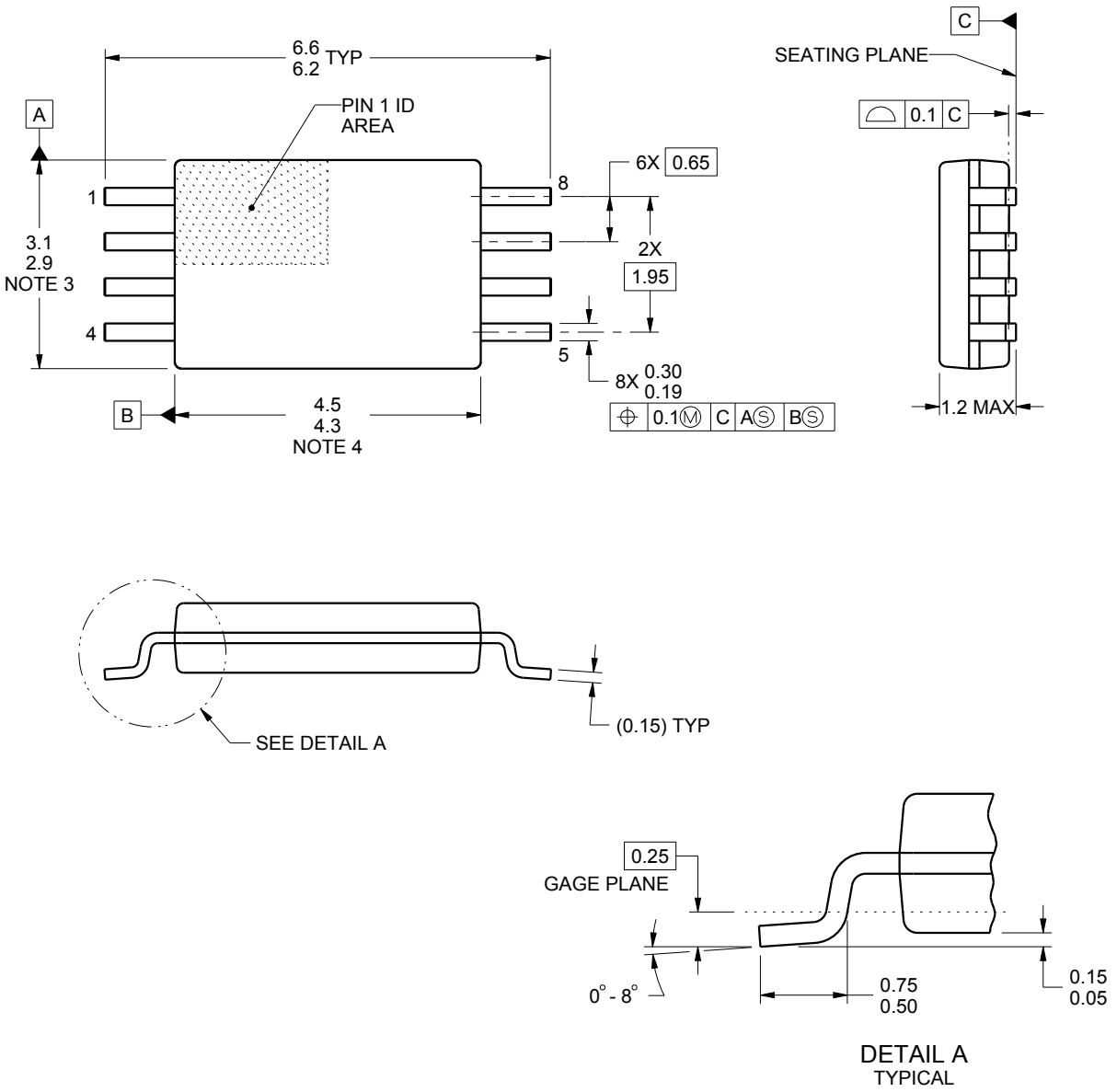
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0008A

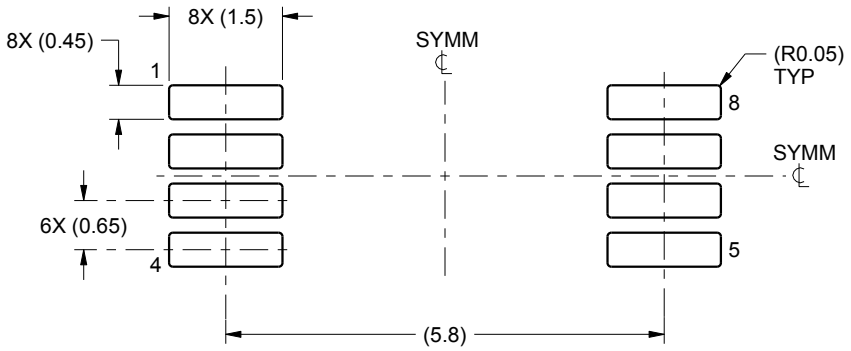
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

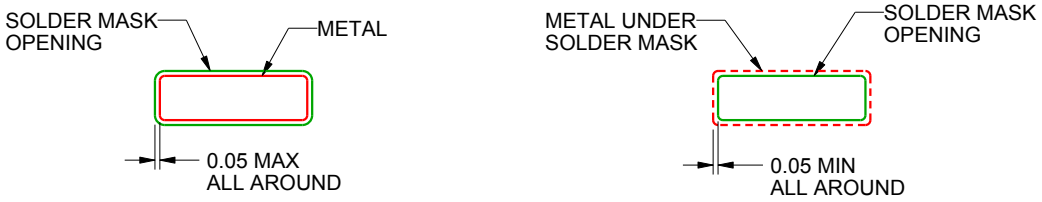


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

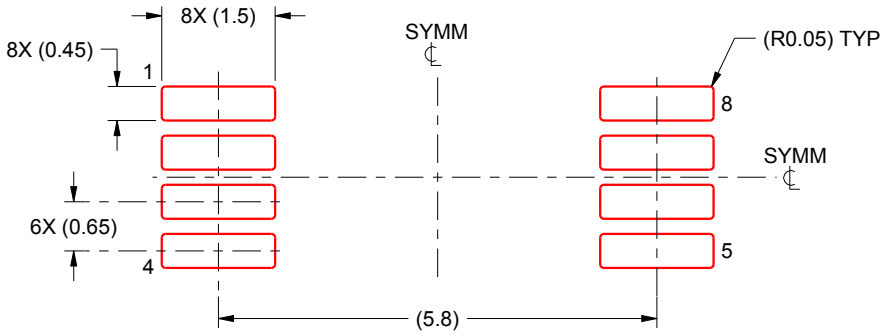


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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