

TLV27x Family of 550- μ A/Ch, 3-MHz, Rail-to-Rail Output Operational Amplifiers

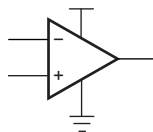
1 Features

- Rail-to-Rail Output
- Wide Bandwidth: 3 MHz
- High Slew Rate: 2.4 V/ μ s
- Supply Voltage Range: 2.7 V to 16 V
- Supply Current: 550 μ A/Channel
- Input Noise Voltage: 39 nV/ $\sqrt{\text{Hz}}$
- Input Bias Current: 1 pA
- Specified Temperature Range:
 - Commercial Grade: 0°C to 70°C
 - Industrial Grade: -40°C to 125°C
- Ultrasmall Packaging:
 - 5-Pin SOT-23 (TLV271)
 - 8-Pin MSOP (TLV272)
- Ideal Upgrade for TLC72x Family

2 Applications

- E-Bike
- Power Banks
- Smoke detectors
- Solar Inverters
- Low-Power Motor Controls
- Battery-Powered Instruments
- Building Automation

Operational Amplifier



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3 Description

Operating from 2.7 V to 16 V over the extended industrial temperature range from -40°C to +125°C, the TLV27x is a low power, wide bandwidth operational amplifier (opamp) with rail to rail output. This makes it an ideal alternative to the TLC27x family for applications where rail-to-rail output swings are essential. The TLV27x provides 3-MHz bandwidth from only 550 μ A.

Like the TLC27x, the TLV27x is fully specified for 5-V and \pm 5-V supplies. The maximum recommended supply voltage is 16 V, which allows the devices to be operated from a variety of rechargeable cells (\pm 8 V supplies down to \pm 1.35 V).

The CMOS inputs enable use in high-impedance sensor interfaces, with the lower voltage operation making an attractive alternative for the TLC27x in battery-powered applications.

All members are available in PDIP and SOIC with the singles in the small SOT-23 package, duals in the MSOP, and quads in the TSSOP package.

The 2.7-V operation makes it compatible with Li-Ion powered systems and the operating supply voltage range of many micropower microcontrollers available today including TI's [MSP430](#).

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|------------|-------------------|
| TLV271 | SOIC (8) | 4.98 mm x 3.91 mm |
| | SOT-23 (5) | 2.90 mm x 1.60 mm |
| | PDIP (8) | 9.81 mm x 6.35 mm |
| TLV272 | SOIC (8) | 4.98 mm x 3.91 mm |
| | PDIP (8) | 9.81 mm x 6.35 mm |
| | VSSOP (8) | 3.00 mm x 3.00 mm |
| TLV274 | SOIC (14) | 8.65 mm x 3.91 mm |
| | PDIP (14) | 3.90 mm x 6.35 mm |
| | TSSOP (14) | 5.00 mm x 4.40 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

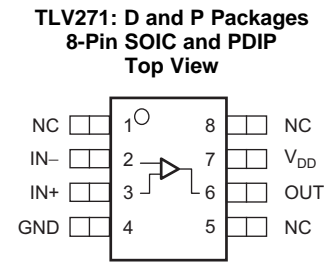
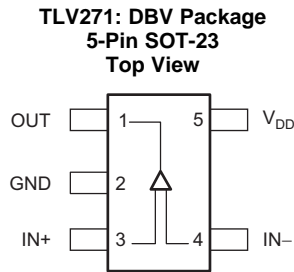
| Changes from Revision D (February 2004) to Revision E | Page |
|--|------|
| • Added <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section | 1 |
| • Deleted <i>Continuous total power dissipation</i> parameter from <i>Absolute Maximum Ratings</i> | 6 |
| • Deleted <i>Dissipation Ratings</i> table | 7 |
| • Deleted <i>Macromodel Information</i> | 21 |

5 Device Comparison Table

| DEVICE ⁽¹⁾ | V _{DD} (V) | V _{IO} (μV) | I _Q /Ch (μA) | I _B (pA) | GBW (MHz) | SR (V/μs) | SHUTDOWN | RAIL-TO-RAIL | SINGLES/ DUALS/ QUADS |
|-----------------------|---------------------|----------------------|-------------------------|---------------------|-----------|-----------|----------|--------------|-----------------------------|
| TLV27x | 2.7 to 16 | 500 | 550 | 1 | 3 | 2.4 | — | O | S/D/Q |
| TLC27x | 3 to 16 | 1100 | 675 | 1 | 1.7 | 3.6 | — | — | S/D/Q |
| TLV237x | 2.7 to 16 | 500 | 550 | 1 | 3 | 2.4 | Yes | I/O | S/D/Q |
| TLC227x | 2.7 to 16 | 300 | 1100 | 1 | 2.2 | 3.6 | — | O | D/Q |
| TLV246x | 2.7 to 6 | 150 | 550 | 1300 | 6.4 | 1.6 | Yes | I/O | S/D/Q |
| TLV247x | 2.7 to 6 | 250 | 600 | 2 | 2.8 | 1.5 | Yes | I/O | S/D/Q |
| TLV244x | 2.7 to 10 | 300 | 725 | 1 | 1.8 | 1.4 | — | O | D/Q |

(1) Typical values measured at 5 V, 25°C.

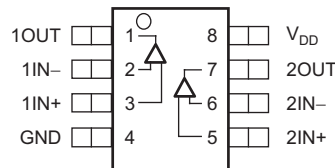
6 Pin Configuration and Functions



Pin Functions

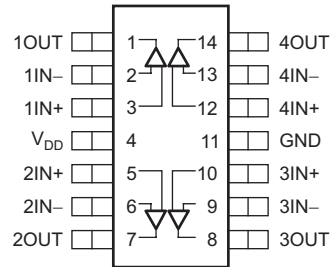
| NAME | PIN | | I/O | DESCRIPTION |
|-----------------|--------|-----------|-----|--|
| | TLV271 | | | |
| | SOT-23 | SOIC PDIP | | |
| GND | 2 | 4 | — | Negative (lowest) supply or ground (for single-supply operation) |
| IN- | 4 | 2 | I | Negative (inverting) input |
| IN+ | 3 | 3 | I | Positive (noninverting) input |
| NC | — | 1, 5, 8 | — | No internal connection (can be left floating) |
| OUT | 1 | 6 | O | Output |
| V _{DD} | 5 | 7 | — | Positive (highest) supply |

**TLV272: D, DGK, and P Packages
8-Pin SOIC, VSSOP, and PDIP
Top View**



Pin Functions

| NAME | PIN | | I/O | DESCRIPTION |
|-----------------|-----------------|---|-----|--|
| | TLV272 | | | |
| | SOIC VSSOP PDIP | | | |
| GND | 4 | — | — | Negative (lowest) supply or ground (for single-supply operation) |
| 1IN- | 2 | I | I | Inverting input, channel 1 |
| 1IN+ | 3 | I | I | Noninverting input, channel 1 |
| 2IN- | 6 | I | I | Inverting input, channel 2 |
| 2IN+ | 5 | I | I | Noninverting input, channel 2 |
| 1OUT | 1 | O | O | Output, channel 1 |
| 2OUT | 7 | O | O | Output, channel 2 |
| V _{DD} | 8 | — | — | Positive (highest) supply |

**TLV274: D, PW, and N Packages
14-Pin SOIC, TSSOP, and PDIP
Top View**

Pin Functions

| PIN | | I/O | DESCRIPTION |
|-----------------|---------------------------------|-----|---|
| NAME | TLV274 SOIC TSSOP PDIP | | |
| GND | 11 | — | Negative supply or ground (for single-supply operation) |
| 1IN– | 2 | I | Inverting input, channel 1 |
| 1IN+ | 3 | I | Noninverting input, channel 1 |
| 2IN– | 6 | I | Inverting input, channel 2 |
| 2IN+ | 5 | I | Noninverting input, channel 2 |
| 3IN– | 9 | I | Inverting input, channel 3 |
| 3IN+ | 10 | I | Noninverting input, channel 3 |
| 4IN– | 13 | I | Inverting input, channel 4 |
| 4IN+ | 12 | I | Noninverting input, channel 4 |
| 1OUT | 1 | O | Output, channel 1 |
| 2OUT | 7 | O | Output, channel 2 |
| 3OUT | 8 | O | Output, channel 3 |
| 4OUT | 14 | O | Output, channel 4 |
| V _{DD} | 4 | — | Positive supply |

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT | |
|-------------|------------------------------|-----------|----------------|------|----|
| Voltage | Supply, V_{DD} | | 16.5 | V | |
| | Differential input, V_{ID} | $-V_{DD}$ | V_{DD} | V | |
| | Input, V_I | -0.2 | $V_{DD} + 0.2$ | V | |
| Current | Input, I_I | -10 | 10 | mA | |
| | Output, I_O | -100 | 100 | mA | |
| Temperature | Operating, T_A | C-suffix | 0 | 70 | °C |
| | | I-suffix | -40 | 125 | °C |
| | Junction, T_J | | 150 | °C | |
| | Storage, T_{stg} | -65 | 150 | °C | |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values, except differential voltages, are with respect to GND.

7.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---------------------------------------|---------------|------------|-----|-----------------|------|
| Supply voltage, V_{DD} | Single-supply | 2.7 | | 16 | V |
| | Split-supply | ± 1.35 | | ± 8 | |
| Common-mode input voltage, V_{ICR} | | 0 | | $V_{DD} - 1.35$ | V |
| Operating free-air temperature, T_A | C-suffix | 0 | | 70 | °C |
| | I-suffix | -40 | | 125 | |

7.3 Thermal Information: TLV271

| THERMAL METRIC ⁽¹⁾ | | TLV271 | | | UNIT |
|-------------------------------|--|-------------|-----------------|-------------|------|
| | | D (SOIC) | DBV (SOT-23) | P (PDIP) | |
| | | 8 PINS | 5 PINS | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 127.2 | 221.7 | 49.2 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 71.6 | 144.7 | 39.4 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 68.2 | 49.7 | 26.4 | °C/W |
| Ψ_{JT} | Junction-to-top characterization parameter | 22 | 26.1 | 15.4 | °C/W |
| Ψ_{JB} | Junction-to-board characterization parameter | 67.6 | 49 | 26.3 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | n/a | n/a | n/a | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.4 Thermal Information: TLV272

| THERMAL METRIC ⁽¹⁾ | | TLV272 | | | UNIT |
|-------------------------------|--|-------------|----------------|-------------|------|
| | | D (SOIC) | DGK (VSSOP) | P (PDIP) | |
| | | 8 PINS | 8 PINS | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 127.2 | 186.6 | 49.2 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 71.6 | 78.8 | 39.4 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 68.2 | 107.9 | 26.4 | °C/W |
| Ψ_{JT} | Junction-to-top characterization parameter | 22 | 15.5 | 15.4 | °C/W |
| Ψ_{JB} | Junction-to-board characterization parameter | 67.6 | 106.3 | 26.3 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | n/a | n/a | n/a | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Thermal Information: TLV274

| THERMAL METRIC ⁽¹⁾ | | TLV274 | | | UNIT |
|-------------------------------|--|-------------|-------------|---------------|------|
| | | D (SOIC) | N (PDIP) | PW (TSSOP) | |
| | | 14 PINS | 14 PINS | 14 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 97 | 66.3 | 135 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 56 | 20.5 | 45 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 53 | 26.8 | 66 | °C/W |
| Ψ_{JT} | Junction-to-top characterization parameter | 19 | 2.1 | n/a | °C/W |
| Ψ_{JB} | Junction-to-board characterization parameter | 46 | 26.2 | 60 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | n/a | n/a | n/a | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.6 Electrical Characteristics: DC Characteristics

 at specified free-air temperature, $V_{DD} = 2.7\text{ V}$, 5 V , and $\pm 5\text{ V}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $T_A^{(1)}$ | MIN | TYP | MAX | UNIT |
|-----------------|---|---|---------------------------|-------------|-----|-----|-----|------------------------------|
| V_{IO} | Input offset voltage | $V_{IC} = V_{DD}/2$, $R_L = 10\text{ k}\Omega$, $V_O = V_{DD}/2$, $R_S = 50\ \Omega$ | | 25°C | | 0.5 | 5 | mV |
| | | | | Full range | | | 7 | |
| αV_{IO} | Offset voltage drift | | | 25°C | | 2 | | $\mu\text{V}/^\circ\text{C}$ |
| CMRR | Common-mode rejection ratio | $V_{IC} = 0\text{ to }V_{DD} - 1.35\text{ V}$, $R_S = 50\ \Omega$ | $V_{DD} = 2.7\text{ V}$ | 25°C | 58 | 70 | dB | |
| | | | | Full range | 55 | | | |
| | | $V_{DD} = 5\text{ V}$ | 25°C | 65 | 80 | | | |
| | | | Full range | 62 | | | | |
| | | $V_{DD} = \pm 5\text{ V}$ | 25°C | 69 | 85 | | | |
| | | | Full range | 66 | | | | |
| A_{VD} | Large-signal differential voltage amplification | $V_{O(PP)} = V_{DD}/2$, $R_L = 10\text{ k}\Omega$ | $V_{DD} = 2.7\text{ V}$ | 25°C | 97 | 106 | dB | |
| | | | | Full range | 76 | | | |
| | | | $V_{DD} = 5\text{ V}$ | 25°C | 100 | 110 | | |
| | | | | Full range | 86 | | | |
| | | | $V_{DD} = \pm 5\text{ V}$ | 25°C | 100 | 115 | | |
| | | | | Full range | 90 | | | |

(1) Full range is 0°C to 70°C for C-suffix and full range is –40°C to 125°C for I-suffix. If not specified, full range is –40°C to 125°C.

7.7 Electrical Characteristics: Input Characteristics

 at specified free-air temperature, $V_{DD} = 2.7\text{ V}$, 5 V , and $\pm 5\text{ V}$ (unless otherwise noted).

| PARAMETER | TEST CONDITIONS | T_A | MIN | TYP | MAX | UNIT |
|------------|--|---------------------|-----|------|------|------------|
| I_{IO} | $V_{DD} = 5\text{ V}$, $V_{IC} = V_{DD}/2$, $V_O = V_{DD}/2$, $R_S = 50\ \Omega$ | 25°C | | 1 | 60 | pA |
| | | 70°C | | | 100 | |
| | | 125°C | | | 1000 | |
| I_{IB} | $V_{DD} = 5\text{ V}$, $V_{IC} = V_{DD}/2$, $V_O = V_{DD}/2$, $R_S = 50\ \Omega$ | 25°C | | 1 | 60 | pA |
| | | 70°C | | | 100 | |
| | | 125°C | | | 1000 | |
| $r_{i(d)}$ | Differential input resistance | 25°C | | 1000 | | G Ω |
| C_{IC} | Common-mode input capacitance | $f = 21\text{ kHz}$ | | 8 | | pF |

7.8 Electrical Characteristics: Output Characteristics

 at specified free-air temperature, $V_{DD} = 2.7\text{ V}$, 5 V , and $\pm 5\text{ V}$ (unless otherwise noted).

| PARAMETER | TEST CONDITIONS | | T_A | MIN | TYP | MAX | UNIT |
|------------------------------------|--|---------------------------|------------|------|-------|-------|------|
| V_{OH} High-level output voltage | $V_{IC} = V_{DD}/2$, $I_{OH} = -1\text{ mA}$ | $V_{DD} = 2.7\text{ V}$ | 25°C | 2.55 | 2.58 | | V |
| | | | Full range | 2.48 | | | |
| | | $V_{DD} = 5\text{ V}$ | 25°C | 4.9 | 4.93 | | |
| | | | Full range | 4.85 | | | |
| | | $V_{DD} = \pm 5\text{ V}$ | 25°C | 4.92 | 4.96 | | |
| | | | Full range | 4.9 | | | |
| | $V_{IC} = V_{DD}/2$, $I_{OH} = -5\text{ mA}$ | $V_{DD} = 2.7\text{ V}$ | 25°C | 1.9 | 2.1 | | |
| | | | Full range | 1.5 | | | |
| | | $V_{DD} = 5\text{ V}$ | 25°C | 4.6 | 4.68 | | |
| | | | Full range | 4.5 | | | |
| | | $V_{DD} = \pm 5\text{ V}$ | 25°C | 4.7 | 4.84 | | |
| | | | Full range | 4.65 | | | |
| V_{OL} Low-level output voltage | $V_{IC} = V_{DD}/2$, $I_{OH} = 1\text{ mA}$ | $V_{DD} = 2.7\text{ V}$ | 25°C | | 0.1 | 0.15 | V |
| | | | Full range | | | 0.22 | |
| | | $V_{DD} = 5\text{ V}$ | 25°C | | 0.05 | 0.1 | |
| | | | Full range | | | 0.15 | |
| | | $V_{DD} = \pm 5\text{ V}$ | 25°C | | -4.95 | -4.92 | |
| | | | Full range | | | -4.9 | |
| | $V_{IC} = V_{DD}/2$, $I_{OH} = 5\text{ mA}$ | $V_{DD} = 2.7\text{ V}$ | 25°C | | 0.5 | 0.7 | |
| | | | Full range | | | 1.1 | |
| | | $V_{DD} = 5\text{ V}$ | 25°C | | 0.28 | 0.4 | |
| | | | Full range | | | 0.5 | |
| | | $V_{DD} = \pm 5\text{ V}$ | 25°C | | -4.84 | -4.7 | |
| | | | Full range | | | -4.65 | |
| I_O Output current | $V_O = 0.5\text{ V}$ from rail, $V_{DD} = 2.7\text{ V}$ | Positive rail | 25°C | | 4 | mA | |
| | | Negative rail | 25°C | | 5 | | |
| | $V_O = 0.5\text{ V}$ from rail, $V_{DD} = 5\text{ V}$ | Positive rail | 25°C | | 7 | | |
| | | Negative rail | 25°C | | 8 | | |
| | $V_O = 0.5\text{ V}$ from rail, $V_{DD} = 10\text{ V}$ | Positive rail | 25°C | | 13 | | |
| | | Negative rail | 25°C | | 12 | | |

7.9 Electrical Characteristics: Power Supply

 at specified free-air temperature, $V_{DD} = 2.7\text{ V}$, 5 V , and $\pm 5\text{ V}$ (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | | $T_A^{(1)}$ | MIN | TYP | MAX | UNIT |
|-----------|--|--|-------------------------|-------------|-----|-----|------|---------------|
| I_{DD} | Supply current (per channel) | $V_O = V_{DD}/2$ | $V_{DD} = 2.7\text{ V}$ | 25°C | | 470 | 560 | μA |
| | | | $V_{DD} = 5\text{ V}$ | 25°C | | 550 | 660 | |
| | | | $V_{DD} = 10\text{ V}$ | 25°C | | 625 | 800 | |
| | | | Full range | | | | 1000 | |
| PSRR | Supply voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$) | $V_{DD} = 2.7\text{ V}$ to 16 V , $V_{IC} = V_{DD}/2$, no load | | 25°C | 70 | 80 | | dB |
| | | | | Full range | 65 | | | |

(1) Full range is 0°C to 70°C for C-suffix and full range is –40°C to 125°C for I-suffix. If not specified, full range is –40°C to 125°C.

7.10 Electrical Characteristics: Dynamic Performance

over operating free-air temperature range (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | | $T_A^{(1)}$ | MIN | TYP | MAX | UNIT |
|-----------|-------------------------|---|--|-------------|------|-----|-----|------------------------|
| UGBW | Unity-gain bandwidth | $R_L = 2\text{ k}\Omega$, $C_L = 10\text{ pF}$ | $V_{DD} = 2.7\text{ V}$ | 25°C | | 2.4 | | MHz |
| | | | $V_{DD} = 5\text{ V}$ to 10 V | 25°C | | 3 | | |
| SR | Slew rate at unity gain | $V_{O(PP)} = V_{DD}/2$, $C_L = 50\text{ pF}$, $R_L = 10\text{ k}\Omega$ | $V_{DD} = 2.7\text{ V}$ | 25°C | 1.35 | 2.1 | | $\text{V}/\mu\text{s}$ |
| | | | | Full range | 1 | | | |
| | | | $V_{DD} = 5\text{ V}$ | 25°C | 1.45 | 2.4 | | $\text{V}/\mu\text{s}$ |
| | | | | Full range | 1.2 | | | |
| | | | $V_{DD} = \pm 5\text{ V}$ | 25°C | 1.8 | 2.6 | | $\text{V}/\mu\text{s}$ |
| | | | | Full range | 1.3 | | | |
| ϕ_m | Phase margin | $R_L = 2\text{ k}\Omega$ | $C_L = 10\text{ pF}$ | 25°C | | 65 | | ° |
| | Gain margin | $R_L = 2\text{ k}\Omega$ | $C_L = 10\text{ pF}$ | 25°C | | 18 | | dB |
| t_s | Setting time | $V_{DD} = 2.7\text{ V}$, $V_{(STEP)PP} = 1\text{ V}$, $A_V = -1$, $C_L = 10\text{ pF}$, $R_L = 2\text{ k}\Omega$ | 0.1% | 25°C | | 2.9 | | μs |
| | | | 0.1% | | | 2 | | |
| | | $V_{DD} = 5\text{ V}$, $\pm 5\text{ V}$, $V_{(STEP)PP} = 1\text{ V}$, $A_V = -1$, $C_L = 47\text{ pF}$, $R_L = 2\text{ k}\Omega$ | 0.1% | | | | | |

(1) Full range is 0°C to 70°C for C suffix and full range is –40°C to 125°C for I suffix. If not specified, full range is –40°C to 125°C.

7.11 Electrical Characteristics: Noise/Distortion Performance

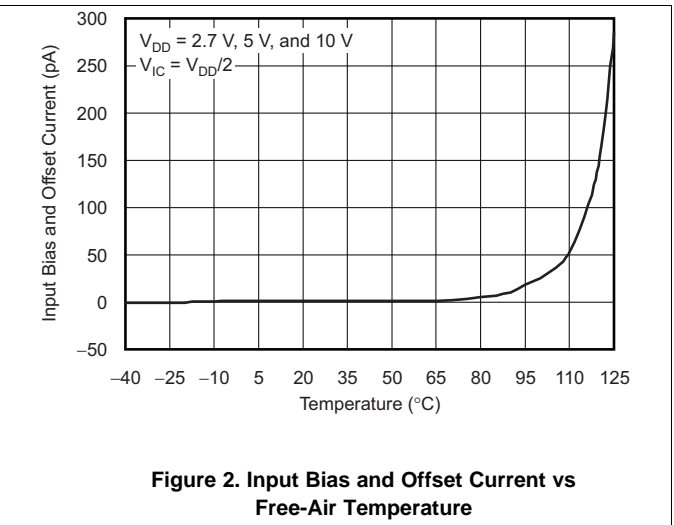
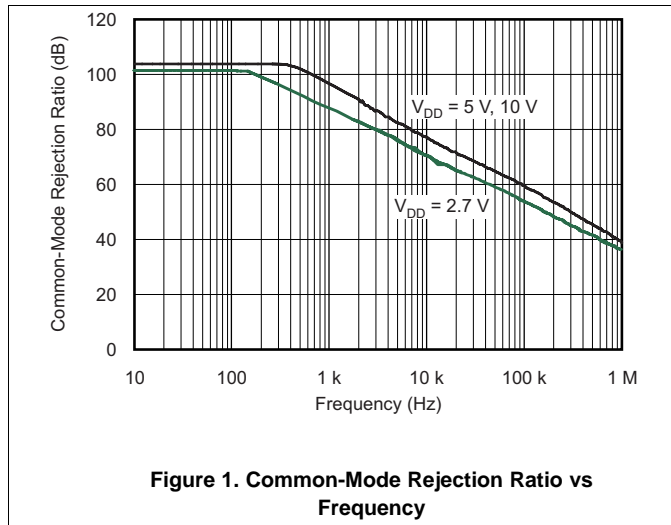
over operating free-air temperature range (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | | T_A | MIN | TYP | MAX | UNIT |
|-----------|--------------------------------------|---|-------------|-------|-----|-------|------------------------------|------|
| THD + N | Total harmonic distortion plus noise | $V_{DD} = 2.7\text{ V}$, $V_{O(PP)} = V_{DD}/2\text{ V}$, $R_L = 2\text{ k}\Omega$, $f = 10\text{ kHz}$ | $A_V = 1$ | 25°C | | 0.02% | | |
| | | | $A_V = 10$ | | | 0.05% | | |
| | | | $A_V = 100$ | | | 0.18% | | |
| | | $V_{DD} = 5\text{ V}$, $\pm 5\text{ V}$, $V_{O(PP)} = V_{DD}/2\text{ V}$, $R_L = 2\text{ k}\Omega$, $f = 10\text{ kHz}$ | $A_V = 1$ | 25°C | | 0.02% | | |
| | | | $A_V = 10$ | | | 0.09% | | |
| | | | $A_V = 100$ | | | 0.5% | | |
| V_n | Equivalent input noise voltage | $f = 1\text{ kHz}$ | 25°C | | 39 | | $\text{nV}/\sqrt{\text{Hz}}$ | |
| | | $f = 10\text{ kHz}$ | | | 35 | | | |
| I_n | Equivalent input noise current | $f = 1\text{ kHz}$ | 25°C | | 0.6 | | $\text{fA}/\sqrt{\text{Hz}}$ | |

7.12 Typical Characteristics

Table 1. Table of Graphs

| DESCRIPTION | | FIGURE NO. |
|-------------|--|------------------------------|
| CMRR | Common-mode rejection ratio | vs Frequency |
| | Input bias and offset current | vs Free-air temperature |
| V_{OL} | Low-level output voltage | vs Low-level output current |
| V_{OH} | High-level output voltage | vs High-level output current |
| $V_{O(PP)}$ | Peak-to-peak output voltage | vs Frequency |
| I_{DD} | Supply current | vs Supply voltage |
| PSRR | Power-supply rejection ratio | vs Frequency |
| A_{VD} | Differential voltage gain and phase | vs Frequency |
| | Gain-bandwidth product | vs Free-air temperature |
| SR | Slew rate | vs Supply voltage |
| | | vs Free-air temperature |
| ϕ_m | Phase margin | vs Capacitive load |
| V_n | Equivalent input noise voltage | vs Frequency |
| | Voltage-follower large-signal pulse response | |
| | Voltage-follower small-signal pulse response | |
| | Inverting large-signal response | |
| | Inverting small-signal response | |
| | Crosstalk | vs Frequency |



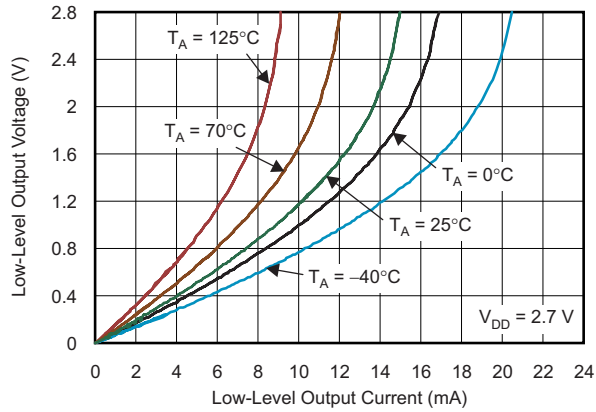


Figure 3. Low-Level Output Voltage vs Low-Level Output Current

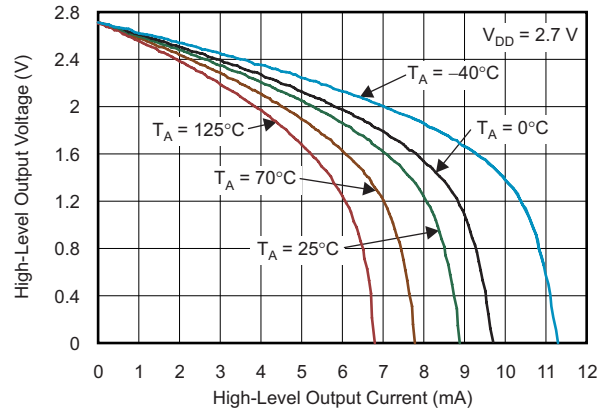


Figure 4. High-Level Output Voltage vs High-Level Output Current

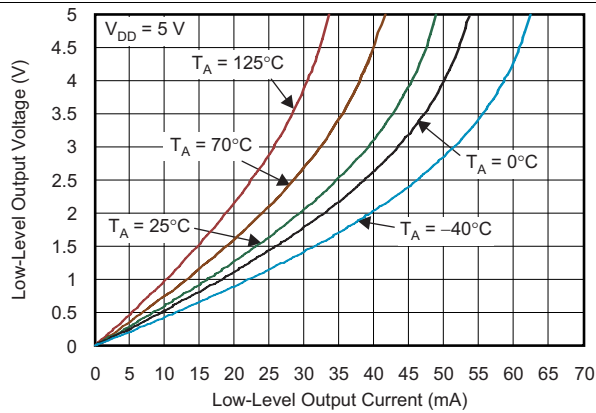


Figure 5. Low-Level Output Voltage vs Low-Level Output Current

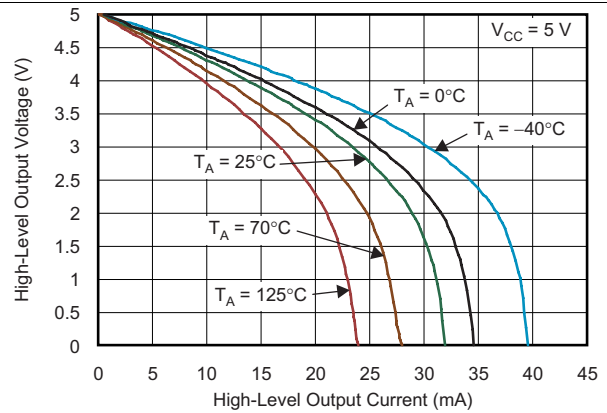


Figure 6. High-Level Output Voltage vs High-Level Output Current

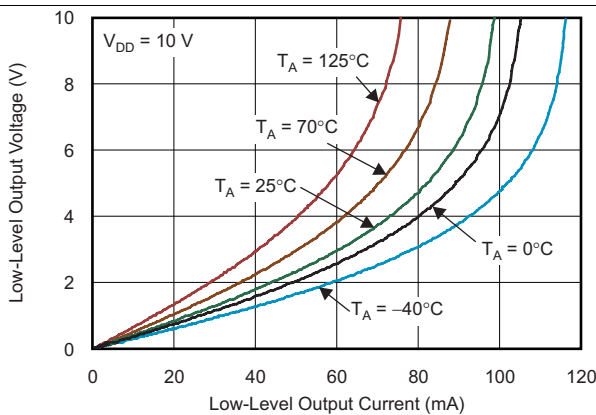


Figure 7. Low-Level Output Voltage vs Low-Level Output Current

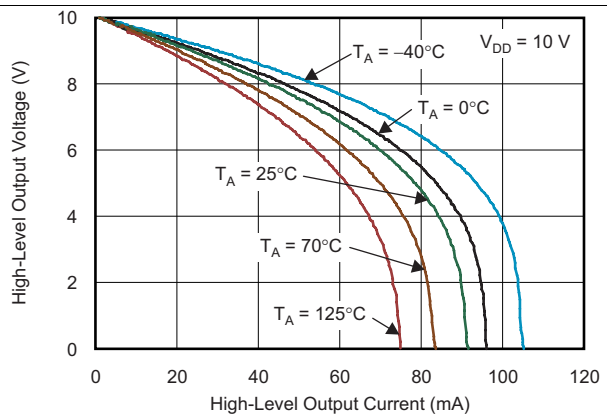


Figure 8. High-Level Output Voltage vs High-Level Output Current

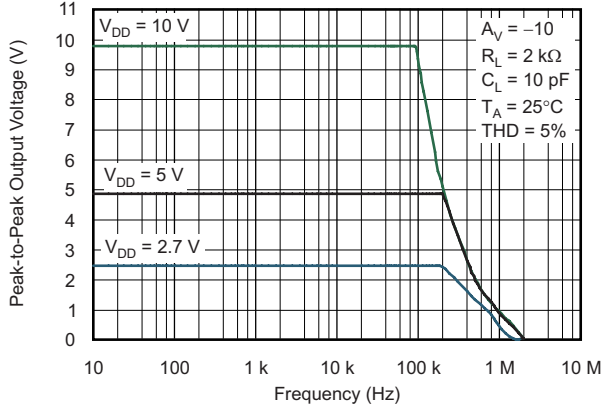


Figure 9. Peak-to-Peak Output Voltage vs Frequency

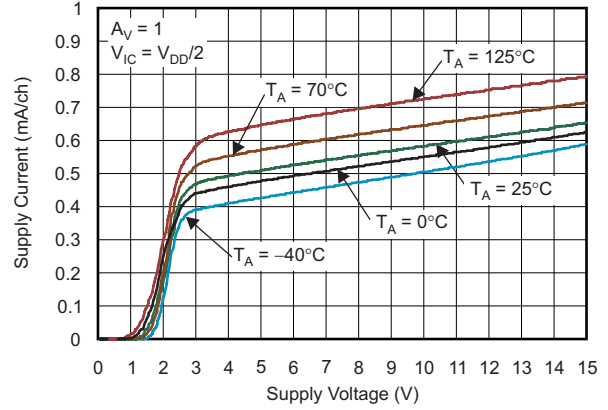


Figure 10. Supply Current vs Supply Voltage

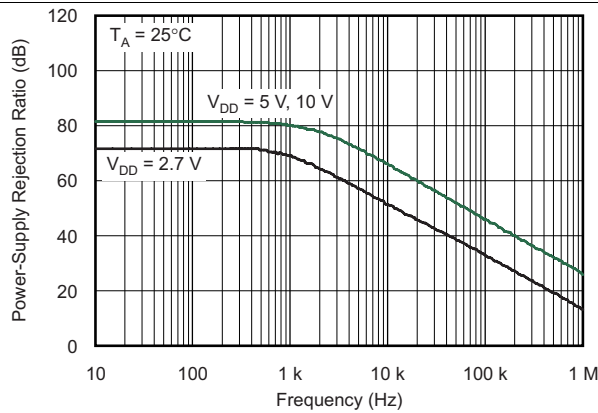


Figure 11. Power-Supply Rejection Ratio vs Frequency

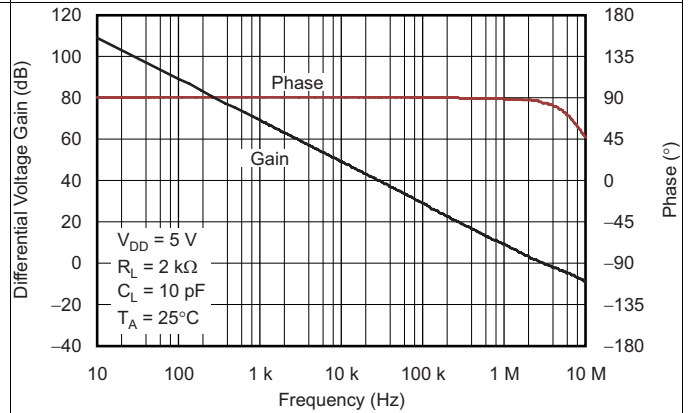


Figure 12. Differential Voltage Gain and Phase

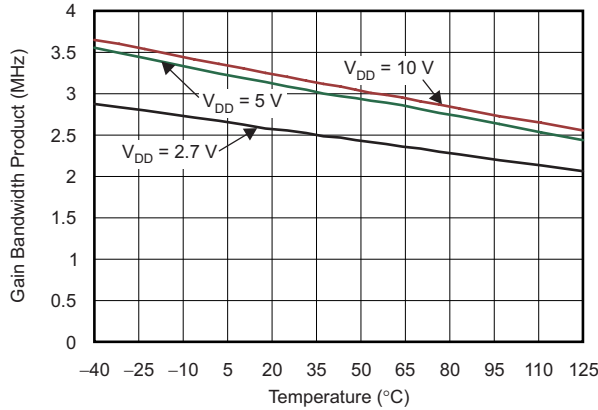


Figure 13. Gain Bandwidth Product vs Free-Air Temperature

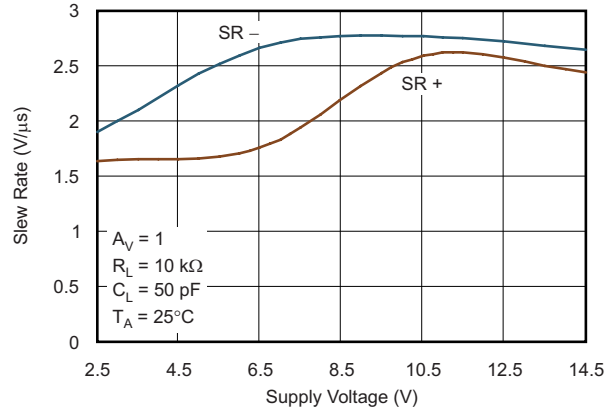


Figure 14. Slew Rate vs Supply Voltage

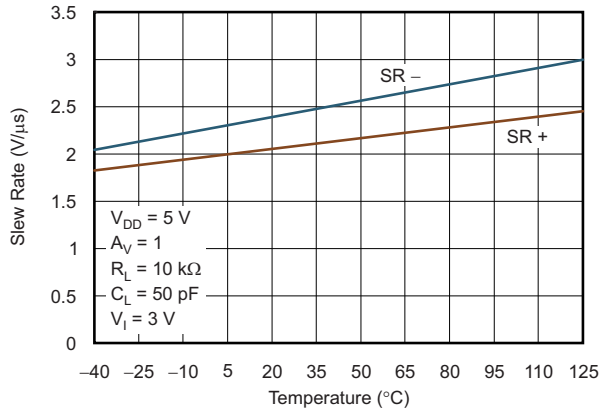


Figure 15. Slew Rate vs Free-Air Temperature

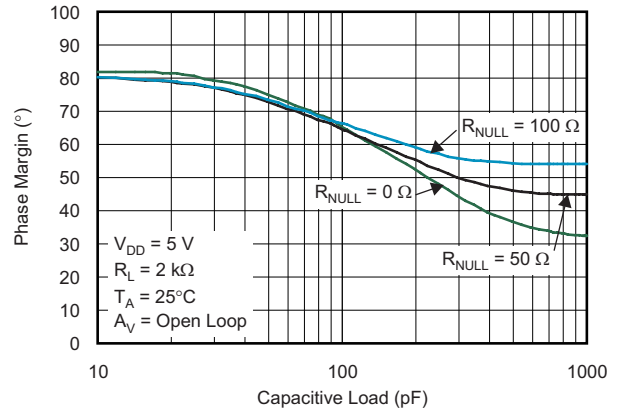


Figure 16. Phase Margin vs Capacitive Load

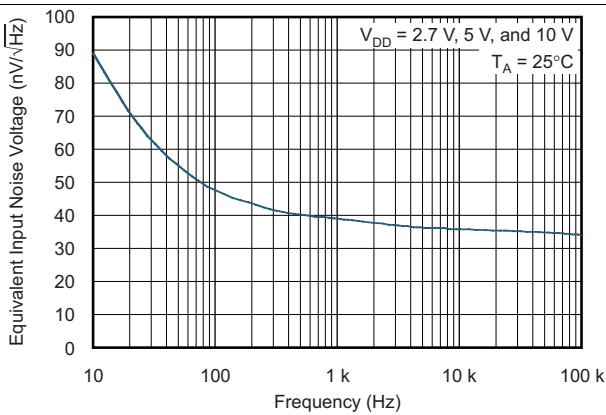


Figure 17. Equivalent Input Noise Voltage vs Frequency

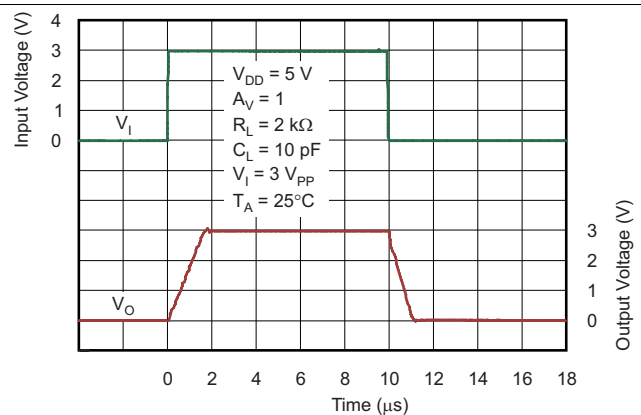


Figure 18. Voltage-Follower Large-Signal Pulse Response

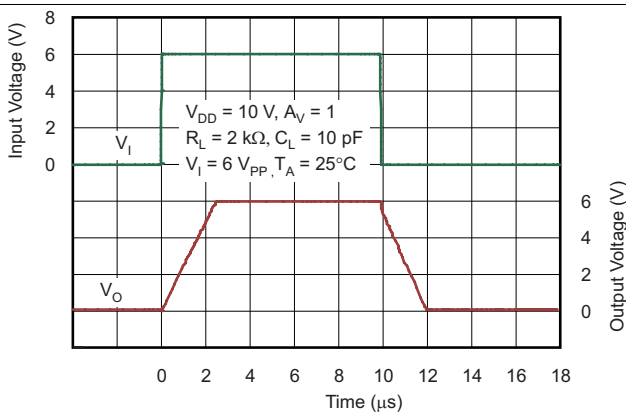


Figure 19. Voltage-Follower Large-Signal Pulse Response

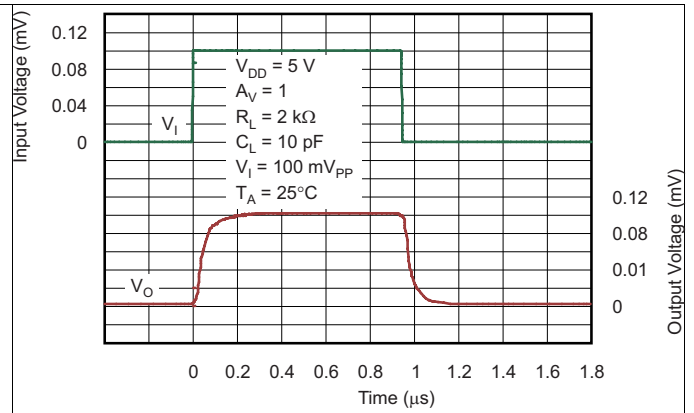
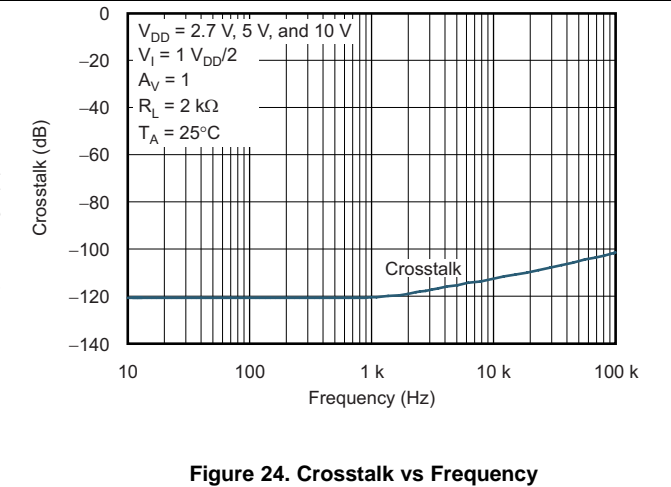
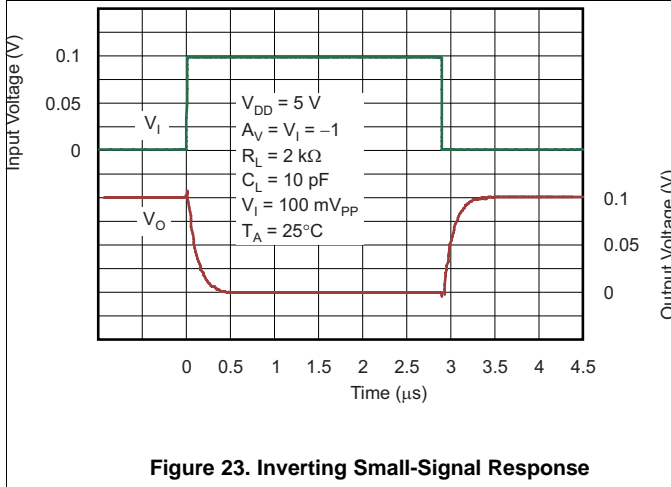
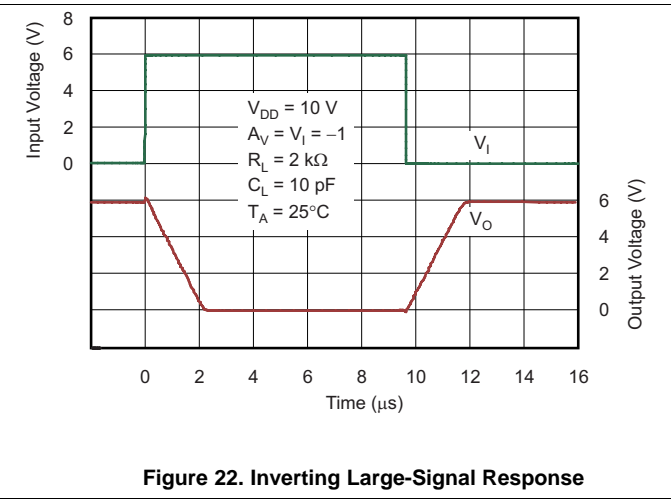
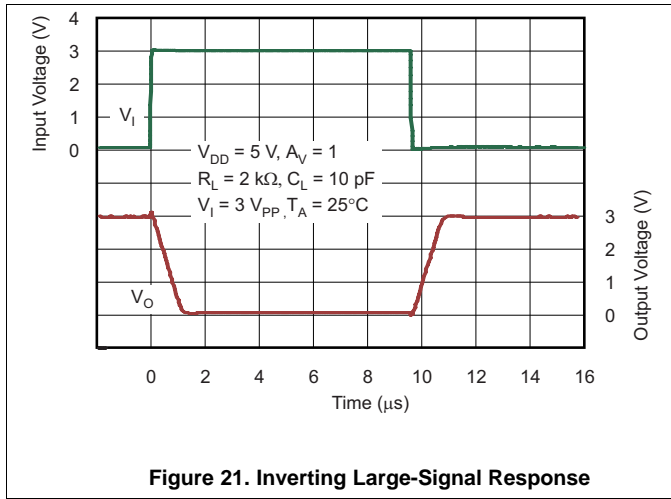


Figure 20. Voltage-Follower Small-Signal Pulse Response

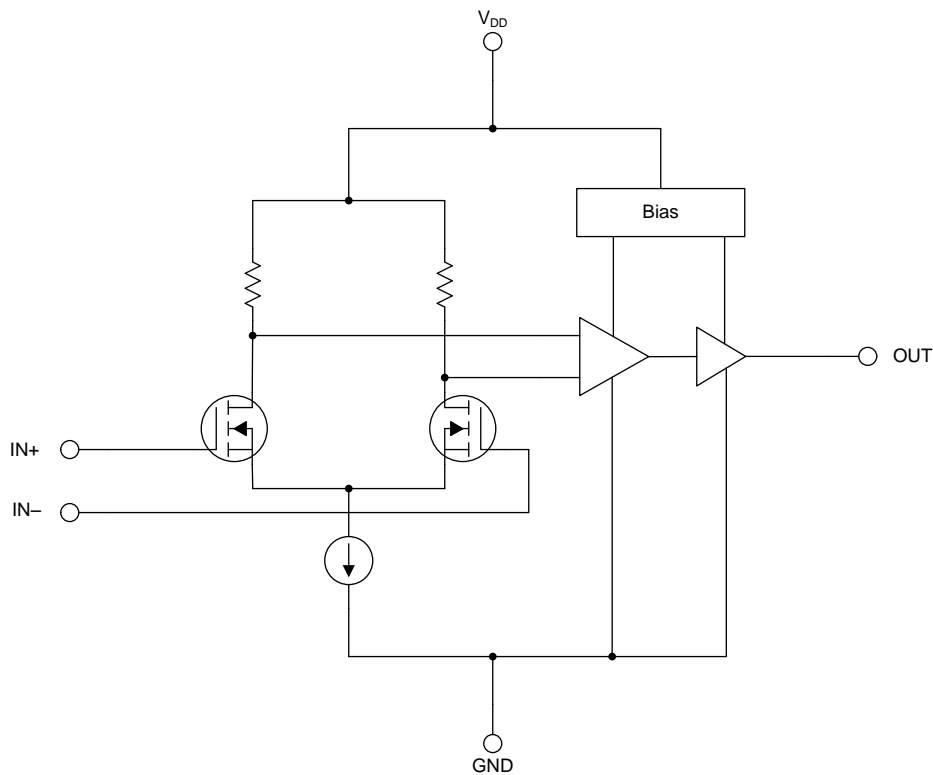


8 Detailed Description

8.1 Overview

The TLV27x operates from a single power supply and consumes only 550 μA of quiescent current. With rail-to-rail output swing capability and 3-MHz bandwidth, the TLV27x is ideal for battery-powered and industrial applications.

8.2 Functional Block Diagram



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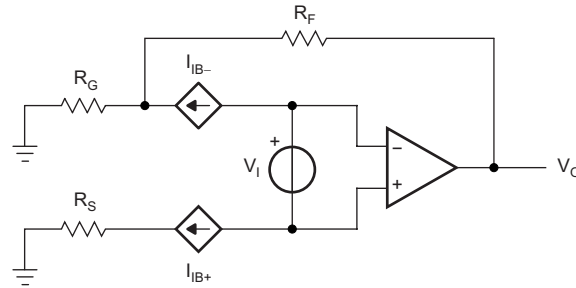
8.3 Feature Description

8.3.1 Rail to Rail Output

The TLV27x family of opamps features a rail to rail output stage. Rail to rail outputs allow for a wide dynamic range in low voltage systems. This feature along with low power and wide bandwidth make the TLV27x family suitable for portable and battery powered systems.

8.3.2 Offset Voltage

The output offset voltage (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. Use the schematic in [Figure 25](#) and [Equation 1](#) to calculate the output offset voltage:



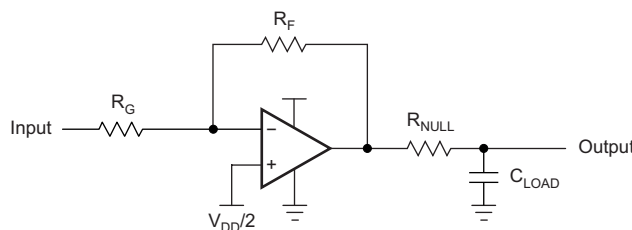
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Figure 25. Output Offset Voltage Model

$$V_{OO} = V_{IO} \left[1 + \left(\frac{R_F}{R_G} \right) \right] \pm I_{IB+} R_S \left[1 + \left(\frac{R_F}{R_G} \right) \right] \pm I_{IB-} R_F \quad (1)$$

8.3.3 Driving a Capacitive Load

When the amplifier is configured in this manner, capacitive loading directly on the output decreases the device phase margin, leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, TI recommends placing a resistor in series (R_{NULL}) with the output of the amplifier, as shown in [Figure 26](#). A minimum value of 20 Ω should work well for most applications.



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Figure 26. Driving a Capacitive Load

8.4 Device Functional Modes

The TLV27x has a single functional mode. It is operational when the power supply applied to the device is between 2.7 V (± 1.35 V) and 16 V (± 8 V). Electrical parameters that can vary with operating conditions are shown in [Typical Characteristics](#).

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TLV27x family offers outstanding DC and AC performance. These devices operate up to a 16-V power supply and offer ultra-low input bias current and 3-MHz bandwidth. These features make the TLV27x a robust operational amplifier for battery-powered and industrial applications.

9.2 Typical Application

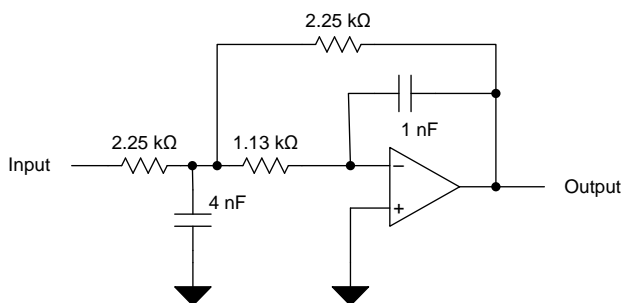


Figure 27. Second-Order, Low-Pass Filter

9.2.1 Design Requirements

- Gain = 1 V/V
- Low-pass cutoff frequency = 50 kHz
- –40-dB/dec filter response
- Maintain less than 3-dB gain peaking in the gain versus frequency response

9.2.2 Detailed Design Procedure

The infinite-gain multiple-feedback circuit for a low-pass network function is shown in [Figure 27](#). Use [Equation 2](#) to calculate the voltage transfer function.

$$\frac{\text{Output}}{\text{Input}}(s) = \frac{-1/R_1 R_3 C_2 C_5}{s^2 + (s/C_2)(1/R_1 + 1/R_3 + 1/R_4) + 1/R_3 R_4 C_2 C_5} \quad (2)$$

This circuit produces a signal inversion. For this circuit, the gain at DC and the low-pass cutoff frequency are calculated by [Equation 3](#):

$$\text{Gain} = \frac{R_4}{R_1}$$

$$f_c = \frac{1}{2\pi} \sqrt{(1/R_3 R_4 C_2 C_5)} \quad (3)$$

Typical Application (continued)

Software tools are readily available to simplify filter design. WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The [WEBENCH® Filter Designer](#) lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web-based tool from the WEBENCH Design Center, WEBENCH Filter Designer allows you to design, optimize, and simulate complete multistage active filter solutions within minutes.

9.2.3 Application Curve

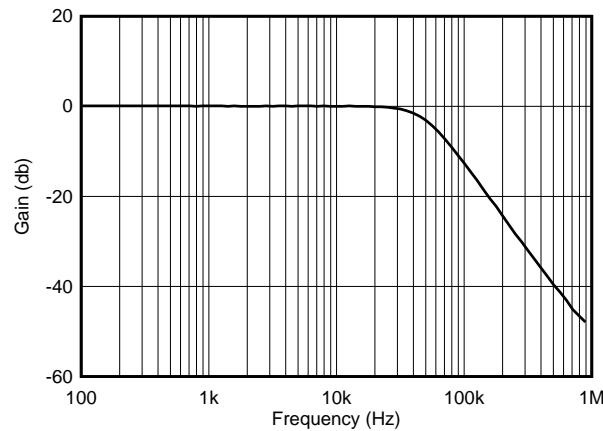
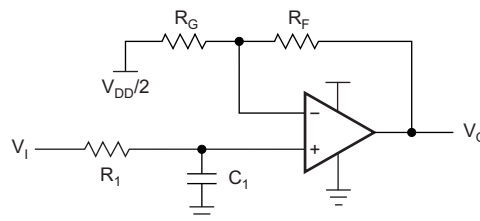


Figure 28. TLV27x Second-Order, 50-kHz, Low-Pass Filter

9.3 System Examples

9.3.1 General Configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this limiting is to place an RC filter at the noninverting terminal of the amplifier (see [Figure 29](#) and [Equation 4](#)).



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Figure 29. Single-Pole Low-Pass Filter

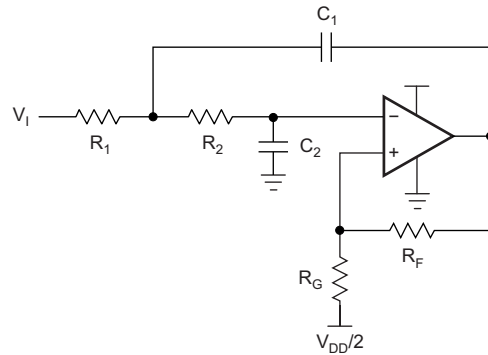
$$\frac{V_O}{V_I} = \left(1 + \frac{R_F}{R_G}\right) \left(\frac{1}{1 + sR_1C_1}\right)$$

$$f_{-3db} = \frac{1}{2\pi R_1 C_1}$$

(4)

System Examples (continued)

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter, shown in [Figure 30](#), can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth; refer to [Equation 5](#). Failure to use an amplifier with this characteristic can result in phase shift of the amplifier.



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Figure 30. Two-Pole, Low-Pass, Sallen-Key Filter

$R_1 = R_2 = R$
 $C_1 = C_2 = C$
 $Q = \text{Peaking Factor}$
 (Butterworth $Q = 0.707$)

$$f_{-3\text{db}} = \frac{1}{2\pi RC}$$

$$R_G = \frac{R_F}{\left(2 - \frac{1}{Q}\right)}$$

(5)

10 Power Supply Recommendations

The TLV27x is specified for operation from 2.7 V to 16 V (± 1.35 V to ± 8 V); many specifications apply from -40°C to 125°C . Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the [Typical Characteristics](#).

CAUTION

Supply voltages larger than 16.5 V can permanently damage the device; see the [Absolute Maximum Ratings](#).

Place 0.1- μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see [Layout Guidelines](#).

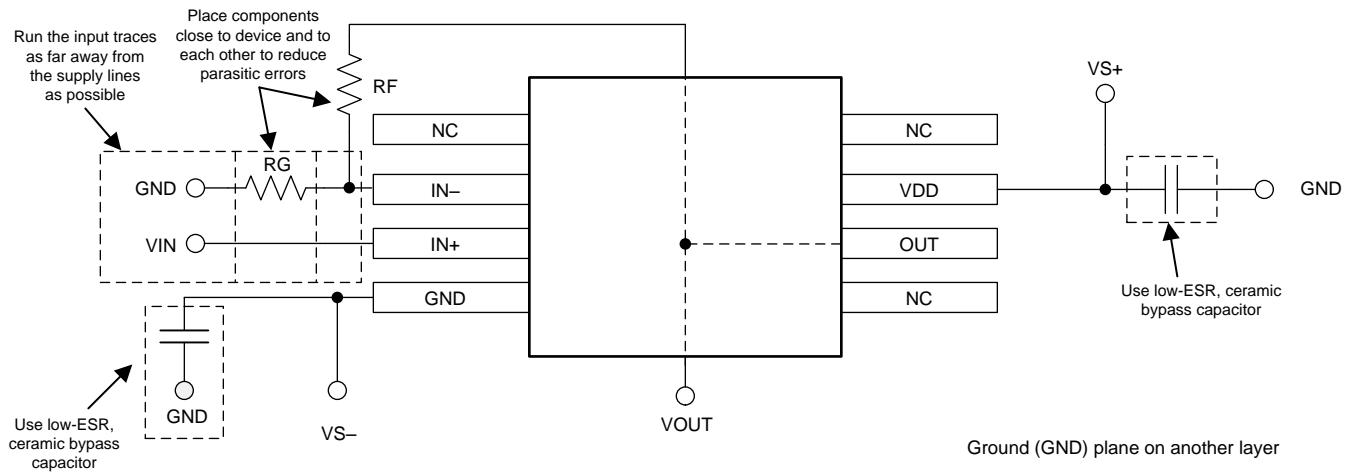
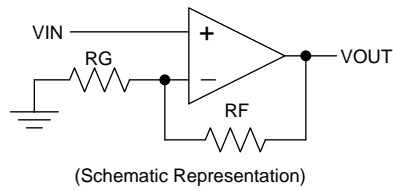
11 Layout

11.1 Layout Guidelines

To achieve the levels of high performance of the TLV27x, follow proper printed circuit board (PCB) design techniques. A general set of guidelines is given in the following.

- Ground planes—TI highly recommends using a ground plane on the board to provide all components with a low-inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling—Use a 6.8- μF tantalum capacitor in parallel with a 0.1- μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1- μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1- μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets—Sockets can be used but are not recommended. The additional lead inductance in the socket pins often leads to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements—Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This helps to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components—Using surface-mount passive components is recommended for high performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, TI recommends keeping the lead lengths as short as possible.

11.2 Layout Example



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Figure 31. TLV27x Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

The following documents are relevant to using the TLV27x, and recommended for reference. All are available for download at www.ti.com unless otherwise noted.

- [Compensate Transimpedance Amplifiers Intuitively](#) (SBOA055)
- [Operational amplifier gain stability, Part 3: AC gain-error analysis](#) (SLYT383)
- [Operational amplifier gain stability, Part 2: DC gain-error analysis](#) (SLYT374)
- [Using the infinite-gain, MFB filter topology in fully differential active filters](#) (SLYT343)
- [Op Amp Performance Analysis](#) (SBOA054)
- [Single-Supply Operation of Operational Amplifiers](#) (SBOA059)
- [Tuning in Amplifiers](#) (SBOA067)
- [Shelf-Life Evaluation of Lead-Free Component Finishes](#) (SZZA046)

12.2 Related Links

[Table 2](#) lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|--------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| TLV271 | Click here | Click here | Click here | Click here | Click here |
| TLV272 | Click here | Click here | Click here | Click here | Click here |
| TLV274 | Click here | Click here | Click here | Click here | Click here |

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
 WEBENCH is a registered trademark of Texas Instruments.
 All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TLV271CD | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | T271C | Samples |
| TLV271CDBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU SN | Level-1-260C-UNLIM | 0 to 70 | VBHC | Samples |
| TLV271CDBVRG4 | LIFEBUY | SOT-23 | DBV | 5 | 3000 | RoHS & Green | SN | Level-1-260C-UNLIM | 0 to 70 | VBHC | |
| TLV271CDBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | RoHS & Green | NIPDAU SN | Level-1-260C-UNLIM | 0 to 70 | VBHC | Samples |
| TLV271CDBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | TBD | Call TI | Call TI | 0 to 70 | | Samples |
| TLV271CDR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | T271C | Samples |
| TLV271ID | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T271I | Samples |
| TLV271IDBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VBHI | Samples |
| TLV271IDBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | TBD | Call TI | Call TI | -40 to 125 | | Samples |
| TLV271IDBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VBHI | Samples |
| TLV271IDBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | TBD | Call TI | Call TI | -40 to 125 | | Samples |
| TLV271IDR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T271I | Samples |
| TLV271IP | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 125 | T271I | Samples |
| TLV272CD | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | T272C | Samples |
| TLV272CDG4 | ACTIVE | SOIC | D | 8 | 75 | TBD | Call TI | Call TI | 0 to 70 | | Samples |
| TLV272CDGK | ACTIVE | VSSOP | DGK | 8 | 80 | RoHS & Green | NIPDAU NIPDAUAG | Level-1-260C-UNLIM | 0 to 70 | AVF | Samples |
| TLV272CDGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | RoHS & Green | NIPDAU NIPDAUAG | Level-1-260C-UNLIM | 0 to 70 | AVF | Samples |
| TLV272CDR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | T272C | Samples |
| TLV272CDRG4 | ACTIVE | SOIC | D | 8 | 2500 | TBD | Call TI | Call TI | 0 to 70 | | Samples |
| TLV272ID | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T272I | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TLV272IDG4 | ACTIVE | SOIC | D | 8 | 75 | TBD | Call TI | Call TI | -40 to 125 | | Samples |
| TLV272IDGK | ACTIVE | VSSOP | DGK | 8 | 80 | RoHS & Green | NIPDAU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | AVG | Samples |
| TLV272IDGKG4 | ACTIVE | VSSOP | DGK | 8 | 80 | TBD | Call TI | Call TI | -40 to 125 | | Samples |
| TLV272IDGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | RoHS & Green | NIPDAU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | AVG | Samples |
| TLV272IDR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T272I | Samples |
| TLV272IDRG4 | LIFEBUY | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T272I | |
| TLV272IP | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 125 | T272I | Samples |
| TLV274CD | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TLV274C | Samples |
| TLV274CDG4 | ACTIVE | SOIC | D | 14 | 50 | TBD | Call TI | Call TI | 0 to 70 | | Samples |
| TLV274CDR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | Call TI NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TLV274C | Samples |
| TLV274CPW | ACTIVE | TSSOP | PW | 14 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TLV274C | Samples |
| TLV274CPWR | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TLV274C | Samples |
| TLV274CPWRG4 | ACTIVE | TSSOP | PW | 14 | 2000 | TBD | Call TI | Call TI | 0 to 70 | | Samples |
| TLV274ID | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TLV274I | Samples |
| TLV274IDG4 | ACTIVE | SOIC | D | 14 | 50 | TBD | Call TI | Call TI | -40 to 125 | | Samples |
| TLV274IDR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | Call TI NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TLV274I | Samples |
| TLV274IDRG4 | ACTIVE | SOIC | D | 14 | 2500 | TBD | Call TI | Call TI | -40 to 125 | | Samples |
| TLV274IN | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 125 | TLV274I | Samples |
| TLV274IPW | ACTIVE | TSSOP | PW | 14 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TLV274I | Samples |
| TLV274IPWG4 | ACTIVE | TSSOP | PW | 14 | 90 | TBD | Call TI | Call TI | -40 to 125 | | Samples |
| TLV274IPWR | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TLV274I | Samples |
| TLV274IPWRG4 | LIFEBUY | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TLV274I | |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TLV271, TLV272, TLV274 :

- Automotive : [TLV271-Q1](#), [TLV272-Q1](#), [TLV274-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TLV271CDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV271CDBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TLV271CDBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV271CDBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV271CDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV271IDBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV271IDBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV271IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV272CDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLV272CDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLV272CDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV272IDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLV272IDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLV272IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV274CDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TLV274CPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TLV274IDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TLV274IPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TLV271CDBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV271CDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TLV271CDBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TLV271CDBVT | SOT-23 | DBV | 5 | 250 | 210.0 | 185.0 | 35.0 |
| TLV271CDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TLV271IDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TLV271IDBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TLV271IDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TLV272CDGKR | VSSOP | DGK | 8 | 2500 | 358.0 | 335.0 | 35.0 |
| TLV272CDGKR | VSSOP | DGK | 8 | 2500 | 364.0 | 364.0 | 27.0 |
| TLV272CDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TLV272IDGKR | VSSOP | DGK | 8 | 2500 | 364.0 | 364.0 | 27.0 |
| TLV272IDGKR | VSSOP | DGK | 8 | 2500 | 358.0 | 335.0 | 35.0 |
| TLV272IDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TLV274CDR | SOIC | D | 14 | 2500 | 340.5 | 336.1 | 32.0 |
| TLV274CPWR | TSSOP | PW | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| TLV274IDR | SOIC | D | 14 | 2500 | 333.2 | 345.9 | 28.6 |
| TLV274IPWR | TSSOP | PW | 14 | 2000 | 356.0 | 356.0 | 35.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| TLV271CD | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TLV271ID | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TLV271IP | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TLV272CD | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TLV272CDGK | DGK | VSSOP | 8 | 80 | 330 | 6.55 | 500 | 2.88 |
| TLV272ID | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TLV272IDGK | DGK | VSSOP | 8 | 80 | 330 | 6.55 | 500 | 2.88 |
| TLV272IP | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TLV274CD | D | SOIC | 14 | 50 | 507 | 8 | 3940 | 4.32 |
| TLV274CPW | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| TLV274ID | D | SOIC | 14 | 50 | 507 | 8 | 3940 | 4.32 |
| TLV274IN | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| TLV274IPW | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |

DBV0005A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

4214839/J 02/2024

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211283-3/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
 EXPOSED METAL SHOWN
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

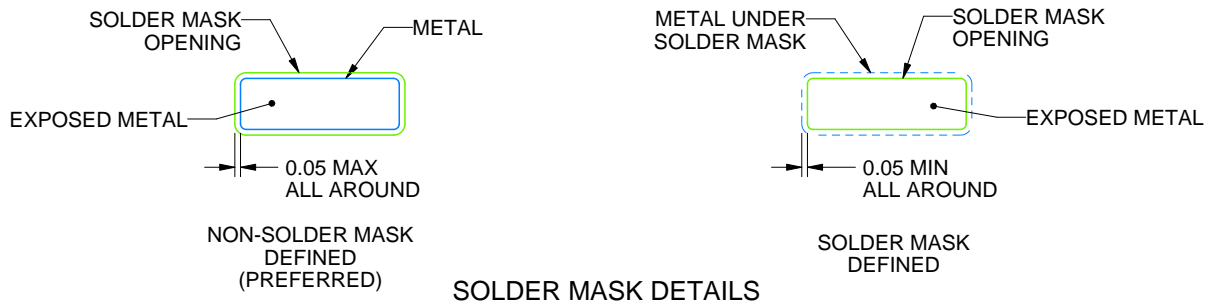
DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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