TLV320x 40ns, microPOWER, Push-Pull Output Comparators

1 Features

- Low Propagation Delay: 40ns
- Low Quiescent Current: 40µA per Channel
- Input Common-Mode Range Extends 200mV Beyond Either Rail
- Low Input Offset Voltage: 1mV
- Push-Pull Outputs
- Supply Range: 2.7V to 5.5V
- Industrial Temperature Range: –40°C to 125°C
- Small Packages: 5-Pin SC70, 5-Pin SOT-23, 8-Pin SOIC, 8-Pin VSSOP

2 Applications

- Inspection Equipment
- Test and Measurement
- High-Speed Sampling Systems
- Telecom
- Portable Communications

3 Description

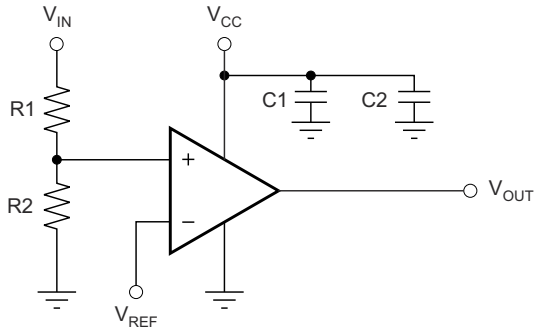
The TLV3201 and TLV3202 are single- and dual-channel comparators that offer the ultimate combination of high speed (40ns) and low-power consumption (40µA), all in extremely small packages with features such as rail-to-rail inputs, low offset voltage (1mV), and large output drive current. The devices are also very easy to implement in a wide variety of applications where response time is critical.

The TLV320x family is available in single (TLV3201) and dual (TLV3202) channel versions, both with push-pull outputs. The TLV3201 is available in 5-pin SOT-23 and 5-pin SC70 packages. The TLV3202 is available in 8-pin SOIC and 8-pin VSSOP packages. All devices are specified for operation across the expanded industrial temperature range of –40°C to 125°C.

Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM) (2)
TLV3201	SOT-23 (5)	2.90mm × 1.60mm
	SC70 (5)	2.00mm × 1.25mm
TLV3202	VSSOP (8)	3.00mm × 3.00mm
	SOIC (8)	4.90mm × 3.91mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable



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Threshold Detector

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4 Device Comparison Table

DEVICE	DESCRIPTION
TLV3011	5µA (maximum) open-drain, 1.8V to 5.5V with integrated voltage reference in 1.5mm × 1.5mm micro-sized packages
TLV3012	5µA (maximum) push-pull, 1.8V to 5.5V with integrated voltage reference in micro-sized packages
TLV3501	4.5ns, rail-to-rail, push-pull comparator in micro-sized packages
LMV7235	75ns, 65µA, 2.7V to 5.5V, rail-to-rail input comparator with open-drain output
REF3333	30ppm/°C drift, 3.9µA, SOT23-3, SC70-3 voltage reference

5 Pin Configuration and Functions

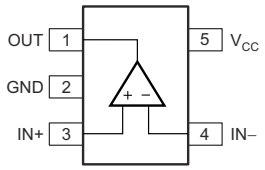

Figure 5-1. TLV3201 DCK and DBV Packages 5-Pin SC70-5 and SOT-23 Top View

Pin Functions: TLV3201

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	2	—	Negative supply, ground
IN–	4	I	Negative input
IN+	3	I	Positive input
OUT	1	O	Output
V_{CC}	5	—	Positive supply

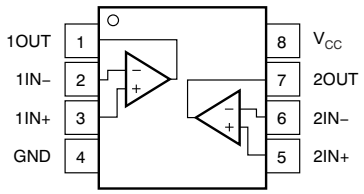

Figure 5-2. TLV3202 D and DGK Packages 8-Pin SOIC and VSSOP Top View

Pin Functions: TLV3202

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN–	2	I	Negative input, comparator 1
1IN+	3	I	Positive input, comparator 1
1OUT	1	O	Output, comparator 1
2IN–	6	I	Negative input, comparator 2
2IN+	5	I	Positive input, comparator 2
2OUT	7	O	Output, comparator 2
GND	4	—	Negative supply, ground
V_{CC}	8	—	Positive supply

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply voltage		7	V
	Signal input pins(2)	–0.5	(V_{CC}) + 0.5	
Current	Signal input pins(2)	–10	10	mA
	Output short circuit(3)		100	
Temperature	Operating	–55	125	°C
	Junction, T_J		150	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Section 6.3*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails must be current limited to 10 mA or less.
(3) Short-circuit to ground.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)		±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	TLV3201	±2000	
		TLV3202	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, V_S = (V_{S+}) – ($V_{S–}$)	2.7 (±1.35)	5.5 (±2.75)	V
	Specified temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TLV3201		TLV3202		UNIT
		DBV (SOT-23)	DCK (SC70)	D (SOIC)	DGK (VSSOP)	
		5 PINS	5 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	237.8	281.9	143.6	201.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	108.7	97.6	97.2	92.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	64.1	68.3	84.2	123.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12.1	2.6	45.5	23.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	63.3	67.3	83.7	212.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics: V_{CC} = 5V

at T_A = 25°C and V_{CC} = 5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
$V_{IO-TLV3201}$	Input offset voltage TLV3201	V_{CM} = V_{CC} / 2		1	3	mV
		T_A = –40°C to 125°C			4	
$V_{IO-TLV3202}$	Input offset voltage TLV3202	V_{CM} = V_{CC} / 2		1	5	mV
		T_A = –40°C to 125°C			6	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to 125°C		1	10	µV/°C
PSRR	Power-supply rejection ratio	V_{CM} = V_{CC} / 2, V_{CC} = 2.5V to 5.5V	65	85		dB
	Input hysteresis			1.2		mV
INPUT BIAS CURRENT						
I_{IB}	Input bias current	V_{CM} = V_{CC} / 2		1	50	pA
		T_A = –40°C to 125°C			5	nA
I_{IO}	Input offset current	V_{CM} = V_{CC} / 2		1	50	pA
		T_A = –40°C to 125°C			2.5	nA
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage	T_A = –40°C to 125°C	(V_{EE}) – 0.2		(V_{CC}) + 0.2	V
CMRR	Common-mode rejection ratio	–0.2V < V_{CM} < 5.2V	60	70		dB
INPUT IMPEDANCE						
	Common mode			10^{13} || 2		Ω ||pF
	Differential			10^{13} || 4		Ω ||pF
OUTPUT						
V_{OL}	Voltage output swing from lower rail	I_{SINK} = 4mA		175	190	mV
		T_A = –40°C to 125°C			225	
V_{OH}	Voltage output swing from upper rail	I_{SOURCE} = 4mA		120	140	mV
		T_A = –40°C to 125°C			170	
I_{SC}	Short-circuit current (per comparator)	I_{SC} sinking	40	48		mA
		T_A = –40°C to 125°C	See Figure 6-14			
		I_{SC} sourcing	52	60		
		T_A = –40°C to 125°C	See Figure 6-14			
POWER SUPPLY						
V_{CC}	Specified voltage		2.7		5.5	V
I_Q	Quiescent current	T_A = 25°C		40	50	µA
		T_A = –40°C to 125°C			65	

6.6 Switching Characteristics: V_{CC} = 5V

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PD}	Propagation delay time	Low to high	Input overdrive = 20mV , C_L = 15pF		47	50	ns
			Input overdrive = 100mV , C_L = 15pF		43	50	
			T_A = –40°C to 125°C			55	
		High to low	Input overdrive = 20mV , C_L = 15pF		45	50	
			Input overdrive = 100mV , C_L = 15pF		42	50	
			T_A = –40°C to 125°C			55	
	Propagation delay skew	Input overdrive = 20mV , C_L = 15pF			2		ns
t_R	Rise time	10% to 90%			2.9		ns
t_F	Fall time	10% to 90%			3.7		ns

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6.7 Electrical Characteristics: V_{CC} = 2.7V

at T_A = 25°C and V_{CC} = 2.7V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
$V_{IO-TLV3201}$	Input offset voltage TLV3201	V_{CM} = V_{CC} / 2		1	3	mV
		T_A = –40°C to 125°C			4	
$V_{IO-TLV3202}$	Input offset voltage TLV3202	V_{CM} = V_{CC} / 2		1	5	mV
		T_A = –40°C to 125°C			6	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to 125°C		1	10	µV/°C
PSRR	Power-supply rejection ratio	V_{CM} = V_{CC} / 2, V_{CC} = 2.5V to 5.5V	65	85		dB
	Input hysteresis			1.2		mV
INPUT BIAS CURRENT						
I_{IB}	Input bias current	V_{CM} = V_{CC} / 2		1	50	pA
		T_A = –40°C to 125°C			5	nA
I_{IO}	Input offset current	V_{CM} = V_{CC} / 2		1	50	pA
		T_A = –40°C to 125°C			2.5	nA
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage	T_A = –40°C to 125°C	(V_{EE}) – 0.2		(V_{CC}) + 0.2	V
CMRR	Common-mode rejection ratio	–0.2V < V_{CM} < 2.9V	56	68		dB
INPUT IMPEDANCE						
	Common mode			10^{13} || 2		Ω ||pF
	Differential			10^{13} || 4		Ω ||pF
OUTPUT						
V_{OL}	Voltage output swing from lower rail	I_{SINK} = 4mA		230	260	mV
		T_A = –40°C to 125°C			325	
V_{OH}	Voltage output swing from upper rail	I_{SOURCE} = 4mA		210	250	mV
		T_A = –40°C to 125°C			350	
I_{SC}	Short-circuit current (per comparator)	I_{SC} sinking	13	19		mA
		T_A = –40°C to 125°C	See Figure 6-14			
		I_{SC} sourcing	15	21		
		T_A = –40°C to 125°C	See Figure 6-14			
POWER SUPPLY						
V_{CC}	Specified voltage		2.7		5.5	V
I_Q	Quiescent current	T_A = 25°C		36	46	µA
		T_A = –40°C to 125°C			60	

6.8 Switching Characteristics: V_{CC} = 2.7V

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PD}	Propagation delay time	Low to high	Input overdrive = 20mV , C_L = 15pF		47	50	ns
			Input overdrive = 100mV , C_L = 15pF		42	50	
			T_A = –40°C to 125°C			55	
		High to low	Input overdrive = 20mV , C_L = 15pF		40	50	
			Input overdrive = 100mV , C_L = 15pF		38	50	
			T_A = –40°C to 125°C			55	
	Propagation delay skew	Input overdrive = 20mV , C_L = 15pF			2		ns
t_R	Rise time	10% to 90%			4.8		ns
t_F	Fall time	10% to 90%			5.2		ns

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6.9 Typical Characteristics

at T_A = 25°C, V_{CC} = 5V, and input overdrive (V_{OD}) = 20mV (unless otherwise noted)

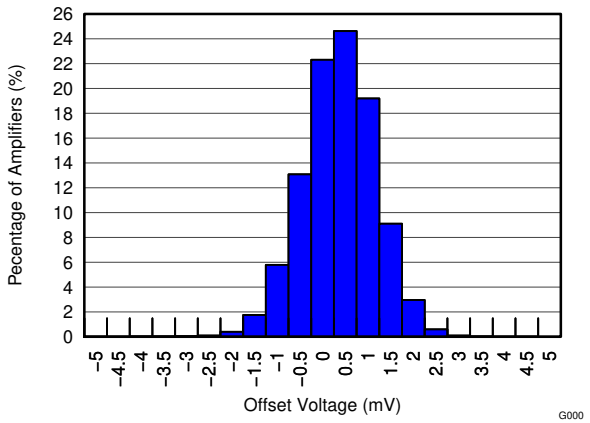

Figure 6-1. Offset Voltage Distribution

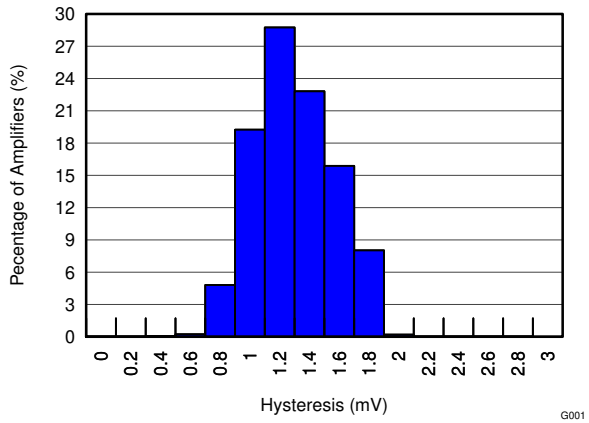

Figure 6-2. Hysteresis Distribution

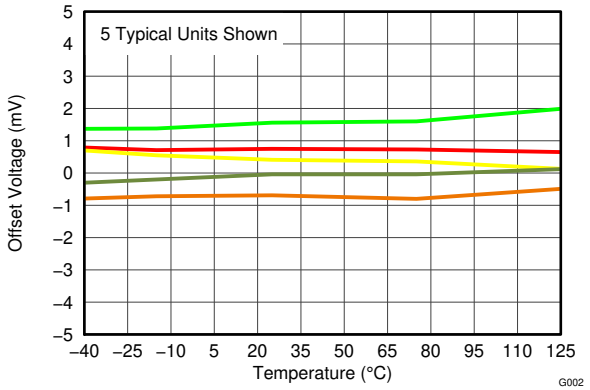

Figure 6-3. Offset Voltage vs Temperature

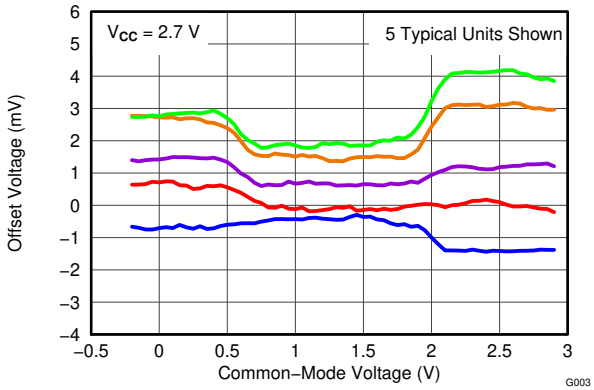

Figure 6-4. Offset Voltage vs Common-Mode Voltage

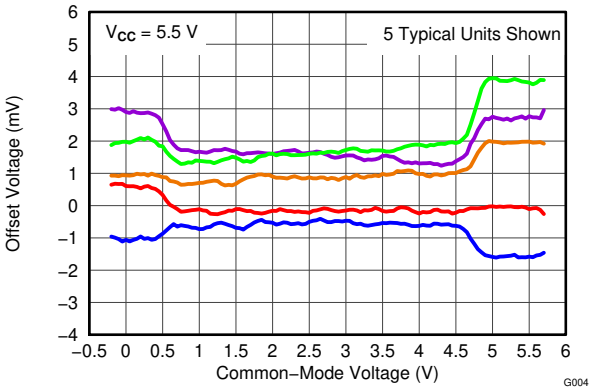

Figure 6-5. Offset Voltage vs Common-Mode Voltage

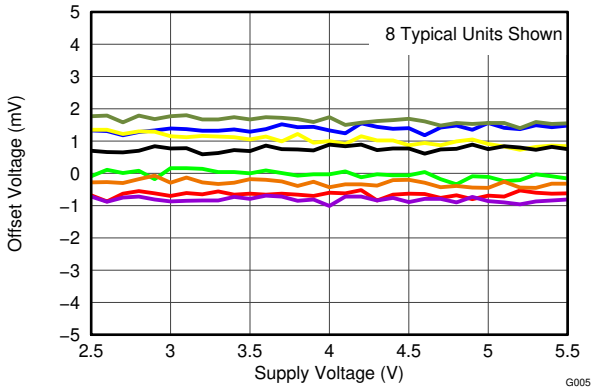

Figure 6-6. Offset Voltage vs Power Supply

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6.9 Typical Characteristics (continued)

at T_A = 25°C, V_{CC} = 5V, and input overdrive (V_{OD}) = 20mV (unless otherwise noted)

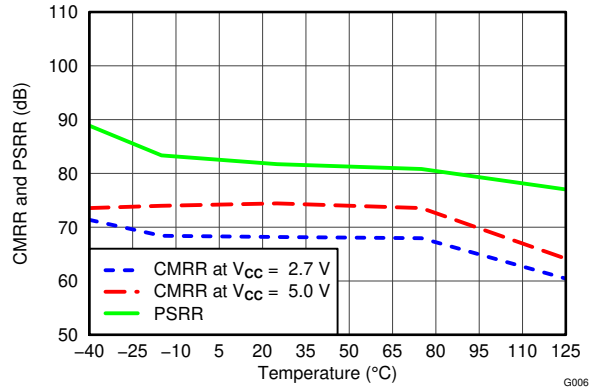

Figure 6-7. Common-Mode Rejection Ratio and Power-Supply Rejection Ratio vs Temperature

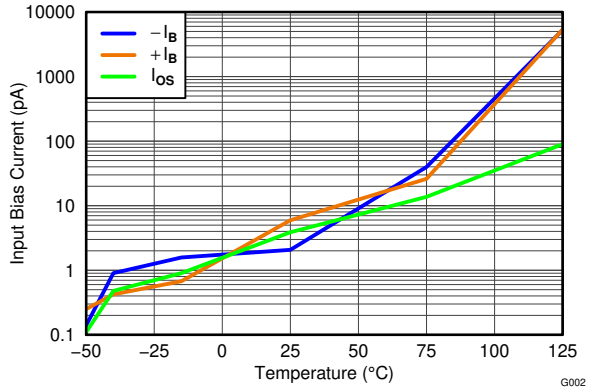

Figure 6-8. Input Bias Current and Input Offset Current vs Temperature

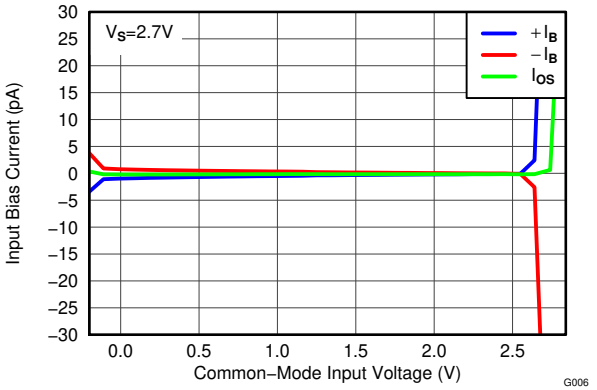

Figure 6-9. Input Bias Current and Input Offset Current vs Common-Mode Input Voltage

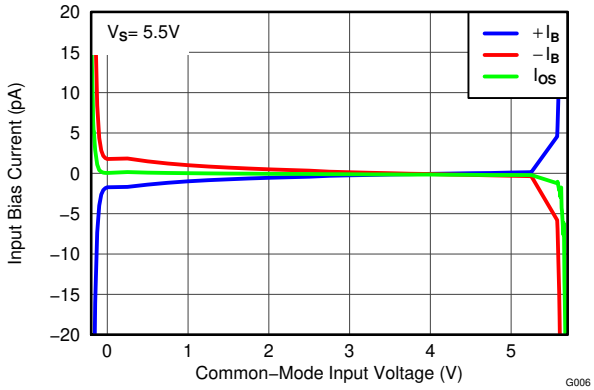

Figure 6-10. Input Bias Current and Input Offset Current vs Common-Mode Input Voltage

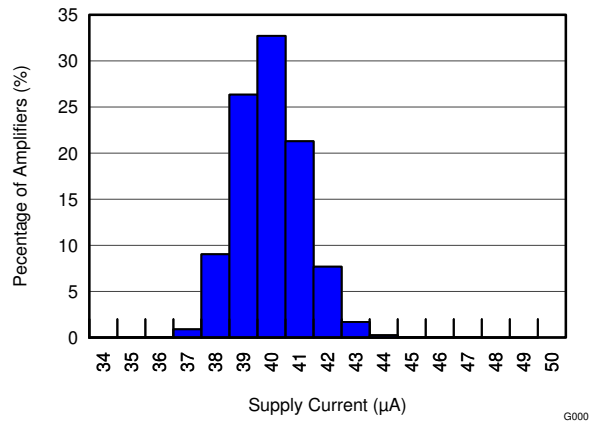

Figure 6-11. Quiescent Current Distribution

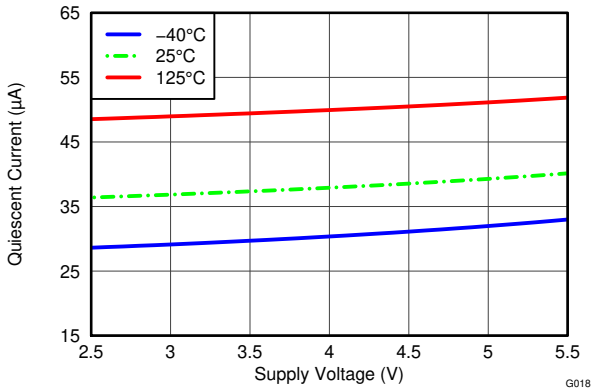

Figure 6-12. Quiescent Current vs Supply Voltage

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6.9 Typical Characteristics (continued)

at T_A = 25°C, V_{CC} = 5V, and input overdrive (V_{OD}) = 20mV (unless otherwise noted)

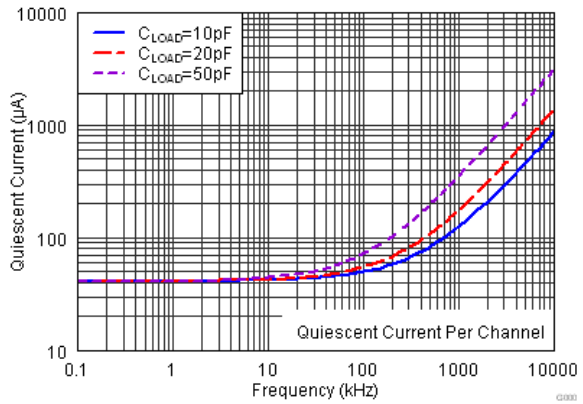

Figure 6-13. Quiescent Current vs Switching Frequency

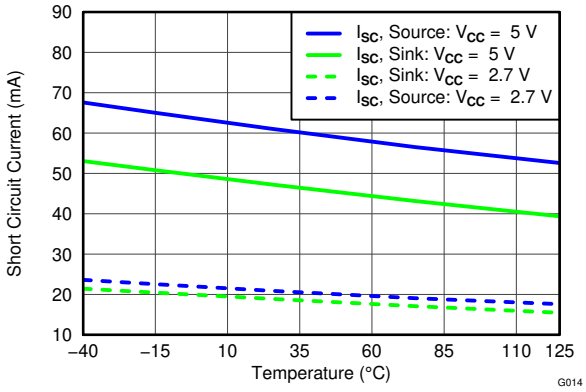

Figure 6-14. Short-Circuit Current vs Temperature

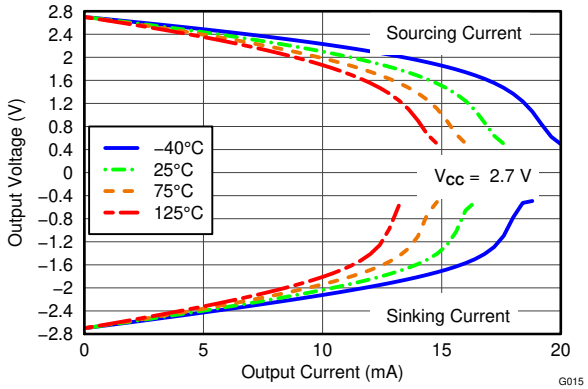

Figure 6-15. Output Voltage vs Output Current

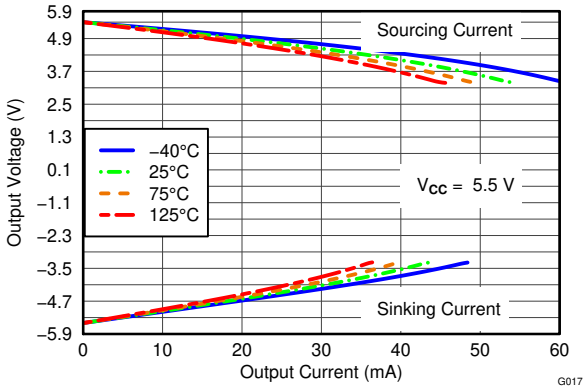

Figure 6-16. Output Voltage vs Output Current

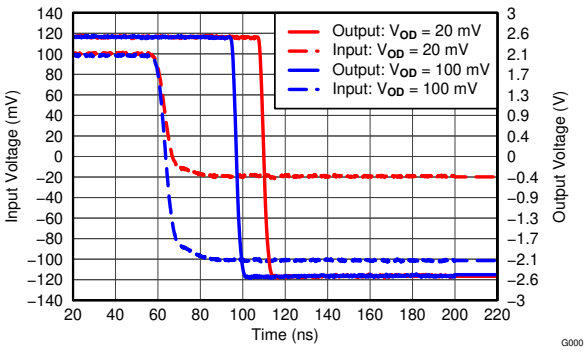

Figure 6-17. Propagation Delay Falling Edge

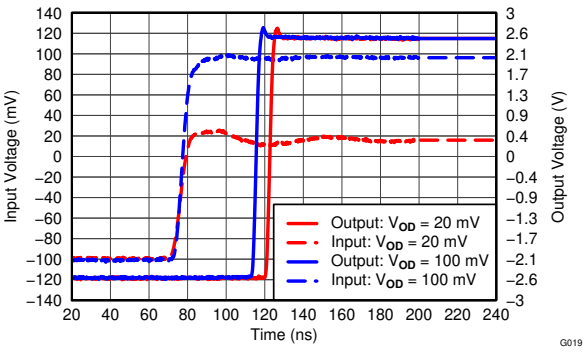

Figure 6-18. Propagation Delay Rising Edge

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6.9 Typical Characteristics (continued)

at T_A = 25°C, V_{CC} = 5V, and input overdrive (V_{OD}) = 20mV (unless otherwise noted)

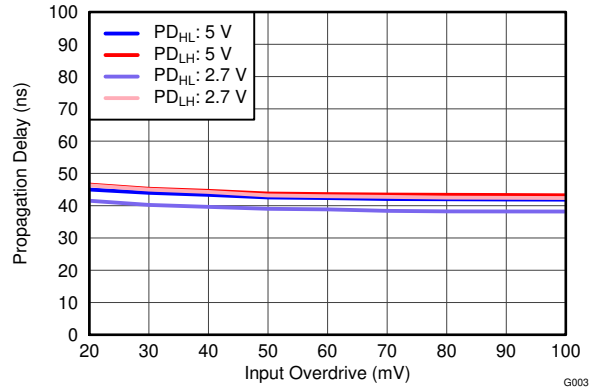

Figure 6-19. Propagation Delay vs Input Overdrive

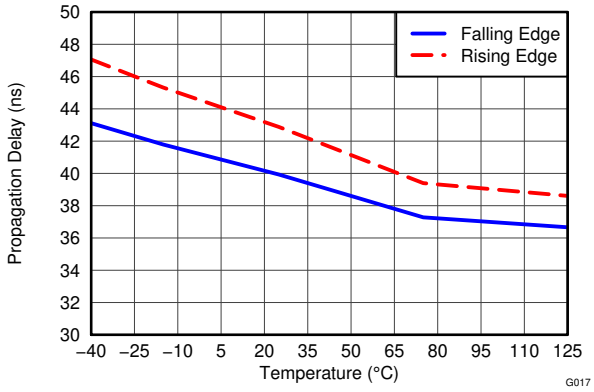

Figure 6-20. Propagation Delay vs Temperature

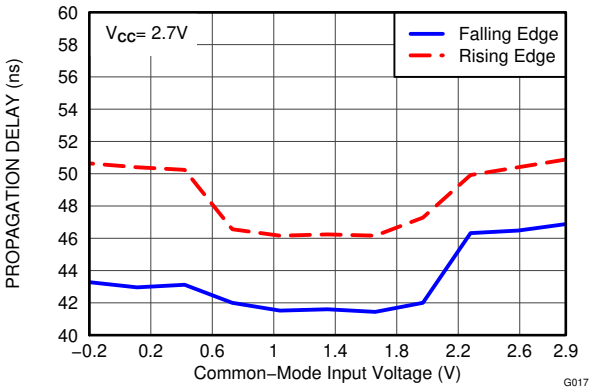

Figure 6-21. Propagation Delay vs Common-Mode Voltage

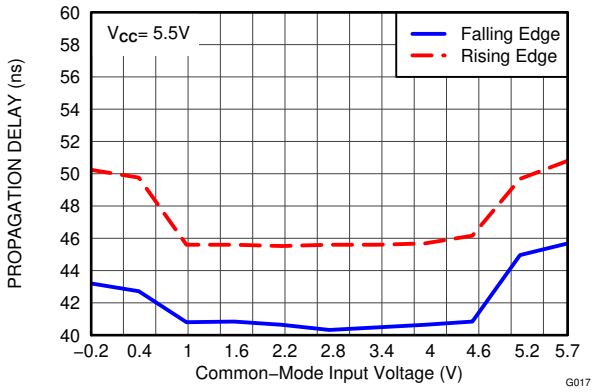

Figure 6-22. Propagation Delay vs Common-Mode Voltage

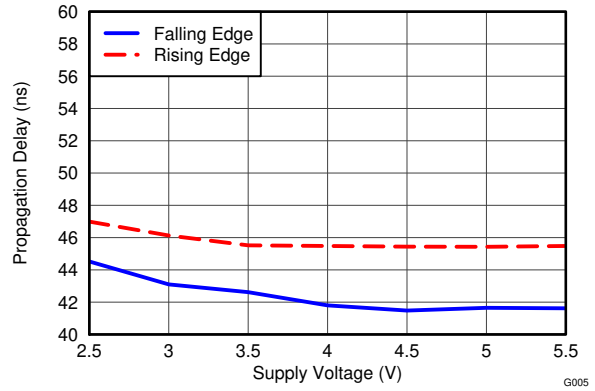

Figure 6-23. Propagation Delay vs Supply Voltage

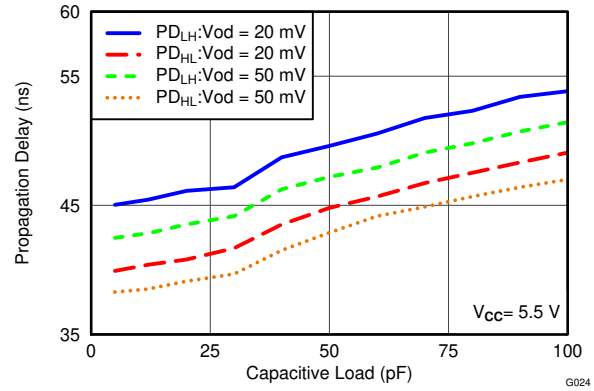

Figure 6-24. Propagation Delay vs Capacitive Load

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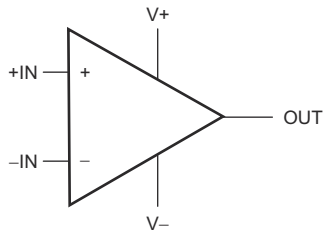
7 Detailed Description

7.1 Overview

The TLV3201 and TLV3202 devices feature 40ns response time, and include 1.2mV of internal hysteresis for improved noise immunity with an input common-mode range that extends 0.2V beyond the power-supply rails.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Operating Voltage

The TLV3201 and TLV3202 comparators are specified for use on a single supply from 2.7V to 5.5V (or a dual supply from ±1.35V to ±2.75V) over a temperature range of −40°C to 125°C. The device continues to function below this range, but performance is not specified.

7.3.2 Input Overvoltage Protection

The device inputs are protected by electrostatic discharge (ESD) diodes that conduct if the input voltages exceed the power supplies by more than approximately 300mV . Momentary voltages greater than 300mV beyond the power supply can be tolerated if the input current is limited to 10mA. This limiting is easily accomplished with a small input resistor in series with the input to the comparator.

7.4 Device Functional Modes

The device is fully functional when powered by rail-to-rail supply voltage greater than 2.7V. The device is off at any voltages below 2.7V.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TLV3201 and TLV3202 are single- and dual-supply (respectively), push-pull comparators featuring 40ns of propagation delay on only 40µA of supply current. This combination of fast response time and minimal power consumption make the TLV3201 and TLV3202 excellent comparators for portable, battery-powered applications as well as fast-switching threshold detection such as pulse-width modulation (PWM) output monitors and zero-cross detection.

8.1.1 Comparator Inputs

The TLV3201 and TLV3202 are rail-to-rail input comparators, with an input common-mode range that exceeds the supply rails by 200mV for both positive and negative supplies. The devices are specified from 2.7V to 5.5V, with room temperature operation from 2.5V to 5.5V. The TLV3201 and TLV3202 are designed to prevent phase inversion when the input pins exceed the supply voltage. Figure 8-1 shows the TLV320x response when input voltages exceed the supply, resulting in no phase inversion.

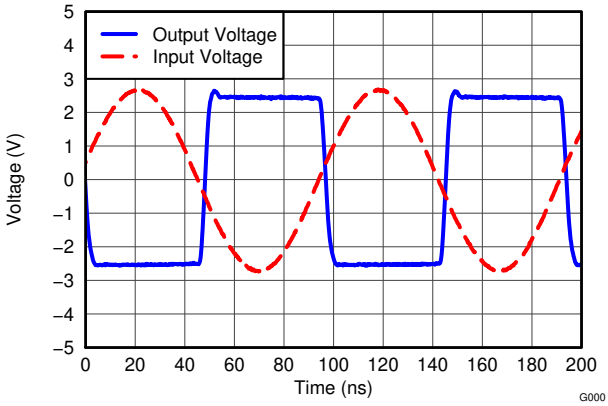

Figure 8-1. No Phase Inversion: Comparator Response to Input Voltage (Propagation Delay Included)

The electrostatic discharge (ESD) protection input structure of two back-to-back diodes and 1kΩ series resistors are used to limit the differential input voltage applied to the precision input of the comparator by clamping input voltages that exceed V_{CC} beyond the specified operating conditions. If potential overvoltage conditions that exceed absolute maximum ratings are present, the addition of external bypass diodes and resistors is recommended, as shown in Figure 8-2. Large differential voltages greater than the supply voltage must be avoided to prevent damage to the input stage.

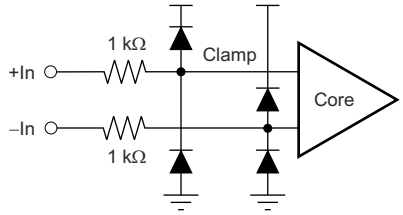

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Figure 8-2. TLV3201 Equivalent Input structure

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8.1.2 External Hysteresis

The TLV3201 and TLV3202 have a hysteresis transfer curve (shown in Figure 8-3) that is a function of three components: V_{TH}, V_{OS}, and V_{HYST}.

- V_{TH}: the actual set voltage or threshold trip voltage
- V_{OS}: the internal offset voltage between V_{IN+} and $V_{IN–}$. This voltage is added to V_{TH} to form the actual trip point at which the comparator must respond to change output states.
- V_{HYST}: internal hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise.

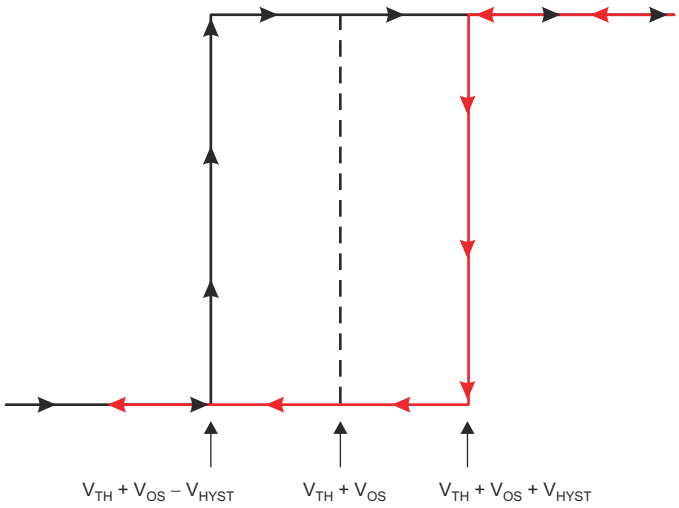

Figure 8-3. TLV320x Hysteresis Transfer Curve

8.1.2.1 Inverting Comparator with Hysteresis

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage (V_{CC}), as shown in Figure 8-4. When V_{IN} at the inverting input is less than V_A, the output voltage is high (for simplicity, assume V_O switches as high as V_{CC}). The three network resistors can be represented as R1 || R3 in series with R2. The lower input trip voltage (V_{A1}) is defined by Equation 1.

$$V_{A1} = V_{CC} \times \frac{R2}{(R1 \parallel R3) + R2} \tag{1}$$

When V_{IN} is greater than [V_A × (V_{IN} > V_A)], the output voltage is low, very close to ground. In this case, the three network resistors can be presented as R2 || R3 in series with R1. The upper trip voltage (V_{A2}) is defined by Equation 2.

$$V_{A2} = V_{CC} \times \frac{R2 \parallel R3}{R1 + (R2 \parallel R3)} \tag{2}$$

The total hysteresis provided by the network is defined by Equation 3.

$$\Delta V_A = V_{A1} - V_{A2} \tag{3}$$

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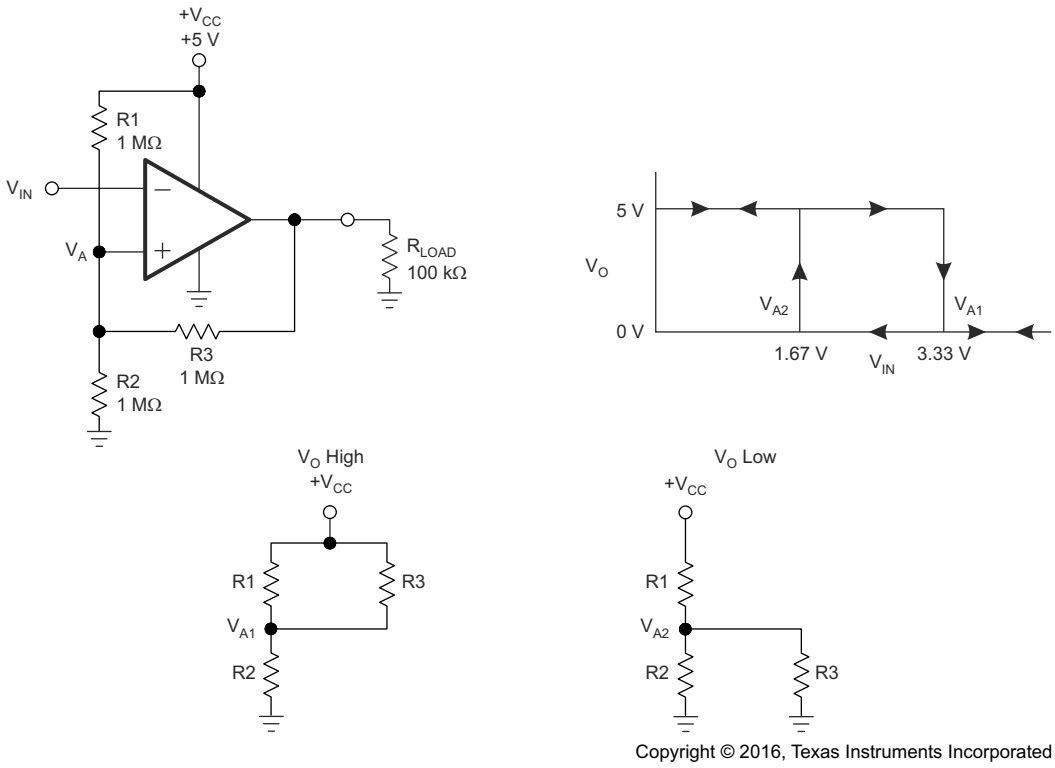

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Figure 8-4. TLV3201 in Inverting Configuration With Hysteresis

8.1.2.2 Noninverting Comparator With Hysteresis

A noninverting comparator with hysteresis requires a two-resistor network, as shown in Figure 8-5, and a voltage reference (V_{REF}) at the inverting input. When V_{IN} is low, the output is also low. For the output to switch from low to high, V_{IN} must rise up to V_{IN1}. V_{IN1} is calculated by Equation 4.

$$V_{IN1} = R1 \times \frac{V_{REF}}{R2} \times V_{REF} \tag{4}$$

When V_{IN} is high, the output is also high. In order for the comparator to switch back to a low state, V_{IN} must equal V_{REF} before V_A is again equal to V_{REF}. V_{IN} can be calculated by Equation 5.

$$V_{IN2} = \frac{V_{REF}\,(R1 + R2) - V_{CC} \times R1}{R2} \tag{5}$$

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2}, as defined by Equation 6.

$$\Delta V_{IN} = V_{CC} \times \frac{R1}{R2} \tag{6}$$

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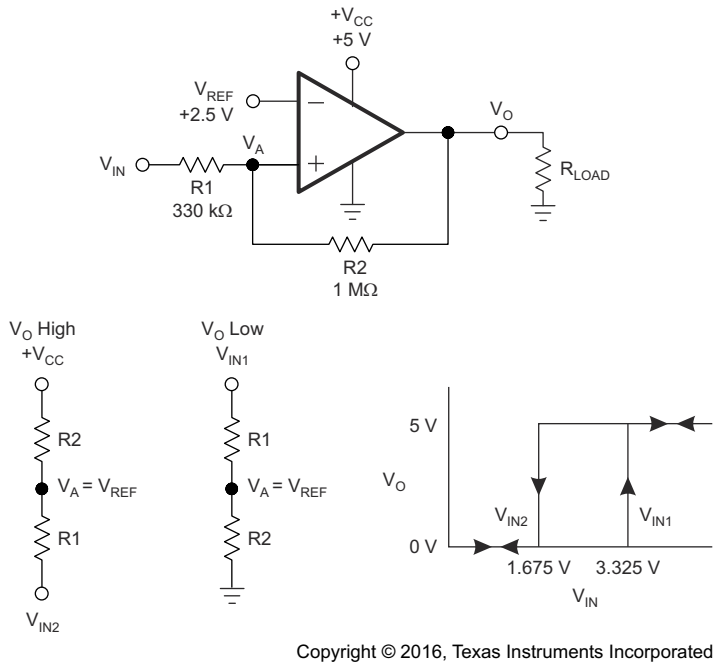

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Figure 8-5. TLV3201 in Noninverting Configuration With Hysteresis

8.1.3 Capacitive Loads

The TLV3201 and TLV3202 feature a push-pull output. When the output switches, there is a direct path between V_{CC} and ground, causing increased output sinking or sourcing current during the transition. Following the transition the output current decreases and supply current returns to 40µA, thus maintaining low power consumption. Under reasonable capacitive loads, the TLV3201 and TLV3202 maintain specified propagation delay (see *Section 6.9*), but excessive capacitive loading under high switching frequencies may increase supply current, propagation delay, or induce decreased slew rate.

8.2 Typical Applications

8.2.1 TLV3201 Configured as an AC-Coupled Comparator

One of the benefits of AC coupling a single-supply comparator circuit is that it can block dc offsets induced by ground-loop offsets that could potentially produce either a false trip or a common-mode input violation. Figure 8-6 shows the TLV3201 configured as an ac-coupled comparator.

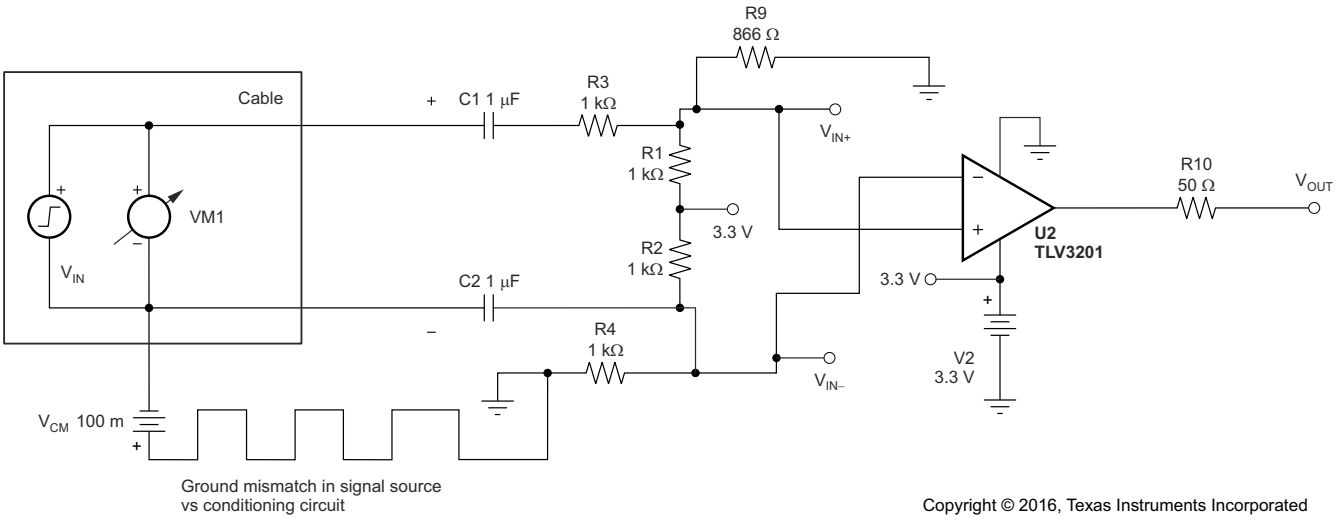

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Figure 8-6. TLV3201 Configured as an AC-Coupled Comparator (Schematic)

8.2.1.1 Design Requirements

Design requirements include:

- Ability to tolerate up to ±100mV of common-mode signal.
- Trigger only on AC signals (such as zero-cross detection).

8.2.1.2 Detailed Design Procedure

Design analysis:

- AC-coupled, high-pass frequency
- Large capacitors require longer start-up time from device power on
- Use 1µF capacitor to achieve high-pass frequency of approximately 159Hz
- For high-pass equivalent, use C_{IN} = 0.5µF, R_{IN} = 2kΩ

1. Set up input dividers initially for one-half supply (to be in center of acceptable common-mode range).
2. Adjust either divider slightly upwards or downwards as desired to establish quiescent output condition.
3. Select coupling capacitors based on lowest expected frequency.

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8.2.1.3 Application Curve

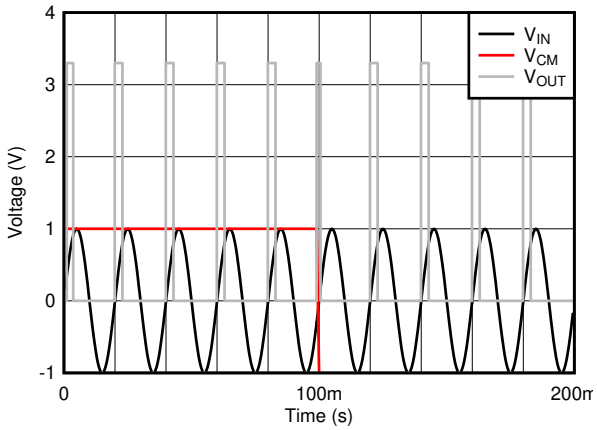

Figure 8-7. AC-Coupled Comparator Results

8.2.2 TLV3201 and OPA320 Configured as a Fast-Response Output Current Monitor

Figure 8-8 shows a single-supply current monitor configured as a difference amplifier with a gain of 50. The OPA320 was chosen for this circuit because of its gain bandwidth (20 MHz), which allows higher speed triggering and monitoring of the current across the shunt resistor followed by the fast response of the TLV3201.

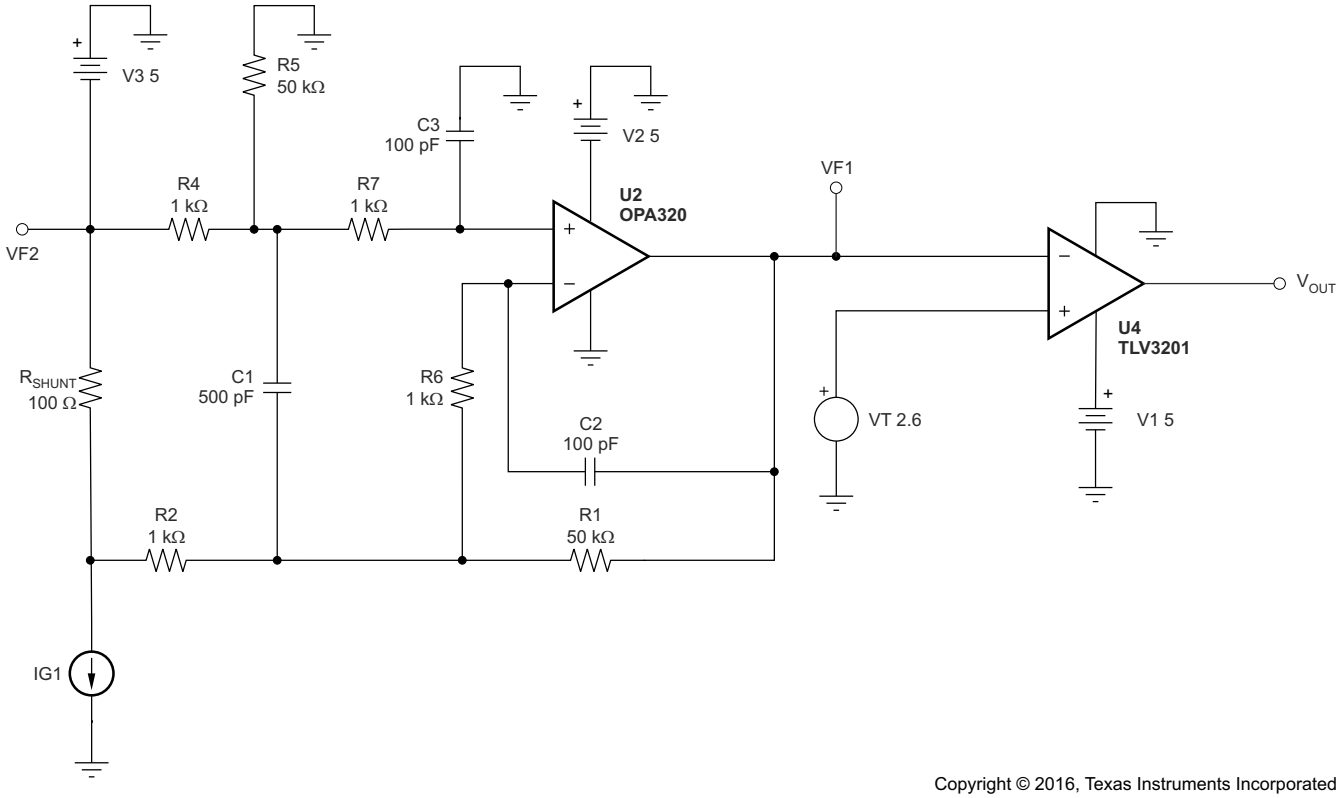

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Figure 8-8. TLV3201 and OPA320 Configured as a Fast-Response Output Current Monitor

8.2.3 TLV3201 and TMP20 Configured as a Precision Analog Temperature Switch

Figure 8-9 shows the TMP20 and TLV3201 designed as a high-speed temperature switch. The TMP20 is an analog output temperature sensor where output voltage decreases with temperature. The comparator output is tripped when the output reaches a critical trip threshold.

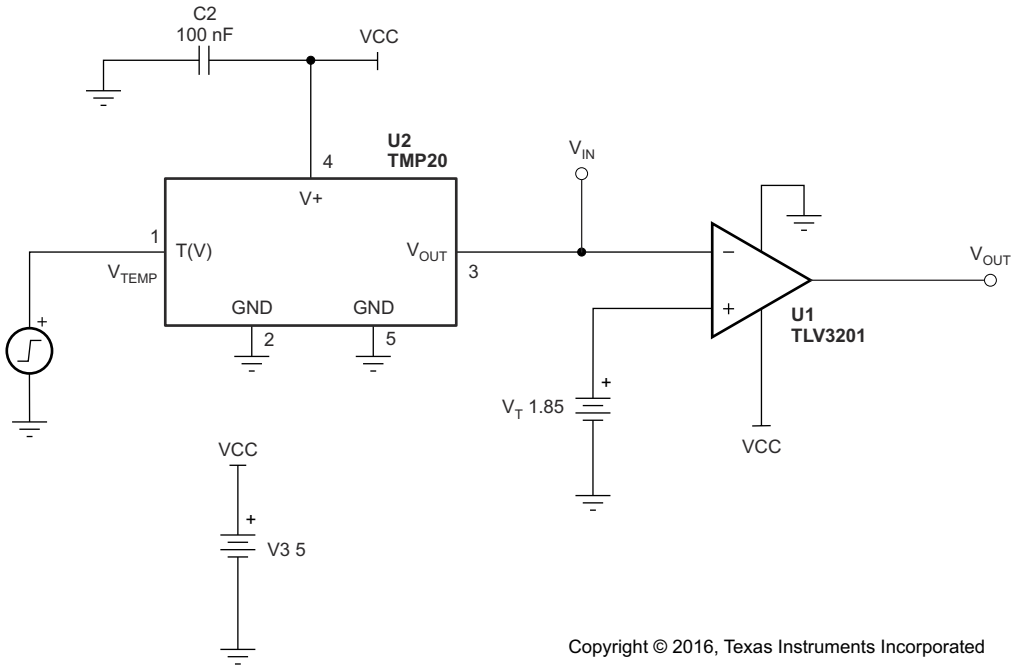

Figure 8-9. TLV3201 and TMP20 Configured as a Precision Analog Temperature Switch

8.3 Power Supply Recommendations

The TLV3201 and TLV3202 comparators are specified for use on a single supply from 2.7V to 5.5V (or a dual supply from ±1.35V to ±2.75V) over a temperature range of −40°C to 125°C. The device continues to function below this range, but performance is not specified. Place bypass capacitors close to the power-supply pins to reduce noise coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see *Section 8.4.1*.

8.4 Layout

8.4.1 Layout Guidelines

The TLV3201 and TLV3202 are fast-switching, high-speed comparators and require high-speed layout considerations. For best results, maintain the following layout guidelines.

- Use a printed-circuit board (PCB) with a good, unbroken low-inductance ground plane.
- Place a decoupling capacitor (0.1µF ceramic, surface-mount capacitor) as close as possible to V_{CC}.
- On the inputs and the output, keep lead lengths as short as possible to avoid unwanted parasitic feedback around the comparator. Keep inputs away from the output.
- Solder the device directly to the PCB rather than using a socket.
- For slow-moving input signals, take care to prevent parasitic feedback. A small capacitor (1000pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes some degradation to propagation delay when the impedance is low. The topside ground plane runs between the output and inputs.
- The ground pin ground trace runs under the device up to the bypass capacitor, shielding the inputs from the outputs.

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8.4.2 Layout Example

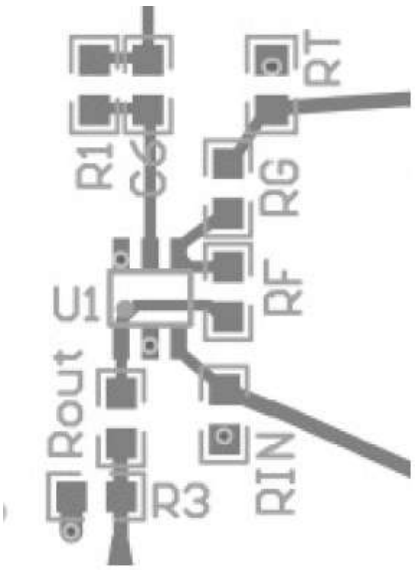

Figure 8-10. TLV320x Board Layout Example

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

9.1.1.1 TINA-TI™ (Free Software Download)

TINA-TI™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

9.1.1.2 Universal Op Amp EVM

The Universal Op Amp EVM is a series of general-purpose, blank circuit boards that simplify prototyping circuits for a variety of IC package types. The evaluation module board design allows many different circuits to be constructed easily and quickly. Five models are offered, with each model intended for a specific package type. PDIP, SOIC, MSOP, TSSOP and SOT23 packages are all supported.

Note

These boards are unpopulated, so users must provide their own ICs. TI recommends requesting several op amp device samples when ordering the Universal Op Amp EVM.

9.1.1.3 TI Precision Designs

TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI Precision Designs are available online at http://www.ti.com/ww/en/analog/precision-designs/.

9.1.1.4 WEBENCH® Filter Designer

WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web-based tool from the WEBENCH® Design Center, WEBENCH® Filter Designer allows you to design, optimize, and simulate complete multistage active filter solutions within minutes.

9.2 Documentation Support

9.2.1 Related Documentation

The following documents are relevant to using the TLV320x, and recommended for reference. All are available for download at www.ti.com unless otherwise noted.

- *Frequency Dithering With the UCC28950 and TLV3201* (SLUA646)
- *Frequency Dithering with the UCC28180 and TLV3201* (SLUA704)
- *Comparator with Hysteresis Reference Design* (TIDU020)

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9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.5 Trademarks

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All trademarks are the property of their respective owners.

9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (December 2016) to Revision C (June 2022)	Page
• Corrected transposed TLV3202 D and DGK columns in Thermal Metric table	4
• Corrected typo in DGK Tja from 146.3 to 143.6 for DGK in Thermal Metric table	4
• Added Input Offset Voltage for TLV3201 for 5V	5
• Added 5V Switching Specifications table	5
• Added Input Offset Voltage for TLV3201 for 2.7V	6

Changes from Revision A (June 2012) to Revision B (December 2016)	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Deleted *Ordering Information* table; see *Package Option Addendum* at the end of the data sheet	1

Changes from Revision * (March 2012) to Revision A (June 2012)	Page
• Changed product status from Production Data to Mixed Status	1
• Added dual channel device	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV3201AIDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	RAI
TLV3201AIDBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	RAI
TLV3201AIDBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	RAI
TLV3201AIDBVT.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	RAI
TLV3201AIDCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU | SPOT AG (TOP SIDE) | SN	Level-2-260C-1 YEAR	-40 to 125	SDP
TLV3201AIDCKR.B	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SDP
TLV3201AIDCKRG4	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SDP
TLV3201AIDCKRG4.B	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SDP
TLV3201AIDCKT	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU | SPOT AG (TOP SIDE)	Level-2-260C-1 YEAR	-40 to 125	SDP
TLV3201AIDCKT.B	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SDP
TLV3202AID	Active	Production	SOIC (D) | 8	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL3202
TLV3202AID.B	Active	Production	SOIC (D) | 8	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL3202
TLV3202AIDGK	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VUDC
TLV3202AIDGK.B	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VUDC
TLV3202AIDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VUDC
TLV3202AIDGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VUDC
TLV3202AIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL3202
TLV3202AIDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL3202
TLV3202AIDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL3202
TLV3202AIDRG4.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL3202

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TLV3201, TLV3202 :

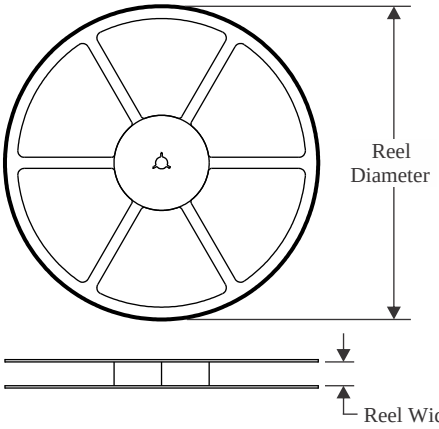
- Automotive : TLV3201-Q1, TLV3202-Q1

NOTE: Qualified Version Definitions:

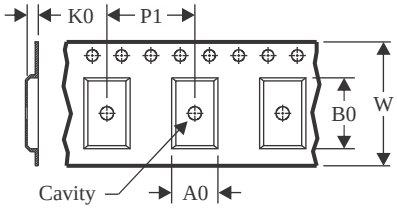
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

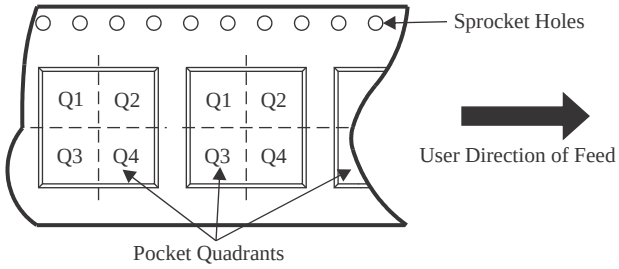


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

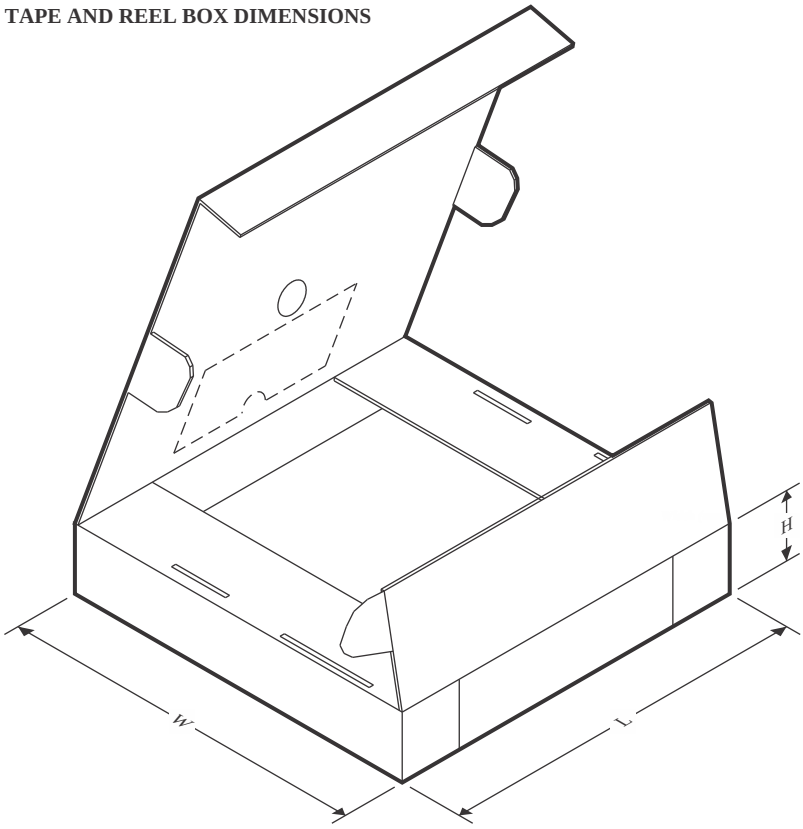
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV3201AIDBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV3201AIDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV3201AIDCKR	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
TLV3201AIDCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
TLV3201AIDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV3201AIDCKRG4	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV3201AIDCKT	SC70	DCK	5	250	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
TLV3201AIDCKT	SC70	DCK	5	250	178.0	8.4	2.4	2.5	1.2	4.0	8.0	Q3
TLV3202AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV3202AIDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

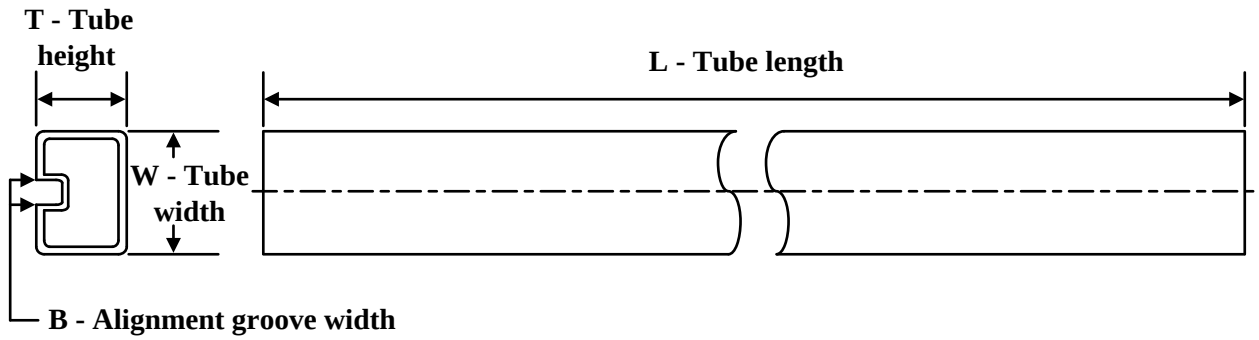
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV3201AIDBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TLV3201AIDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TLV3201AIDCKR	SC70	DCK	5	3000	208.0	191.0	35.0
TLV3201AIDCKR	SC70	DCK	5	3000	210.0	185.0	35.0
TLV3201AIDCKR	SC70	DCK	5	3000	190.0	190.0	30.0
TLV3201AIDCKRG4	SC70	DCK	5	3000	190.0	190.0	30.0
TLV3201AIDCKT	SC70	DCK	5	250	210.0	185.0	35.0
TLV3201AIDCKT	SC70	DCK	5	250	190.0	190.0	30.0
TLV3202AIDGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
TLV3202AIDRG4	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

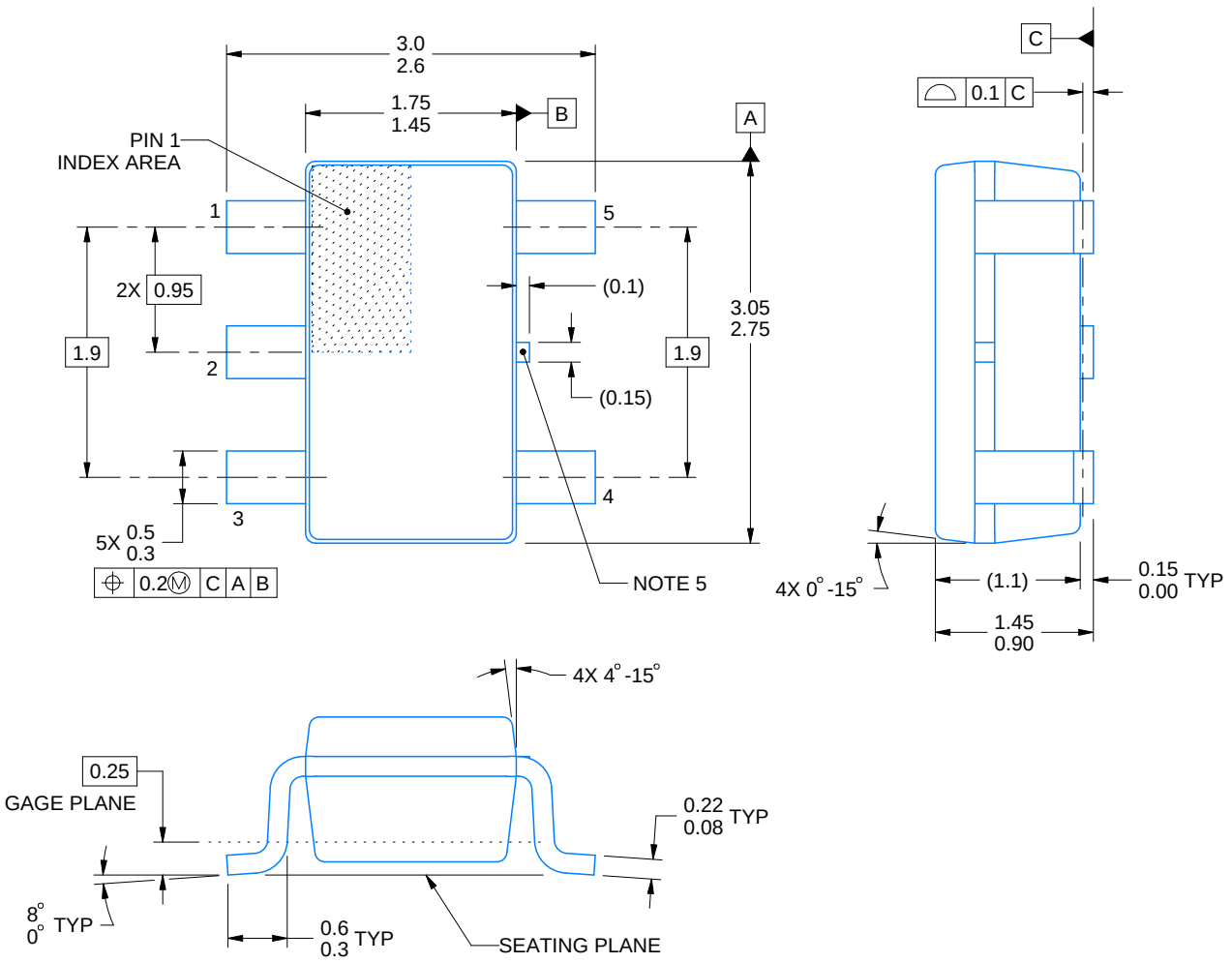
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLV3202AID	D	SOIC	8	50	507	8	3940	4.32
TLV3202AID	D	SOIC	8	50	506.6	8	3940	4.32
TLV3202AID.B	D	SOIC	8	50	506.6	8	3940	4.32
TLV3202AID.B	D	SOIC	8	50	507	8	3940	4.32
TLV3202AIDGK	DGK	VSSOP	8	80	330	6.55	500	2.88
TLV3202AIDGK.B	DGK	VSSOP	8	80	330	6.55	500	2.88

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

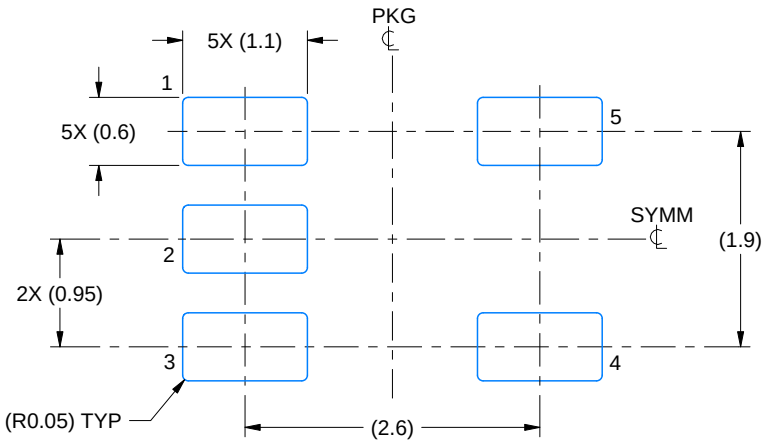
SMALL OUTLINE TRANSISTOR



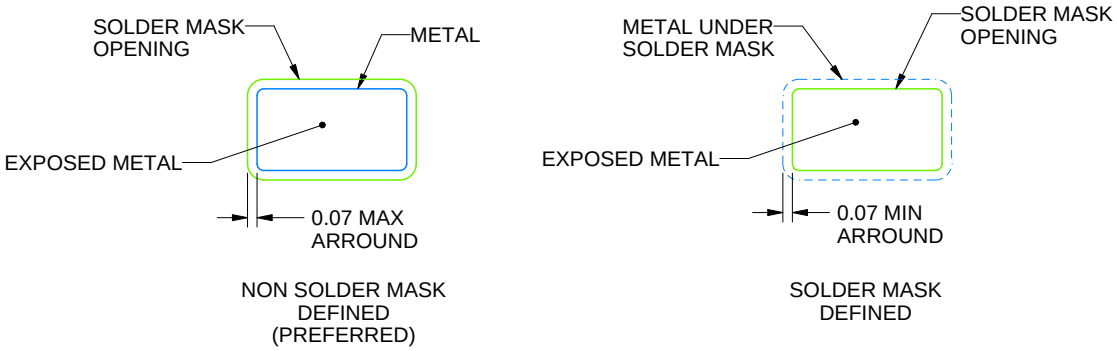
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

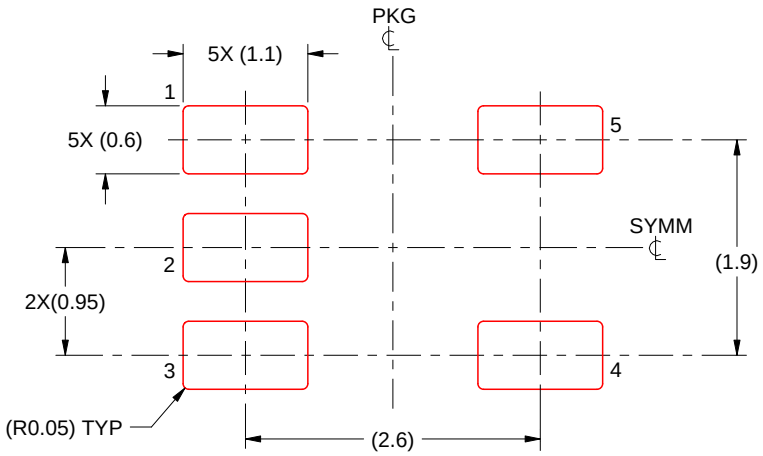


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

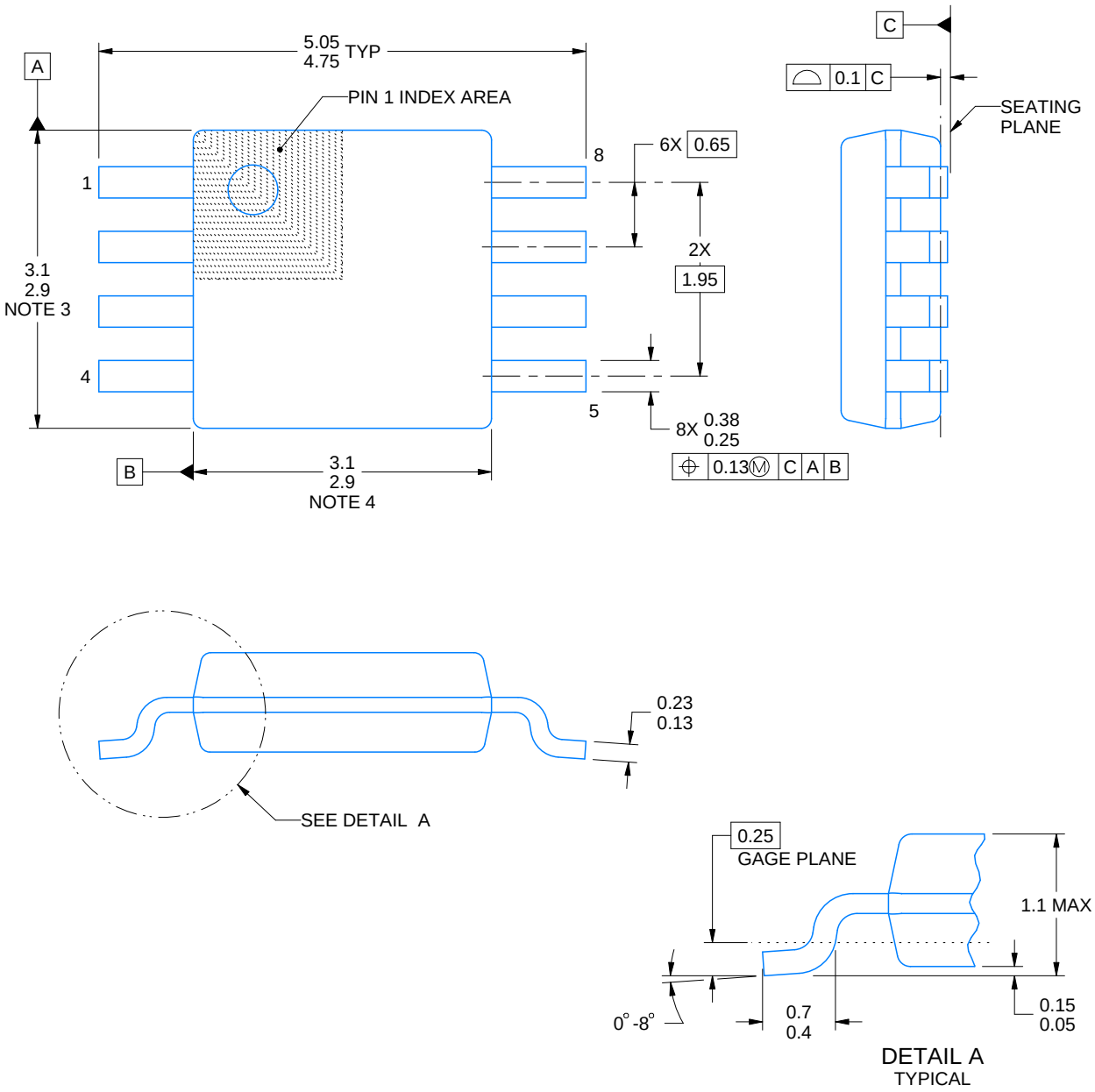
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

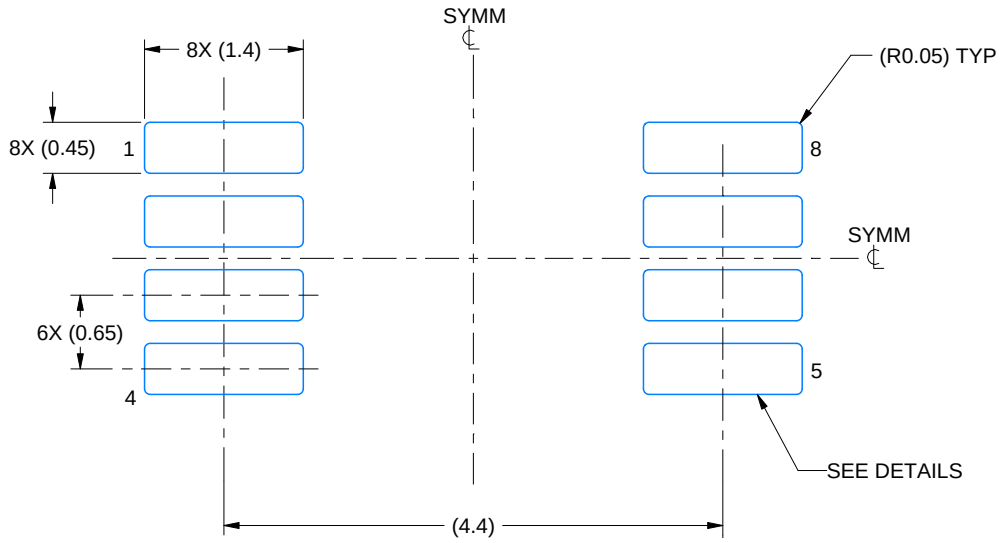
SMALL OUTLINE PACKAGE



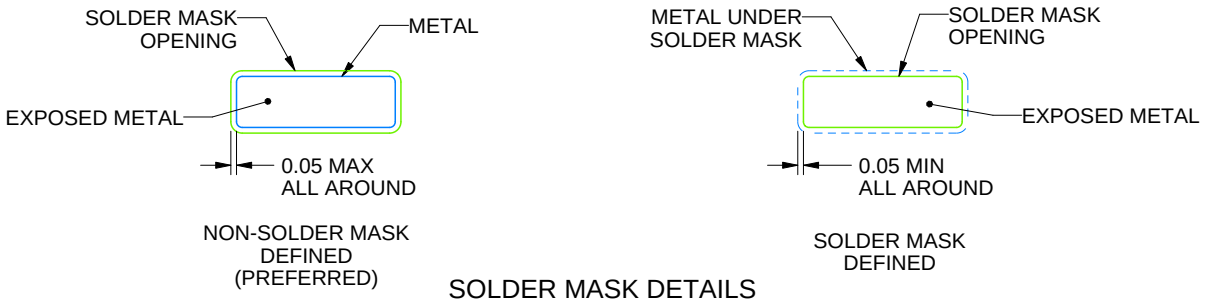
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

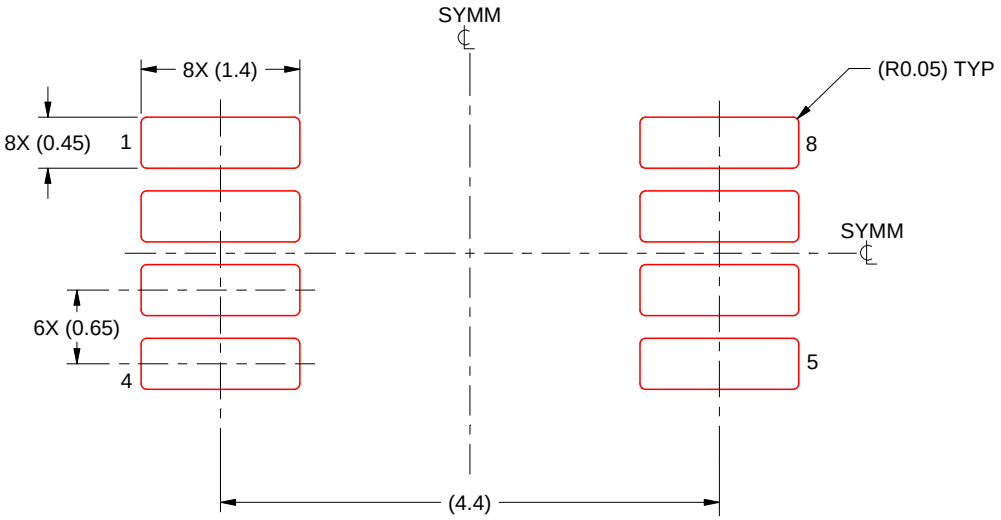


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

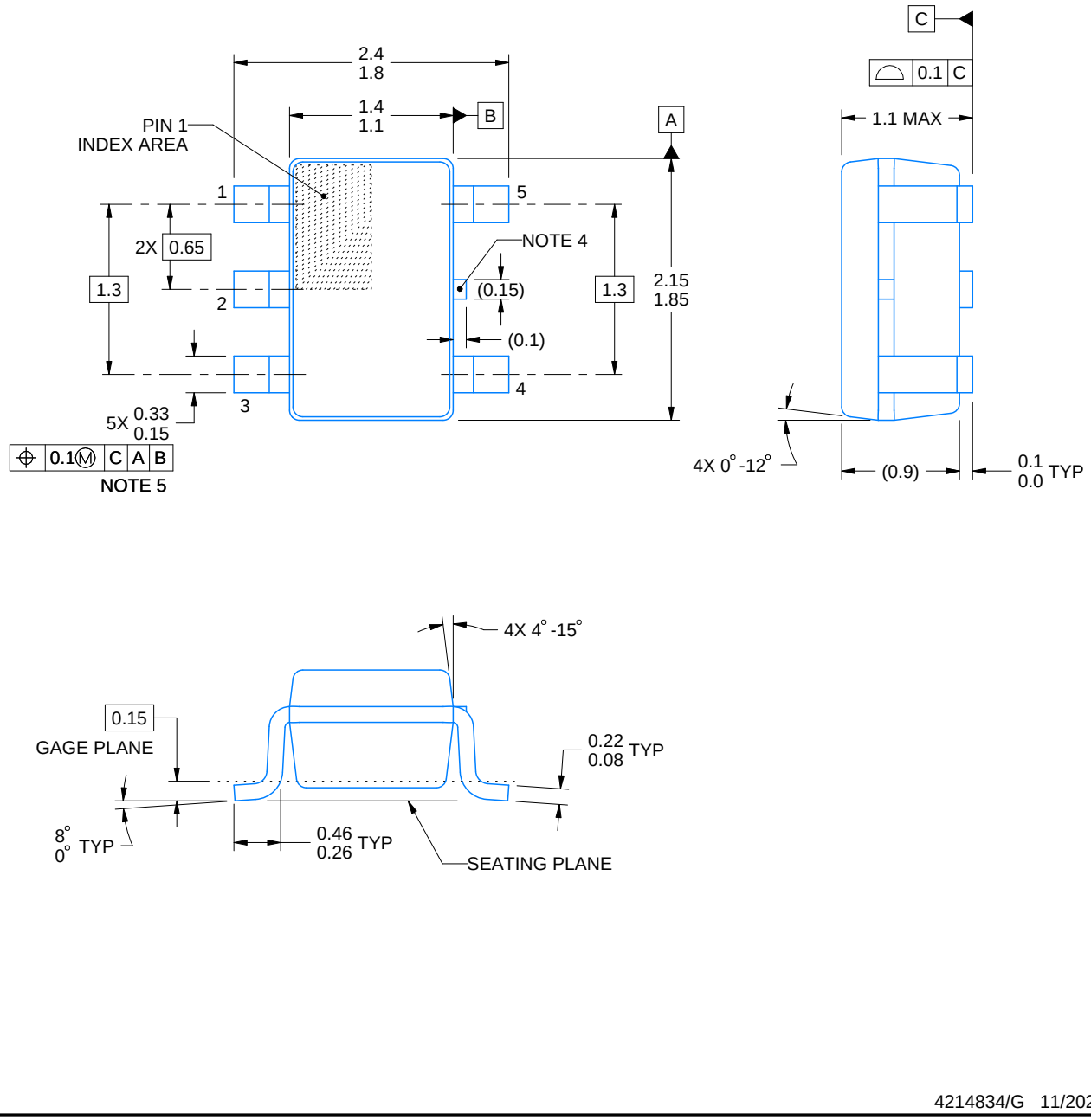
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

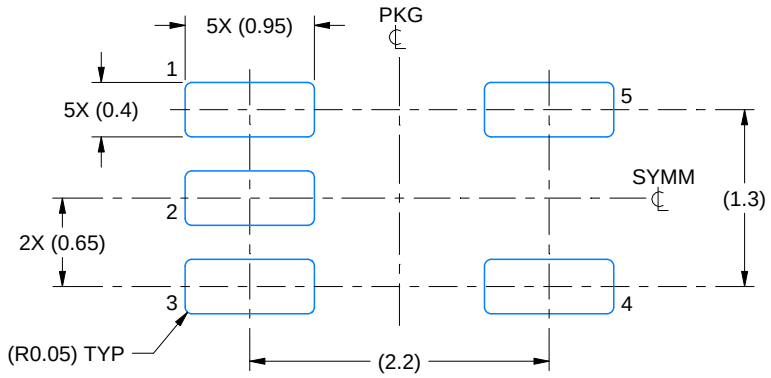
SMALL OUTLINE TRANSISTOR



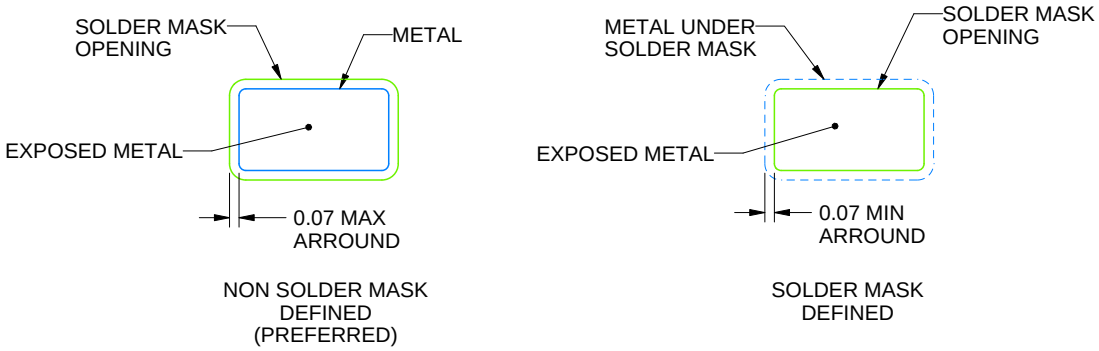
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

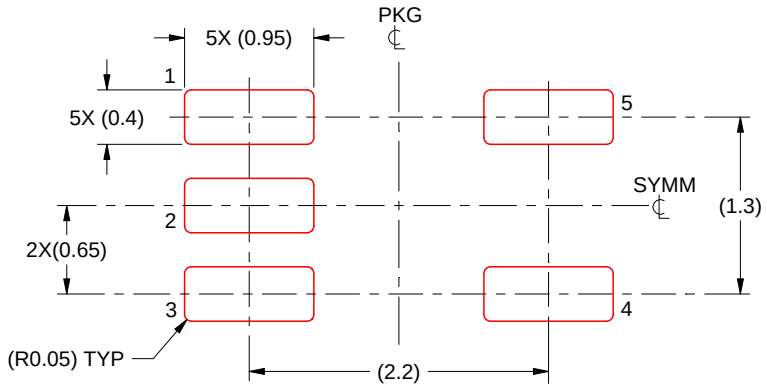


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

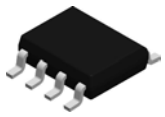


SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

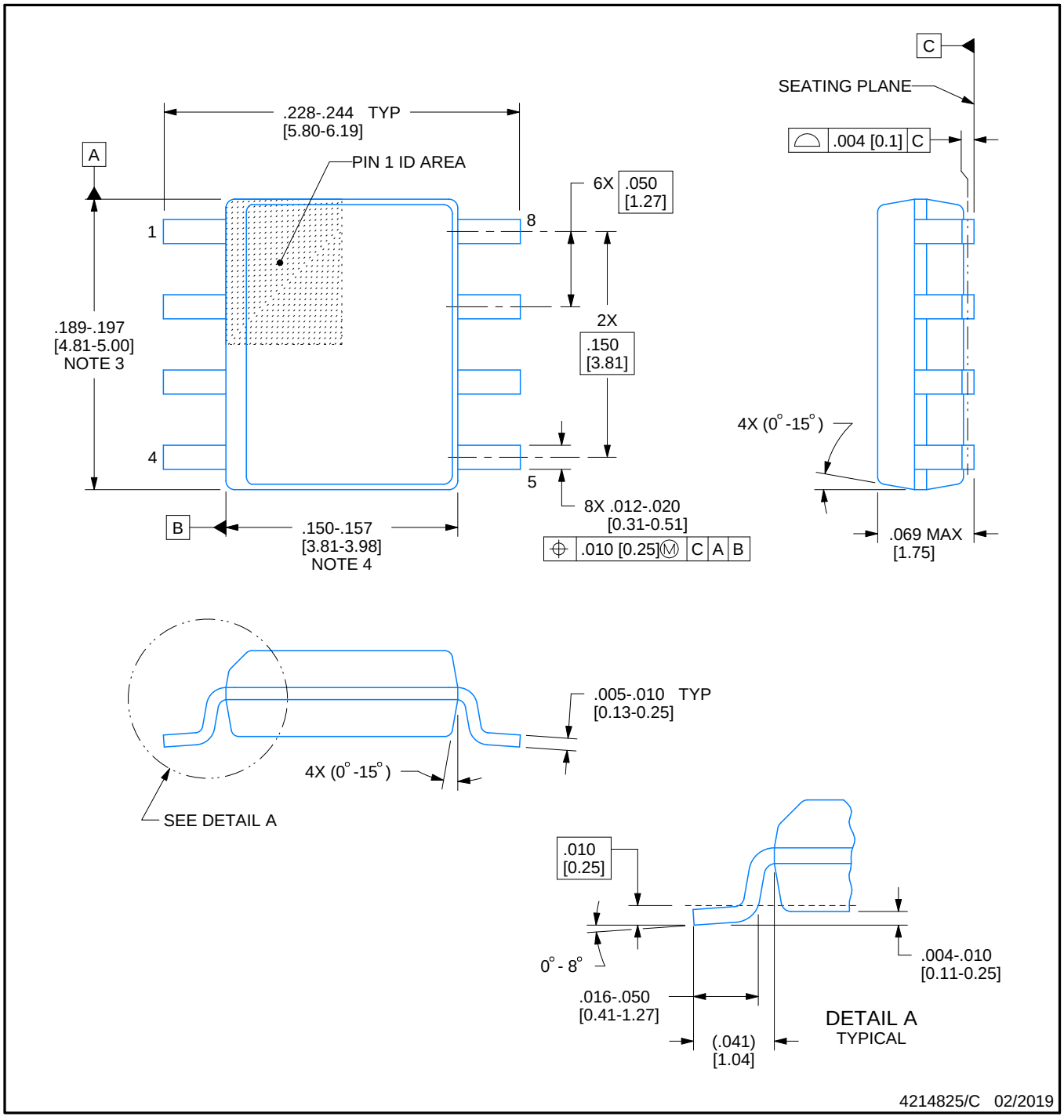


PACKAGE OUTLINE

D0008A

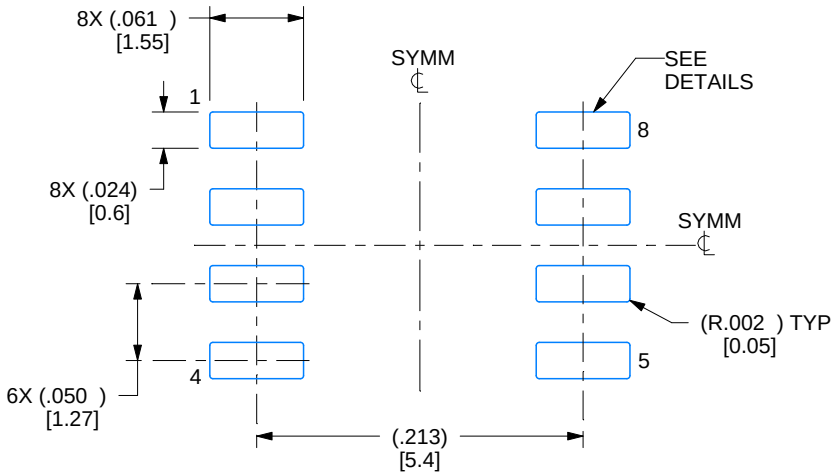
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

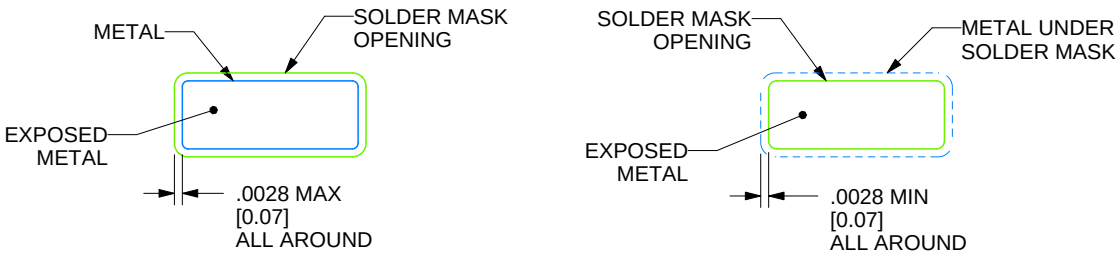


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

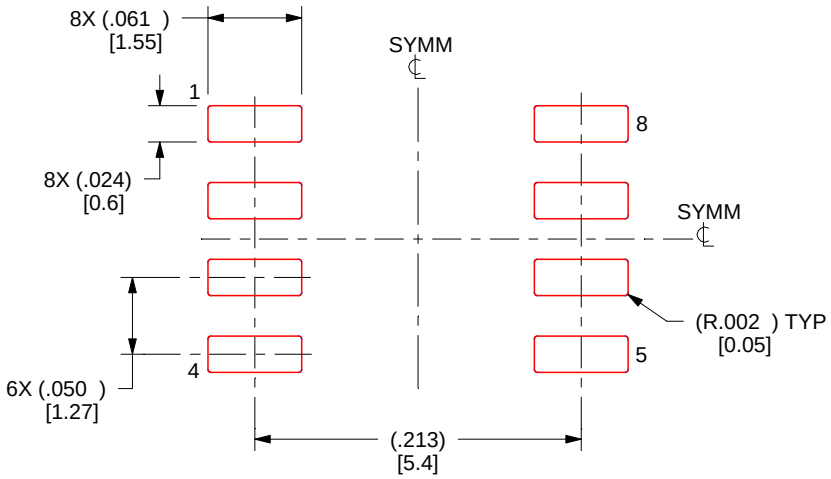
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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