8-CHANNEL, 12-/10-/8-BIT, 2.7-V TO 5.5-V LOW POWER DIGITAL-TO-ANALOG CONVERTER WITH POWER DOWN

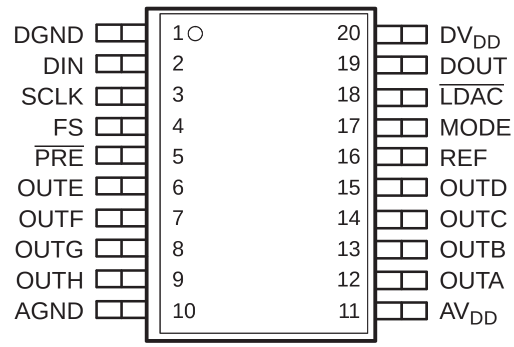
FEATURES

- **Eight Voltage Output DACs in One Package**
  - **TLV5610 . . . 12-Bit**
  - **TLV5608 . . . 10-Bit**
  - **TLV5629 . . . 8-Bit**
- **Programmable Settling Time vs Power Consumption**
  - **1 µs In Fast Mode**
  - **3 µs In Slow Mode**
- **Compatible With TMS320 and SPI™ Serial Ports**
- **Monotonic Over Temperature**
- **Low Power Consumption:**
  - **18 mW In Slow Mode at 3-V**
  - **48 mW In Fast Mode at 3-V**
- **Reference Input Buffers**
- **Power-Down Mode**
- **Buffered, High Impedance Reference Inputs**
- **Data Output for Daisy-Chaining**

APPLICATIONS

- **Digital Servo Control Loops**
- **Digital Offset and Gain Adjustment**
- **Industrial Process Control**
- **Machine and Motion Control Devices**
- **Mass Storage Devices**

DW OR PW PACKAGE
(TOP VIEW)



DESCRIPTION

The TLV5610, TLV5608, and TLV5629 are pin-compatible, eight-channel, 12-/10-/8-bit voltage output DACs each with a flexible serial interface. The serial interface allows glueless interface to TMS320 and SPI, QSPI, and Microwire serial ports. It is programmed with a 16-bit serial string containing 4 control and 12 data bits.

Additional features are a power-down mode, an LDAC input for simultaneous update of all eight DAC outputs, and a data output which can be used to cascade multiple devices.

The resistor string output voltage is buffered by a rail-to-rail output amplifier with a programmable settling time to allow the designer to optimize speed vs power dissipation. The buffered, high-impedance reference input can be connected to the supply voltage.

Implemented with a CMOS process, the DACs are designed for single-supply operation from 2.7 V to 5.5 V, and can operate on two separate analog and digital power supplies. The devices are available in 20-pin SOIC and TSSOP packages.

AVAILABLE OPTIONS

T_A	PACKAGE		
	SMALL OUTLINE (DW)	TSSOP (PW)	RESOLUTION
-40°C to 85°C	TLV5610IDW	TLV5610IPW	12
	TLV5608IDW	TLV5608IPW	10
	TLV5629IDW	TLV5629IPW	8

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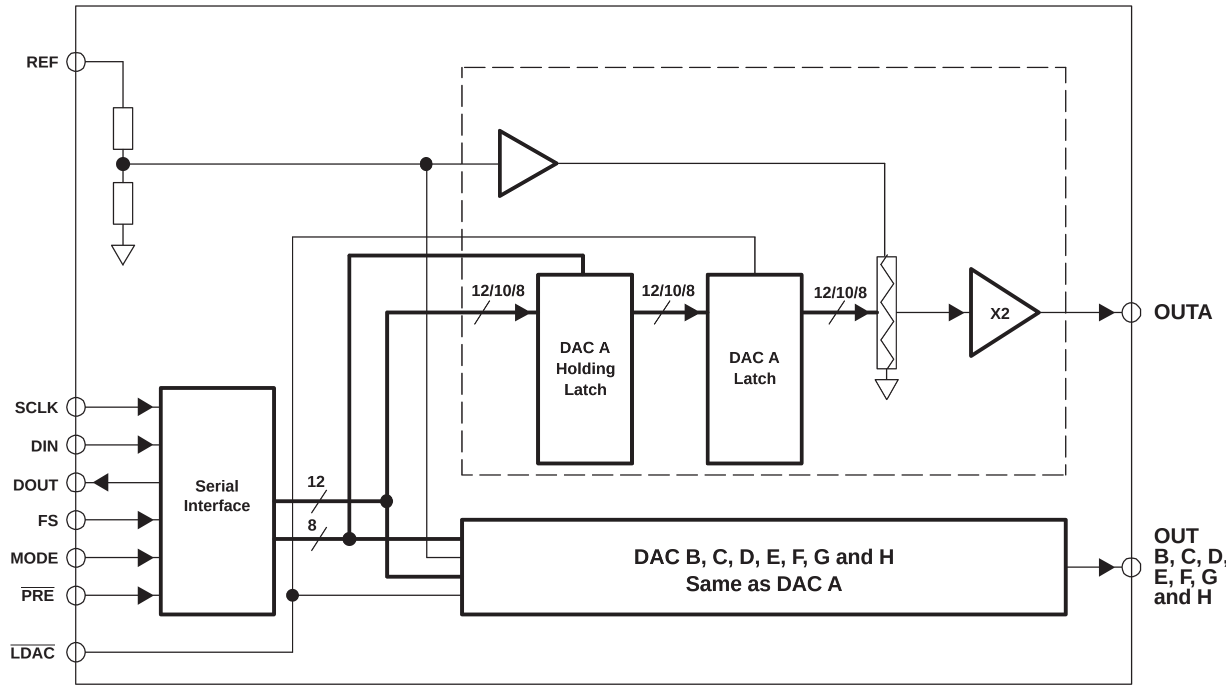
SPI is a trademark of Motorola, Inc.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FUNCTIONAL BLOCK DIAGRAM



Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AGND	10	I	Analog ground
AV_{DD}	11	I	Analog power supply
DGND	1	I	Digital ground
DIN	2	I	Digital serial data input
DOUT	19	O	Digital serial data output
DV_{DD}	20	I	Digital power supply
FS	4	I	Frame sync input
$\overline{\text{LDAC}}$	18	I	Load DAC. The DAC outputs are only updated, if this signal is low. It is an asynchronous input.
MODE	17	I	DSP/µC mode pin. High = µC mode, NC = DSP mode.
$\overline{\text{PRE}}$	5	I	Preset input
REF	16	I	Voltage reference input
SCLK	3	I	Serial clock input
OUTA-OUTH	6-9, 12-15	O	DAC outputs A, B, C, D, E, F, G and H

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

	UNIT
Supply voltage (AV_{DD}, DV_{DD} to GND)	7 V
Reference input voltage	- 0.3 V to AV_{DD} + 0.3 V
Digital input voltage range	- 0.3 V to DV_{DD} + 0.3 V
Operating free-air temperature range, T_A	-40°C to 85°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage, AV_{DD}, DV_{DD}	5-V operation	4.5	5	5.5	V
	3-V operation	2.7	3	3.3	V
High-level digital input voltage, V_{IH}	DV_{DD} = 2.7 V	2			V
	DV_{DD} = 5.5 V	2.4			
Low-level digital input voltage, V_{IL}	DV_{DD} = 2.7 V			0.6	V
	DV_{DD} = 5.5 V			1	
Reference voltage, V_{ref}	AV_{DD} = 5 V	GND	4.096	AV_{DD}	V
	AV_{DD} = 3 V	GND	2.048	AV_{DD}	V
Load resistance, R_L		2			kΩ
Load capacitance, C_L				100	pF
Clock frequency, f_{CLK}				30	MHz
Operating free-air temperature, T_A		-40		85	°C

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, supply voltages, and reference voltages (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY							
I_{DD}	Power supply current	Fast	No load, V_{ref} = 4.096 V, See (1) All inputs = DV_{DD} or GND		16	21	mA
		Slow			6	8	
	Power down supply current				0.1		µA
POR	Power on threshold				2		V
PSRR	Power supply rejection ratio		Full scale, See (2)		-60		dB

(1) I_{DD} is measured while continuously writing code 2048 to the DAC. For $V_{IH} < DV_{DD}$ - 0.7 V and V_{IL} > 0.7 V, supply current increases.
(2) Power supply rejection ratio at full scale is measured by varying AV_{DD} and is given by:
PSRR = 20 log [(E_G(AV_{DD}max) - E_G(AV_{DD}min))/V_{DD}max]

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating free-air temperature range, supply voltages, and reference voltages (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
STATIC DAC SPECIFICATIONS								
	Resolution	TLV5610				12		Bits
		TLV5608				10		
		TLV5629				8		
	Integral nonlinearity (INL)	TLV5610	V_{ref} = 2 V, 4V	Code 40 to 4095		±2	±6	LSB
		TLV5608		Code 20 to 1023		±0.5	±2	
		TLV5629		Code 6 to 255		±0.3	±1	
	Differential nonlinearity (DNL)	TLV5610	V_{ref} = 2 V, 4V	Code 40 to 4095		±0.5	±1	LSB
		TLV5608		Code 20 to 1023		±0.1	±1	
		TLV5629		Code 6 to 255		±0.1	±1	
E_{ZS}	Zero-scale error (offset error at zero scale)						±30	mV
E_{ZS} TC	Zero-scale-error temperature coefficient					30		µV/°C
E_G	Gain error						±0.6	% of FS voltage
E_G TC	Gain error temperature coefficient					10		ppm/°C
OUTPUT SPECIFICATIONS								
V_O	Voltage output range		R_L = 10 kΩ		0		AV_{DD} - 0.4	V
	Output load regulation accuracy		R_L = 2 kΩ vs 10 kΩ				±0.3	% of FS voltage
REFERENCE INPUT								
V_I	Reference input voltage				0		AV_{DD}	V
R_I	Reference input resistance					100		kΩ
C_I	Reference input capacitance					5		pF
	Reference input bandwidth	Fast	V_{ref} = 0.4 V_{pp} + 2.048 Vdc, Input code = 0x800			2.2		MHz
		Slow	V_{ref} = 2 V_{pp} at 1 kHz + 2.048 Vdc, See (3)			1.9		
	Reference feedthrough					-84		dB
DIGITAL INPUT								
I_{IH}	High-level digital input current		$V_I = V_{DD}$				1	µA
I_{IL}	Low-level digital input current		V_I = 0 V		-1			µA
C_I	Input capacitance					8		pF
DIGITAL OUTPUT								
V_{OH}	High-level digital output voltage		R_L = 10 kΩ		2.6			V
V_{OL}	Low-level digital output voltage		R_L = 10 kΩ				0.4	V
	Output voltage rise time		R_L = 10 kΩ, C_L = 20 pF, Includes propagation delay			7	20	ns

(3) Reference feedthrough is measured at the DAC output with an input code = 0x000.

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating free-air temperature range, supply voltages, and reference voltages (unless otherwise noted)

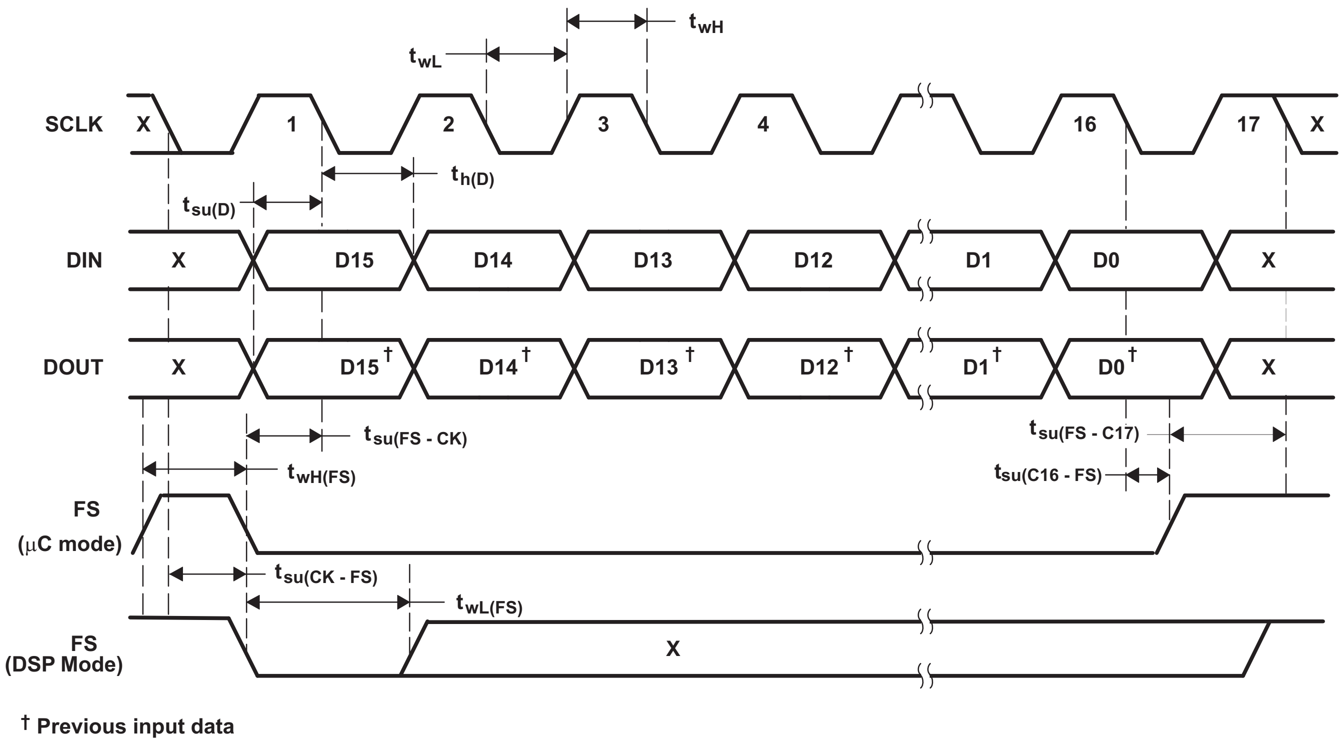
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG OUTPUT DYNAMIC PERFORMANCE							
$t_{s(FS)}$	Output settling time (full scale)	Fast	R_L = 10 kΩ, C_L = 100 pF, See (4)		1	3	µs
		Slow			3	7	
$t_{s(CC)}$	Output settling time, code to code	Fast	R_L = 10 kΩ, C_L = 100 pF, See (5)		0.5	1	µs
		Slow			1	2	
SR	Slew rate	Fast	R_L = 10 kΩ, C_L = 100 pF, See (6)	4	10		V/µs
		Slow		1	3		
	Glitch energy		See (7)		4		nV-s
	Channel crosstalk		10 kHz sine, 4 V_{PP}		-90		dB

(4) Settling time is the time for the output signal to remain within +0.5 LSB of the final measured value for a digital input code change of 0x80 to 0xFFF and 0xFFF to 0x080, respectively. Assured by design; not tested.
(5) Settling time is the time for the output signal to remain within +0.5 LSB of the final measured value for a digital input code change of one count. The max time applies to code changes near zero scale or full scale. Assured by design; not tested.
(6) Slew rate determines the time it takes for a change of the DAC output from 10% to 90% full scale voltage.
(7) Code transition: TLV5610 - 0x7FF to 0x800, TLV5608 - 0x7FC to 0x800, TLV5629 - 0x7F0 to 0x800

TIMING REQUIREMENTS

DIGITAL INPUTS					
		MIN	NOM	MAX	UNIT
$t_{su(FS-CK)}$	Setup time, FS low before next negative SCLK edge	8			ns
$t_{su(C16-FS)}$	Setup time, 16th negative edge after FS low on which bit D0 is sampled before rising edge of FS. µC mode only	10			ns
$t_{su(FS-C17)}$	µC mode, setup time, FS high before 17th negative edge of SCLK.	10			ns
$t_{su(CK-FS)}$	DSP mode, setup time, SLCK low before FS low.	5			ns
$t_{wL(LDAC)}$	$\overline{\text{LDAC}}$ duration low	10			ns
t_{wH}	SCLK pulse duration high	16			ns
t_{wL}	SCLK pulse duration low	16			ns
$t_{su(D)}$	Setup time, data ready before SCLK falling edge	8			ns
$t_{h(D)}$	Hold time, data held valid after SCLK falling edge	5			ns
$t_{wH(FS)}$	FS duration high	10			ns
$t_{wL(FS)}$	FS duration low	10			ns
t_s	Settling time	See AC specs			

PARAMETER MEASUREMENT INFORMATION



† Previous input data

Figure 1. Serial Interface Timing

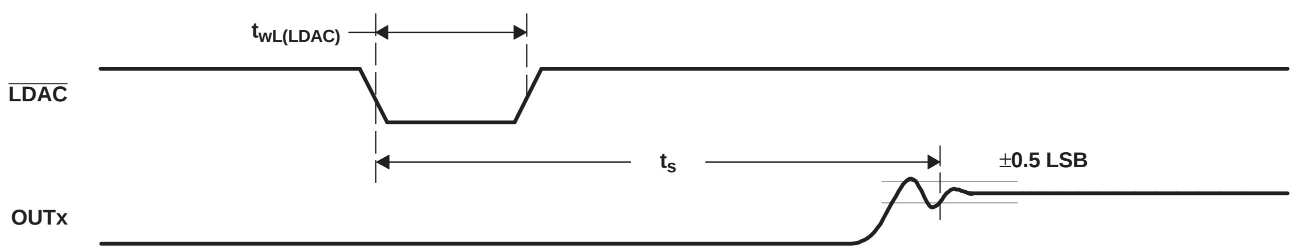


Figure 2. Output Timing

TYPICAL CHARACTERISTICS

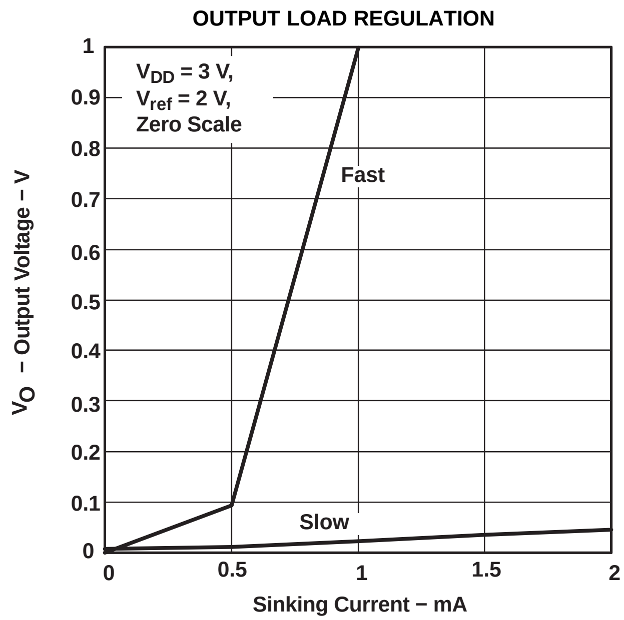


Figure 3.

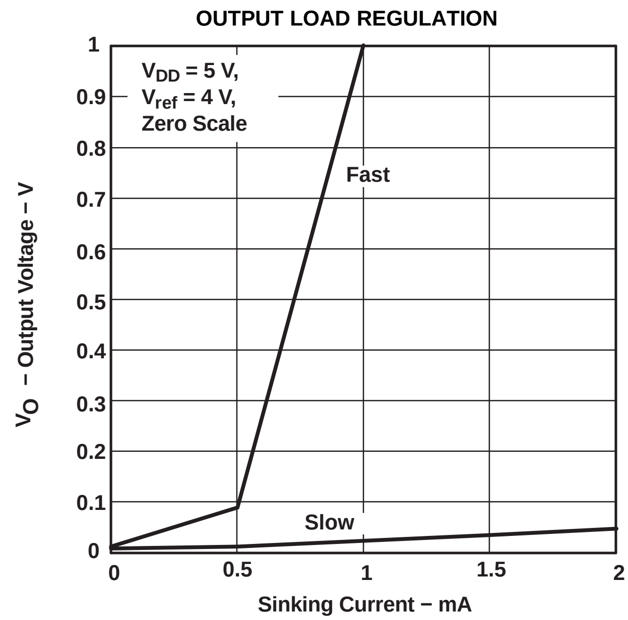


Figure 4.

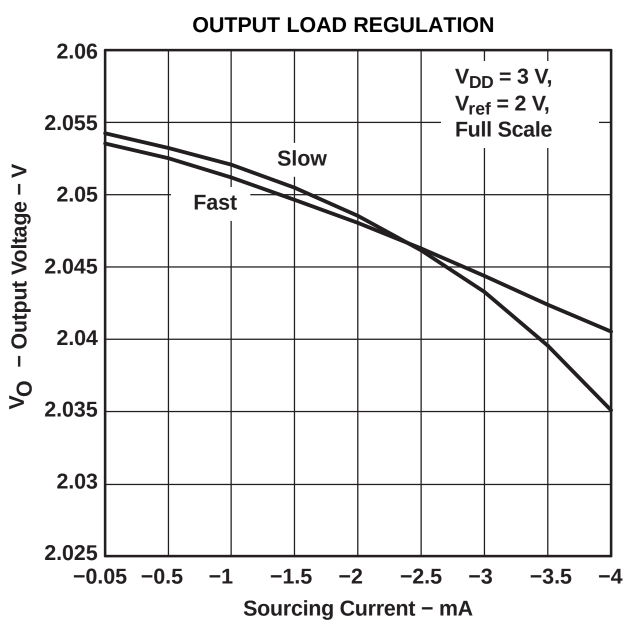


Figure 5.

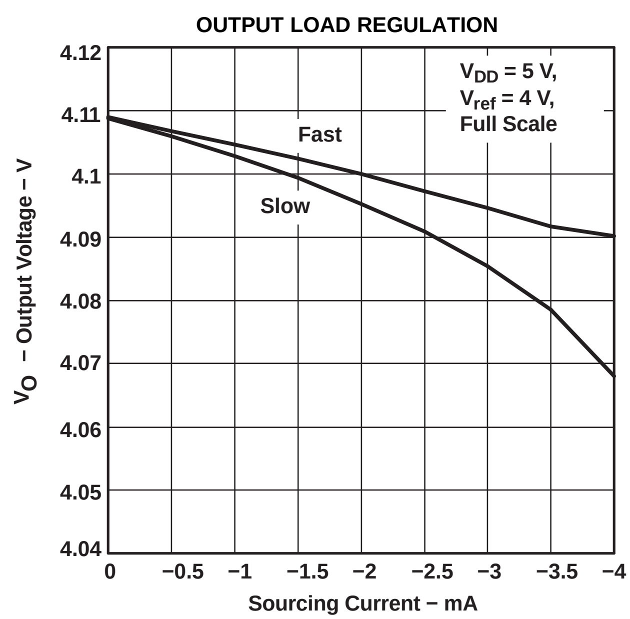


Figure 6.

TYPICAL CHARACTERISTICS (continued)

TLV5610
INTEGRAL NONLINEARITY
vs
CODE

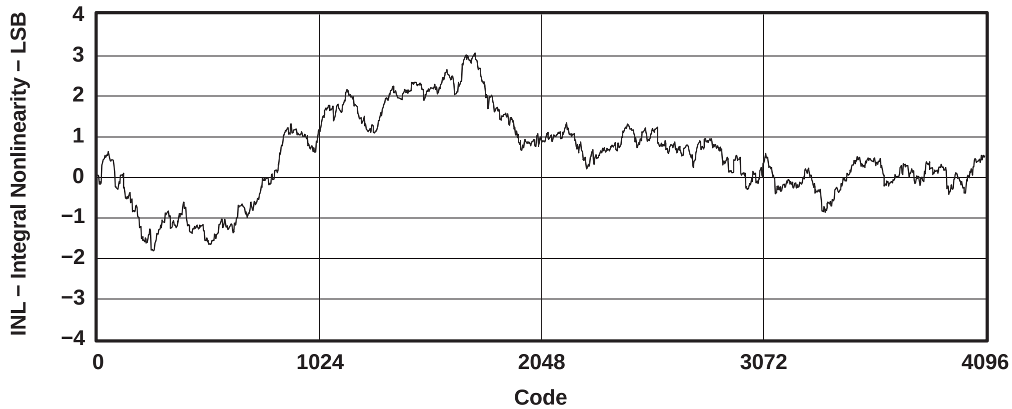


Figure 7.

TLV5610
DIFFERENTIAL NONLINEARITY
vs
CODE

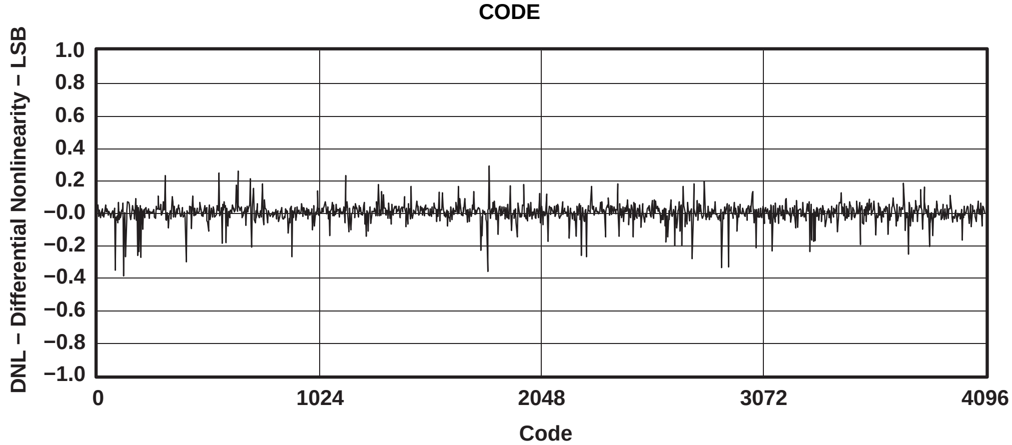


Figure 8.

TYPICAL CHARACTERISTICS (continued)

TLV5608
INTEGRAL NONLINEARITY
vs
CODE

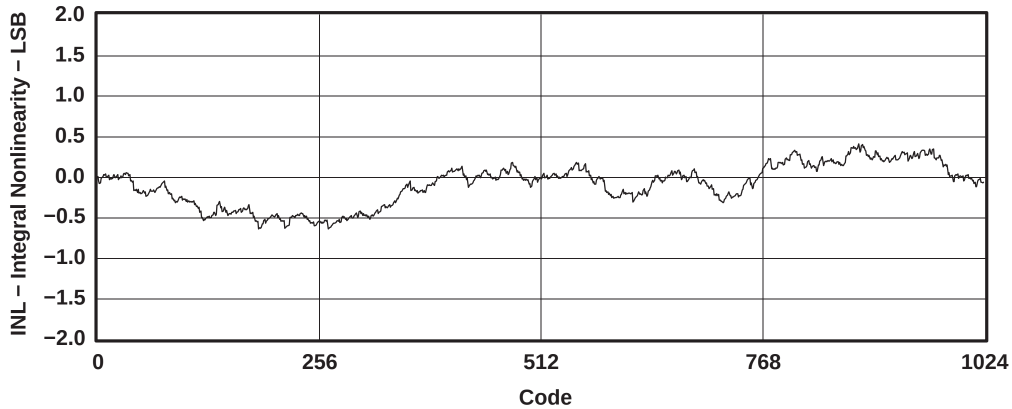


Figure 9.

TLV5608
DIFFERENTIAL NONLINEARITY
vs
CODE

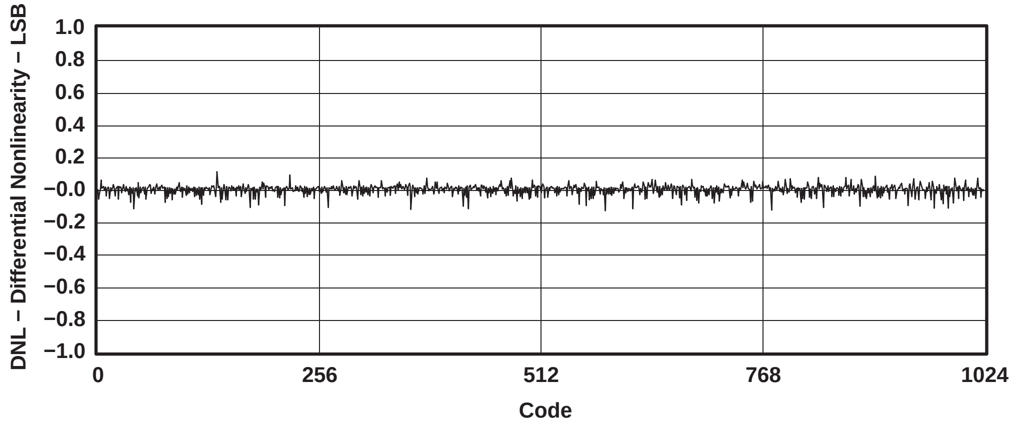


Figure 10.

TYPICAL CHARACTERISTICS (continued)

TLV5629
INTEGRAL NONLINEARITY
vs
CODE

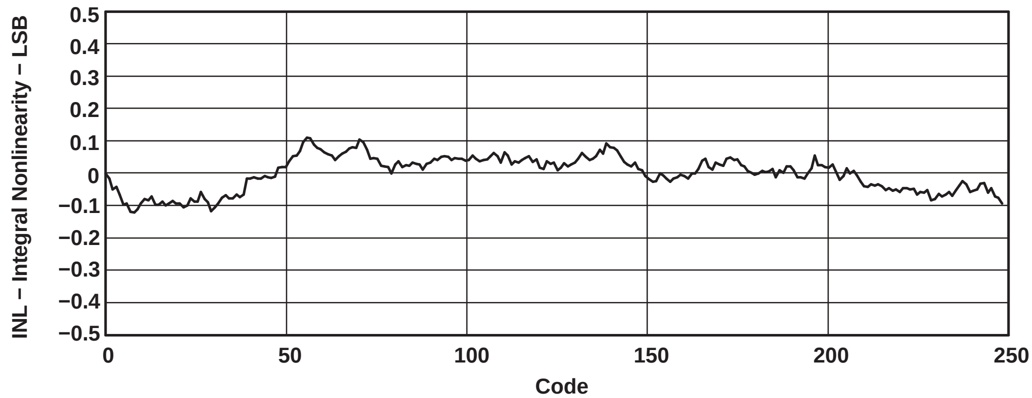


Figure 11.

TLV5629
DIFFERENTIAL NONLINEARITY
vs
CODE

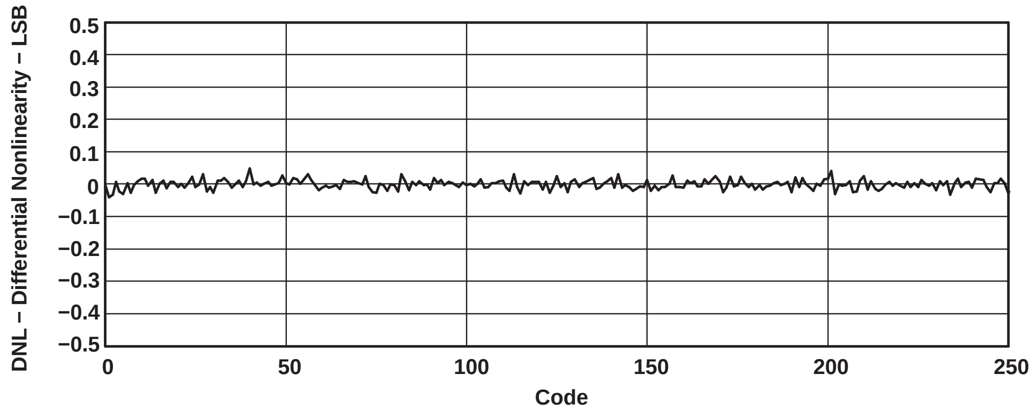


Figure 12.

APPLICATION INFORMATION

GENERAL FUNCTION

The TLV5610, TLV5608, and TLV5629 are 8-channel, 12-bit, single-supply DACs, based on a resistor string architecture. They consist of a serial interface, a speed and power-down control logic, a reference input buffer, a resistor string, and a rail-to-rail output buffer.

The output voltage (full scale determined by external reference) for each channel is given by:

$$\text{REF} \; \frac{\text{CODE}}{\text{0x1000}} \; [\text{V}] \tag{1}$$

where REF is the reference voltage and CODE is the digital input value. The input range is 0x000 to 0xFFF for the TLV5610, 0x000 to 0xFFC for the TLV5608, and 0x000 to 0xFF0 for the TLV5629.

POWER ON RESET (POR)

The built-in power-on-reset circuit controls the output voltage after power up. On power up, all latches including the preset register are set to zero, but the DAC outputs are only set to zero if the $\overline{\text{LDAC}}$ is low. The DAC outputs may have a small offset error produced by the output buffer. The registers remains at zero until a valid write sequence is made to the DAC, changing the DAC register data. This is useful in applications where it is important to know the state of the outputs of the DAC after power up. All digital inputs must be logic low until the digital and analog supplies are applied. Any logic high voltages applied to the logic input pins when power is not applied to AV_{DD} and DV_{DD}, may power the device logic circuit through the overvoltage protection diode causing an undesired operation. When separate analog (AV_{DD}) and digital (DV_{DD}) supplies are used, AV_{DD} must come up first before DV_{DD}, to ensure that the power-on-reset circuit operates correctly.

SERIAL INTERFACE

A falling edge of FS starts shifting the data on DIN starting with the MSB to the internal register on the falling edges of SCLK. After 16 bits have been transferred, the content of the shift register is moved to one of the DAC holding registers, depending on the address bits within the data word. A logic 0 on the $\overline{\text{LDAC}}$ pin is required to transfer the content of the DAC holding register to the DAC latch and to update the DAC outputs. $\overline{\text{LDAC}}$ is an asynchronous input. It can be held low if a simultaneous update of all eight channels is not needed.

For daisy-chaining, DOUT provides the data sampled on DIN with a delay of 16 clock cycles.

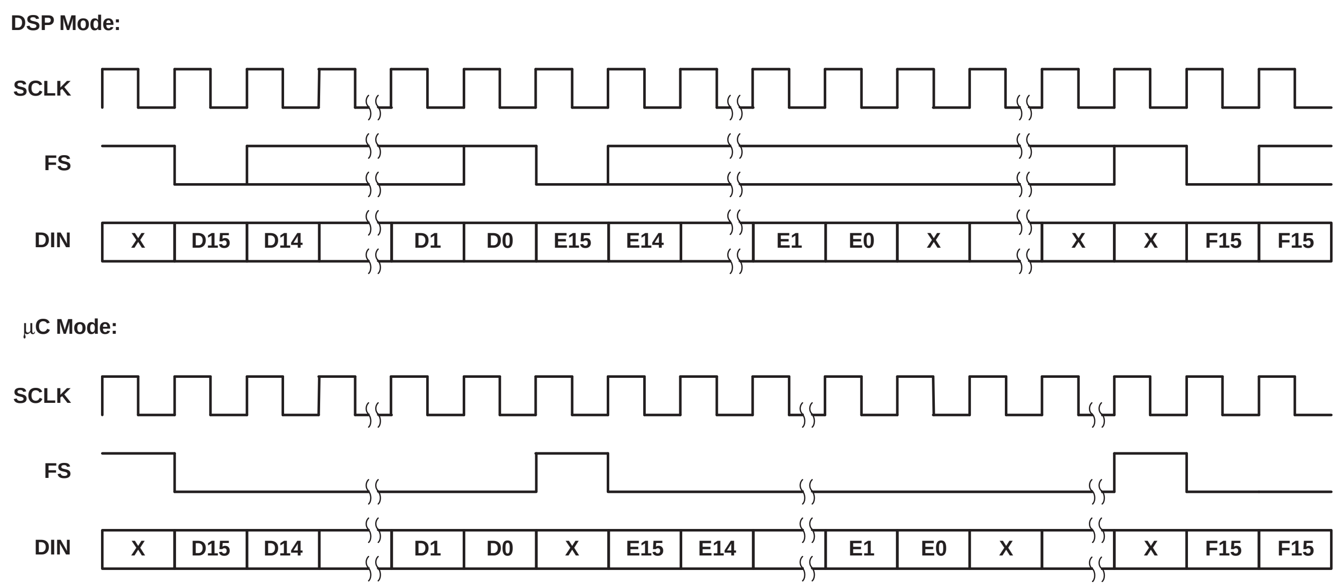


Figure 13. Data Sampled on DIN

Difference between DSP mode (MODE = N.C. or 0) and µC (MODE = 1) mode:

- In µC mode, FS needs to be held low until all 16 data bits have been transferred. If FS is driven high before the 16th falling clock edge, the data transfer is cancelled. The DAC is updated after a rising edge on FS.
- In DSP mode, FS needs to stay low for 20 ns and can go high before the 16th falling clock edge.
- In DSP mode there needs to be one falling SCLK edge before FS goes low to start the write (DIN) cycle. This extra falling SCLK edge has to happen at least 5 ns before FS goes low, $t_{su(CK\text{-}FS)} \geq 5$ ns.
- In µC mode, the extra falling SCLK edge is not necessary. However, if it does happen, the extra negative SCLK edge is not allowed to occur within 10 ns after FS goes HIGH to finish the WRITE cycle ($t_{su(FS\text{-}C17)}$).

SERIAL CLOCK FREQUENCY AND UPDATE RATE

The maximum serial clock frequency is given by:

$$f_{sclkmax} = \frac{1}{t_{whmin} + t_{wlmin}} = 30\text{ MHz} \tag{2}$$

The maximum update rate is:

$$f_{updatemax} = \frac{1}{16\left(t_{whmin} + t_{wlmin}\right)} = 1.95\text{ MHz} \tag{3}$$

Note, that the maximum update rate is just a theoretical value for the serial interface, as the settling time of the DAC has to be considered also.

DATA FORMAT

The 16-bit data word consists of two parts:

- Address bits (D150D12)
- Data bits (D110D0)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
A3	A2	A1	A0	DATA											

Register Map

A3	A2	A1	A0	FUNCTION
0	0	0	0	DAC A
0	0	0	1	DAC B
0	0	1	0	DAC C
0	0	1	1	DAC D
0	1	0	0	DAC E
0	1	0	1	DAC F
0	1	1	0	DAC G
0	1	1	1	DAC H
1	0	0	0	CTRL0
1	0	0	1	CTRL1
1	0	1	0	Preset
1	0	1	1	Reserved
1	1	0	0	DAC A and $\overline{B}$
1	1	0	1	DAC C and $\overline{D}$
1	1	1	0	DAC E and $\overline{F}$
1	1	1	1	DAC G and $\overline{H}$

DAC A-H AND TWO-CHANNEL REGISTERS

Writing to DAC A-H sets the output voltage of channel A-H. It is possible to automatically generate the complement of one channel by writing to one of the four two-channel registers (DAC A and B etc.).

The TLV5610 decodes all 12 data bits. The TLV5608 decodes D11 to D2 (D1 and D0 are ignored). The TLV5629 decodes D11 to D4 (D3 to D0 are ignored).

PRESET

The outputs of the DAC channels can be driven simultaneously to a predefined value stored in the preset register by driving the $\overline{\text{PRE}}$ input pin low and asserting the $\overline{\text{LDAC}}$ input pin. The preset register is cleared (set to zero) by the POR circuit after power up. Therefore, it must be written with a predefined value before asserting the $\overline{\text{PRE}}$ pin low, unless zero is the desired preset value. The $\overline{\text{PRE}}$ input is asynchronous to the clock.

CTRL0

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	PD	DO	X	X	IM

PD	: Full device power down	0 = normal	1 = power down
DO	: Digital output enable	0 = disable	1 = enable
IM	: Input mode	0 = straight binary	1 = twos complement
X	: Reserved		

If DOUT is enabled, the data input on DIN is output on DOUT with a 16-cycle delay. That makes it possible to daisy-chain multiple DACs on one serial bus.

CTRL1

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	P_{GH}	P_{EF}	P_{CD}	P_{AB}	S_{GH}	S_{EF}	S_{CD}	S_{AB}

P_{XY}	: Power down DAC_{XY}	0 = normal	1 = power down
S_{XY}	: Speed DAC_{XY}	0 = slow	1 = fast
XY	: DAC pair AB, CD, EF, or GH		

In power-down mode, the amplifiers of the selected DAC pair within the device are disabled and the total power consumption of the device is significantly reduced. Power-down mode of a specific DAC pair can be selected by setting the PXY bit within the data word to 1.

There are two settling time modes: fast and slow. Fast mode of a DAC pair is selected by setting S_{XY} to 1 and slow mode is selected by setting S_{XY} to 0.

REFERENCE

The DAC reference can be sourced externally using precision reference circuits. Since the reference input is buffered, it can be connected to the supply voltage.

BUFFERED AMPLIFIER

The DAC outputs are buffered by an amplifier with a gain of two, which are configurable as Class A (fast mode) or Class AB (slow or low-power mode). The output buffers have near rail-to-rail output with short-circuit protection, and can reliably drive a 2-kΩ load with a 100-pF load capacitance.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV5608IDW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLV5608I	Samples
TLV5608IDWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLV5608I	Samples
TLV5608IPW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY5608	Samples
TLV5608IPWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY5608	Samples
TLV5608IPWRG4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY5608	Samples
TLV5610IDW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLV5610I	Samples
TLV5610IDWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLV5610I	Samples
TLV5610IPW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY5610	Samples
TLV5610IPWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY5610	Samples
TLV5629IDW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLV5629I	Samples
TLV5629IDWG4	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLV5629I	Samples
TLV5629IDWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLV5629I	Samples
TLV5629IPW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY5629	Samples
TLV5629IPWG4	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY5629	Samples
TLV5629IPWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY5629	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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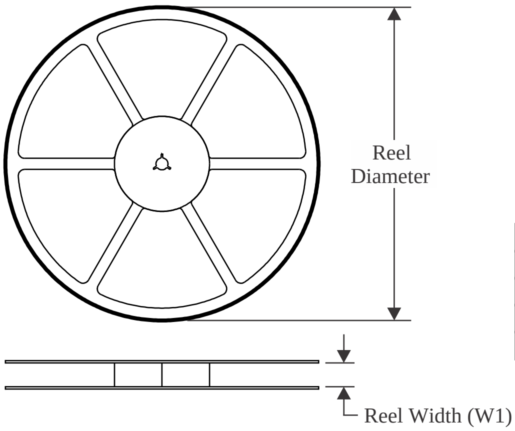
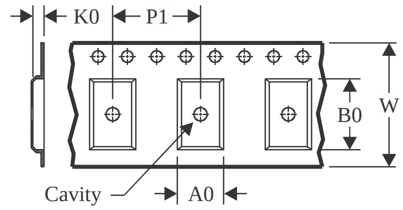
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

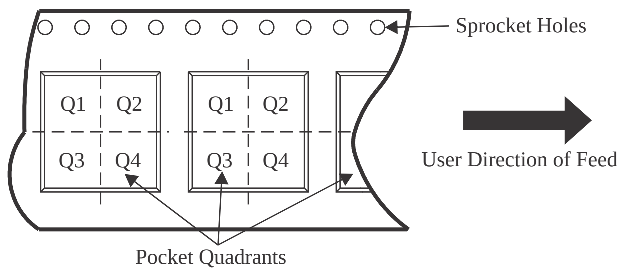


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

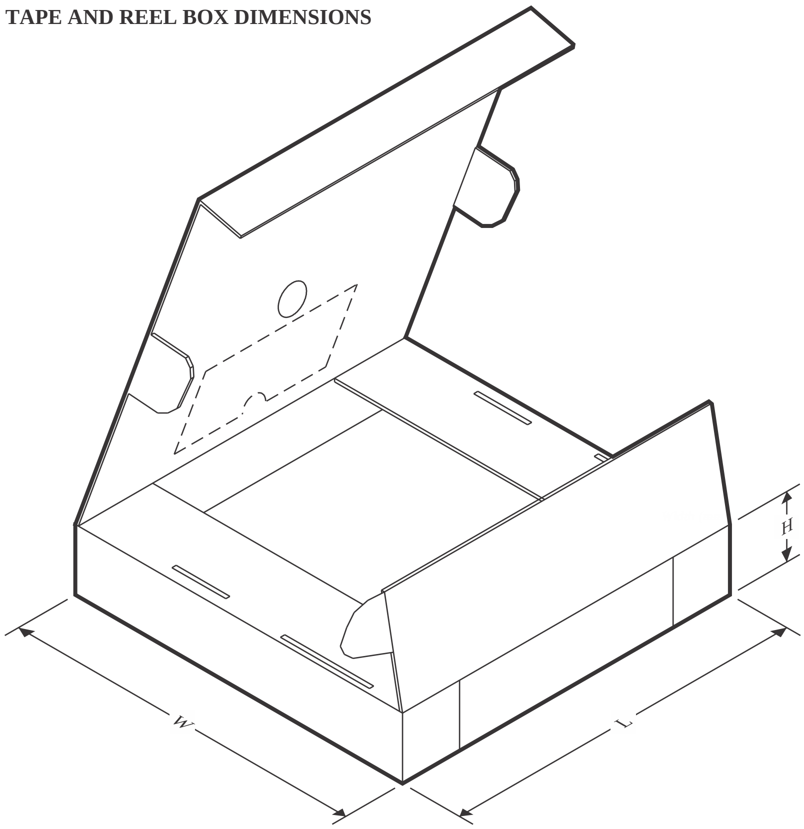
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV5608IDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
TLV5608IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TLV5610IDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
TLV5610IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TLV5629IDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
TLV5629IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

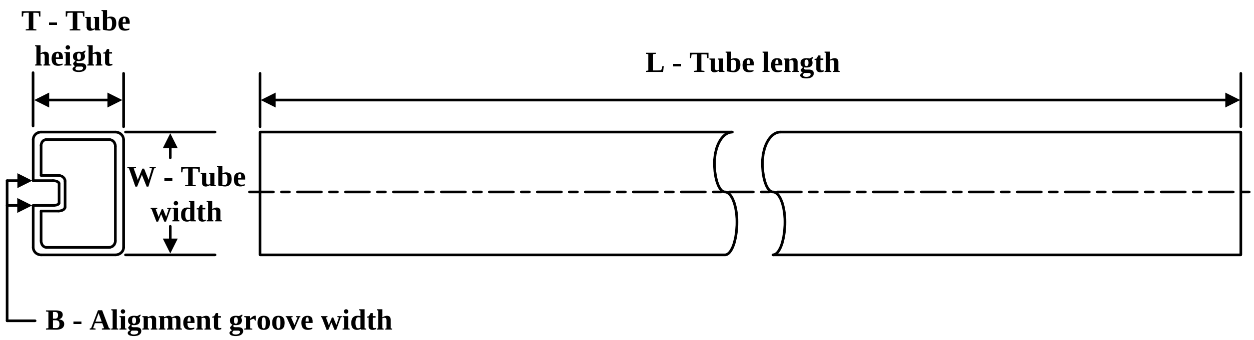
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

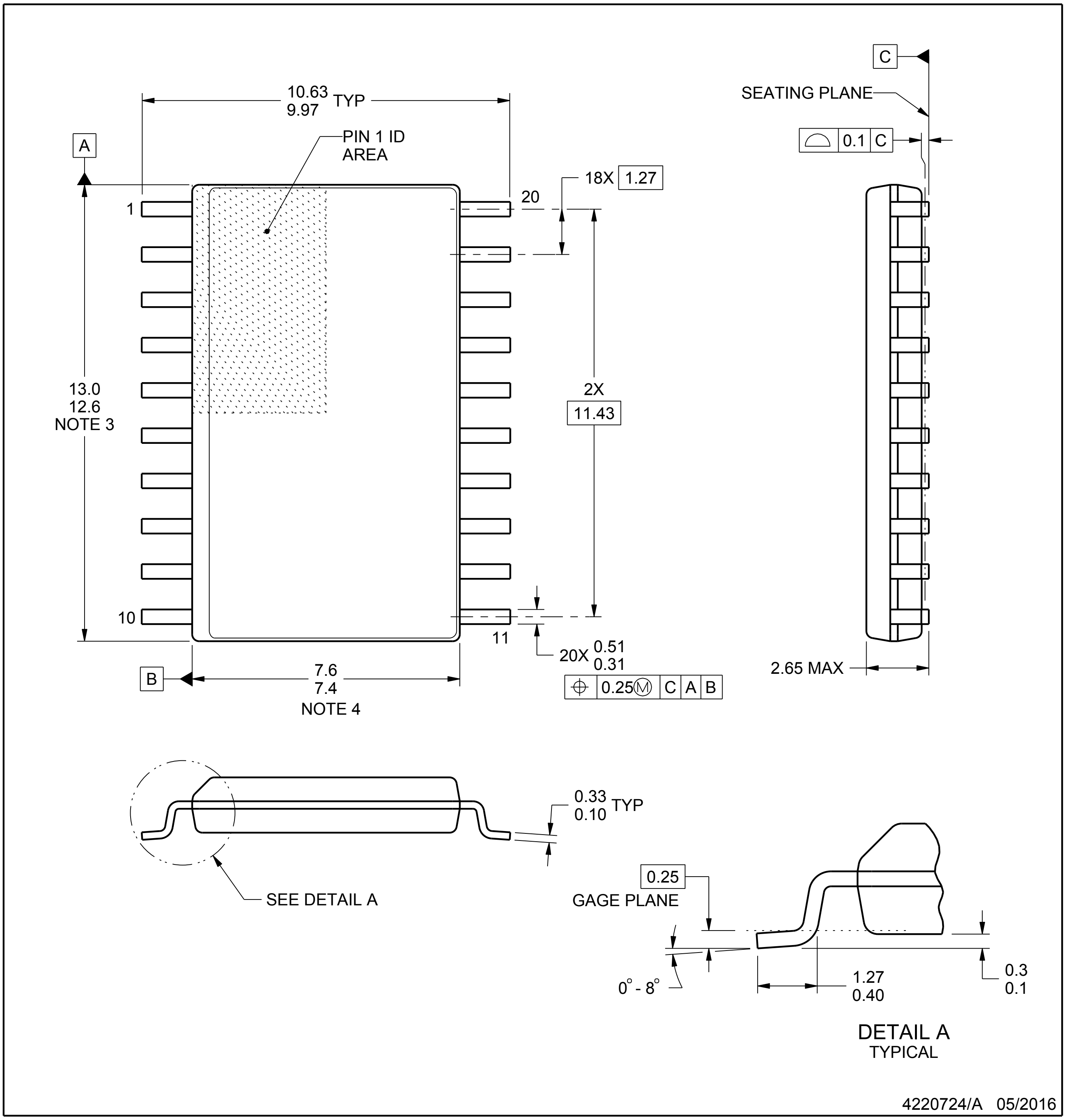
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV5608IDWR	SOIC	DW	20	2000	350.0	350.0	43.0
TLV5608IPWR	TSSOP	PW	20	2000	350.0	350.0	43.0
TLV5610IDWR	SOIC	DW	20	2000	350.0	350.0	43.0
TLV5610IPWR	TSSOP	PW	20	2000	350.0	350.0	43.0
TLV5629IDWR	SOIC	DW	20	2000	350.0	350.0	43.0
TLV5629IPWR	TSSOP	PW	20	2000	350.0	350.0	43.0

TUBE



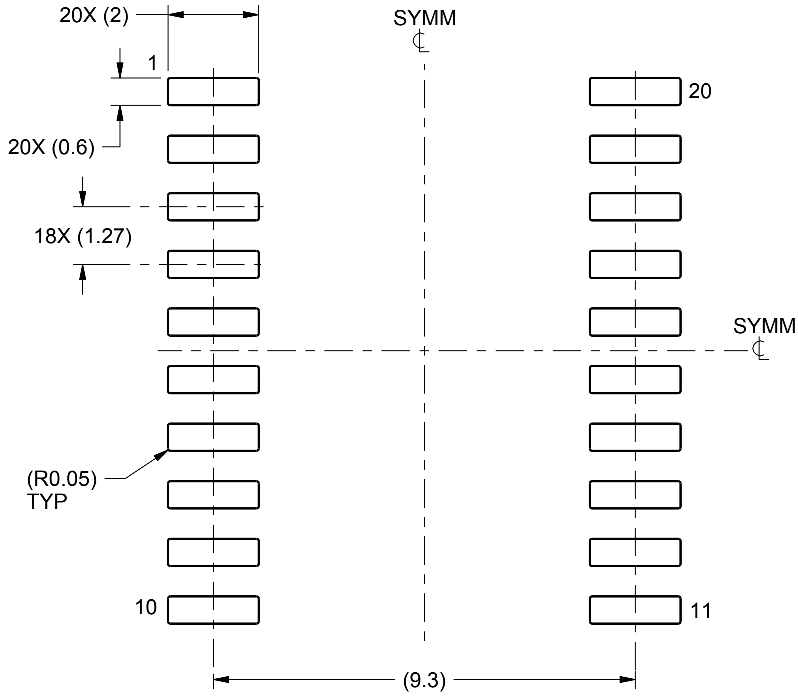
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLV5608IDW	DW	SOIC	20	25	506.98	12.7	4826	6.6
TLV5608IPW	PW	TSSOP	20	70	530	10.2	3600	3.5
TLV5610IDW	DW	SOIC	20	25	506.98	12.7	4826	6.6
TLV5610IPW	PW	TSSOP	20	70	530	10.2	3600	3.5
TLV5629IDW	DW	SOIC	20	25	506.98	12.7	4826	6.6
TLV5629IDWG4	DW	SOIC	20	25	506.98	12.7	4826	6.6
TLV5629IPW	PW	TSSOP	20	70	530	10.2	3600	3.5
TLV5629IPWG4	PW	TSSOP	20	70	530	10.2	3600	3.5

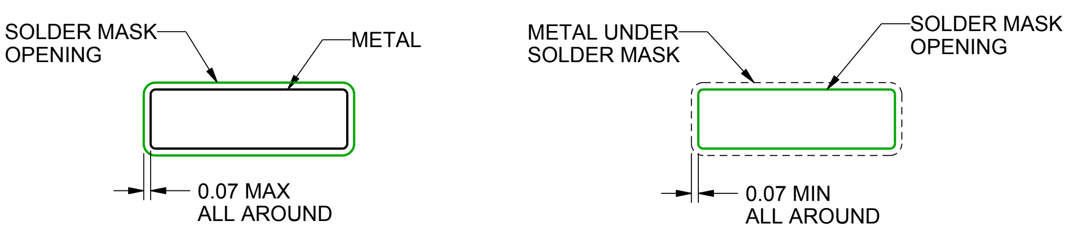


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X



NON SOLDER MASK
DEFINED

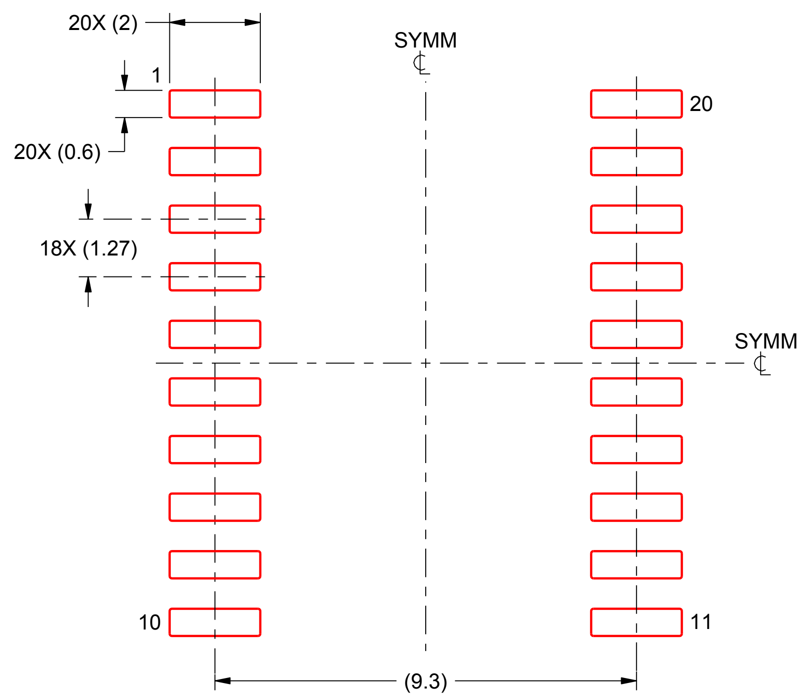
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

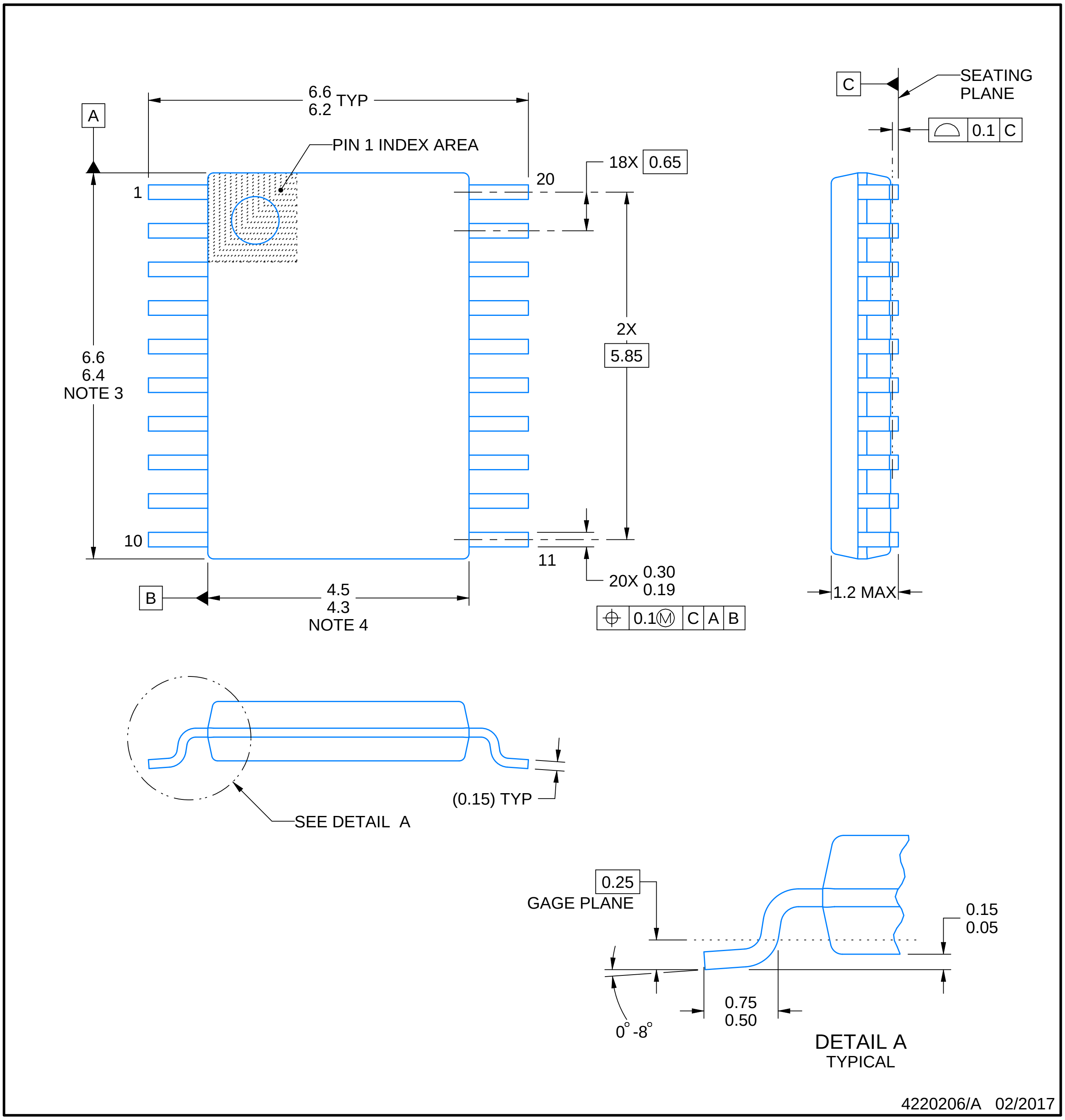


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

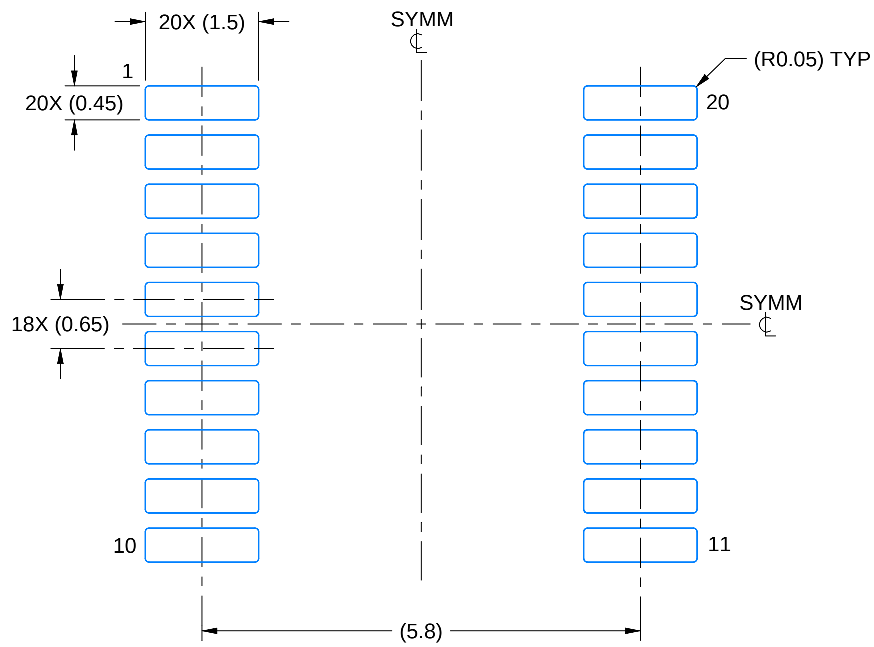
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



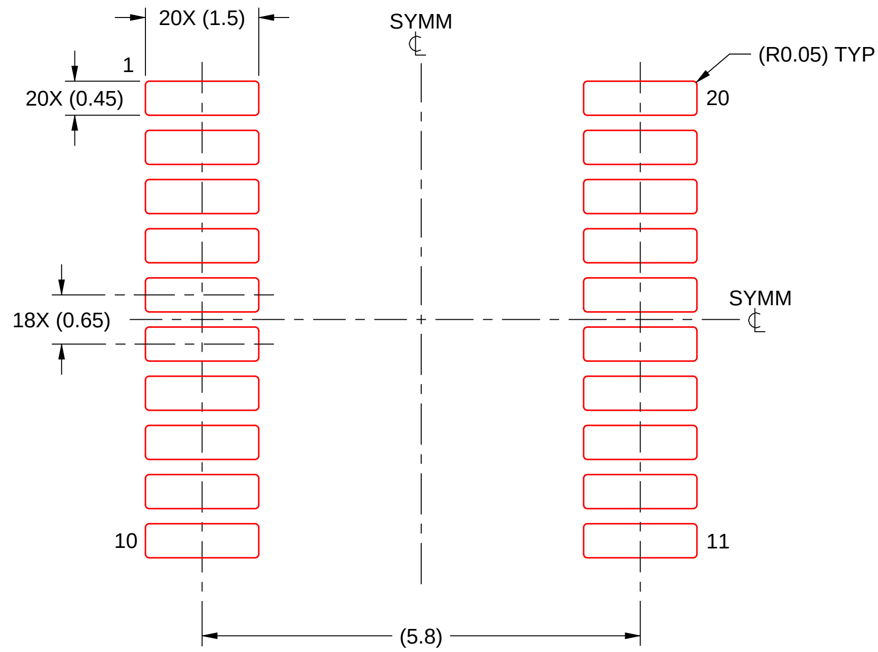
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



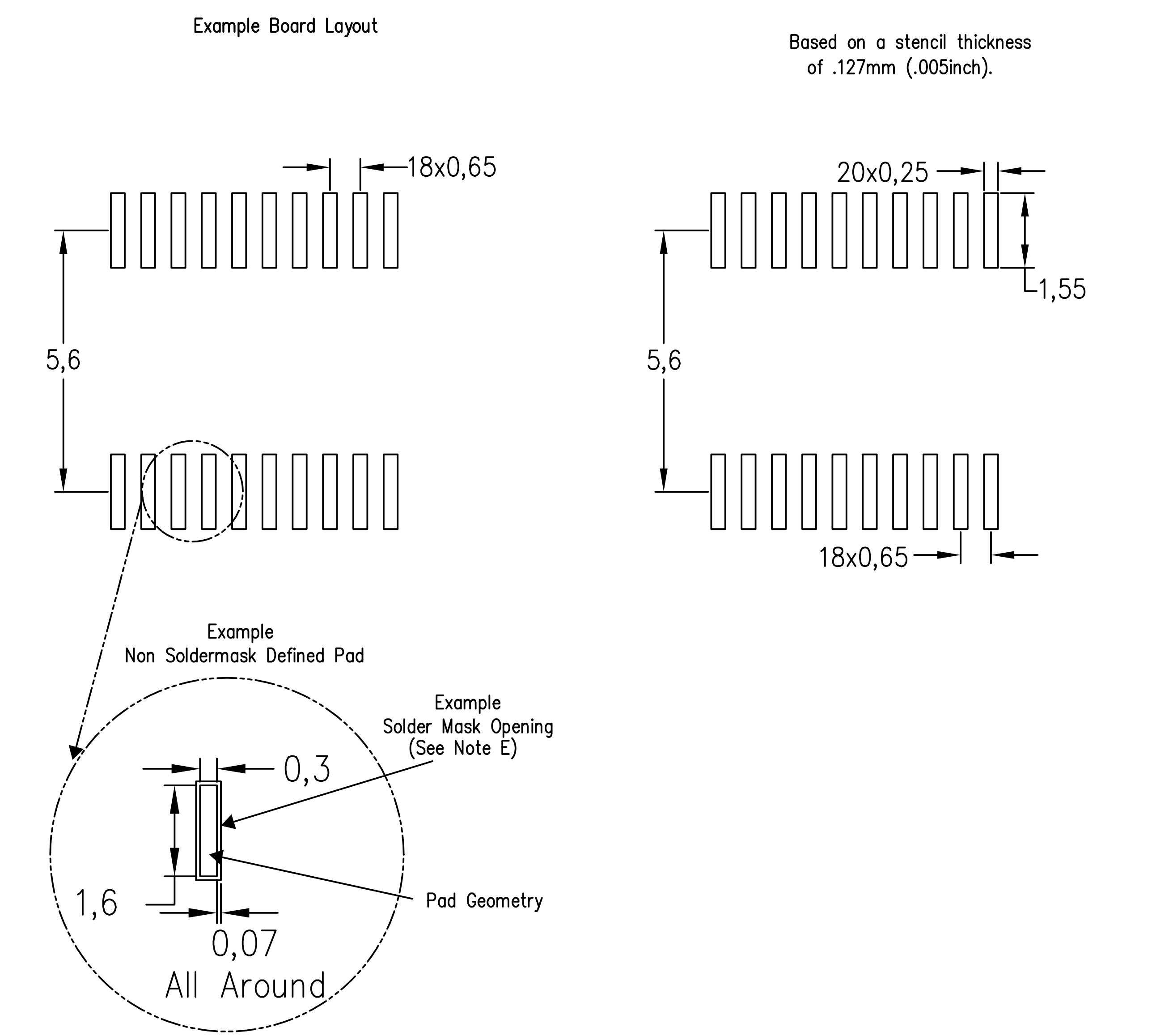
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



4211284–5/G 08/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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