The TLV5614 is a quadruple 12-bit voltage output digital-to-analog converter (DAC) with a flexible 4-wire serial interface. The 4-wire serial interface allows glueless interface to TMS320, SPI, QSPI, and Microwire serial ports. The TLV5614 is programmed with a 16-bit serial word comprised of a DAC address, individual DAC control bits, and a 12-bit DAC value. The device has provision for two supplies: one digital supply for the serial interface (via pins DVDD and DGND), and one for the DACs, reference buffers, and output buffers (via pins AVDD and AGND). Each supply is independent of the other, and can be any value between 2.7 V and 5.5 V. The dual supplies allow a typical application where the DAC is controlled via a microprocessor operating on a 3 V supply (also used on pins DVDD and DGND), with the DACs operating on a 5 V supply. Of course, the digital and analog supplies can be tied together.

The resistor string output voltage is buffered by a x2 gain rail-to-rail output buffer. The buffer features a Class AB output stage to improve stability and reduce settling time. A rail-to-rail output stage and a power-down mode makes it ideal for single voltage, battery based applications. The settling time of the DAC is programmable to allow the designer to optimize speed versus power dissipation. The settling time is chosen by the control bits within the 16-bit serial input string. A high-impedance buffer is integrated on the REFINAB and REFINCD terminals to reduce the need for a low source impedance drive to the terminal. REFINAB and REFINCD allow DACs A and B to have a different reference voltage then DACs C and D.

The TLV5614 is implemented with a CMOS process and is available in a 16-terminal SOIC package. The TLV5614C is characterized for operation from 0°C to 70°C. The TLV5614I is characterized for operation from -40°C to 85°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SPI and QSPI are trademarks of Motorola, Inc.
Microwire is a trademark of National Semiconductor Corporation.

Copyright © 1998 – 2003, Texas Instruments Incorporated

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.
TTL5614
2.7-V TO 5.5-V 12-BIT 3-μS QUADRUPLE DIGITAL-TO-ANALOG CONVERTERS
WITH POWER DOWN

AVAILABLE OPTIONS

<table>
<thead>
<tr>
<th></th>
<th>TA</th>
<th>PACKAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>SOIC (D)</td>
<td>TSSOP (PW)</td>
</tr>
<tr>
<td>0°C to 70°C</td>
<td>TLV5614CD</td>
<td>TLV5614CPW</td>
</tr>
<tr>
<td>-40°C to 85°C</td>
<td>TLV5614ID</td>
<td>TLV5614IPW</td>
</tr>
</tbody>
</table>

† Wafer Scale Packaging, also called Bumped Dice. See Figure 17.

functional block diagram

REFINAB 15

Power-On Reset

DIN 4

Serial Input Register

FS 7

DAC Select/Control Logic

SCLK 5

CS 6

REFINCD 10

AVDD 16

DVDD 1

DAC A

12-Bit DAC Latch

2-Bit Control Data Latch

Power-Down/Speed Control

DAC B

DAC C

DAC D

OUTA 14

OUTB 13

OUTC 12

OUTD 11

AGND 9

DGND 8

LDAC 3

PD 2
## Terminal Functions

<table>
<thead>
<tr>
<th>TERMINAL NAME</th>
<th>NO.</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>AGND</td>
<td>9</td>
<td>I</td>
<td>Analog ground</td>
</tr>
<tr>
<td>AVDD</td>
<td>16</td>
<td>I</td>
<td>Analog supply</td>
</tr>
<tr>
<td>CS</td>
<td>6</td>
<td>I</td>
<td>Chip select. This terminal is active low.</td>
</tr>
<tr>
<td>DGND</td>
<td>8</td>
<td>I</td>
<td>Digital ground</td>
</tr>
<tr>
<td>DIN</td>
<td>4</td>
<td>I</td>
<td>Serial data input</td>
</tr>
<tr>
<td>DVDD</td>
<td>1</td>
<td>I</td>
<td>Digital supply</td>
</tr>
<tr>
<td>FS</td>
<td>7</td>
<td>I</td>
<td>Frame sync input. The falling edge of the frame sync pulse indicates the start of a serial data frame shifted out to the TLV5614.</td>
</tr>
<tr>
<td>PD</td>
<td>2</td>
<td>I</td>
<td>Power down pin. Powers down all DACs (overriding their individual power down settings), and all output stages. This terminal is active low.</td>
</tr>
<tr>
<td>LDAC</td>
<td>3</td>
<td>I</td>
<td>Load DAC. When the LDAC signal is high, no DAC output updates occur when the input digital data is read into the serial interface. The DAC outputs are only updated when LDAC is low.</td>
</tr>
<tr>
<td>REFINAB</td>
<td>15</td>
<td>I</td>
<td>Voltage reference input for DACs A and B.</td>
</tr>
<tr>
<td>REFINCD</td>
<td>10</td>
<td>I</td>
<td>Voltage reference input for DACs C and D.</td>
</tr>
<tr>
<td>SCLK</td>
<td>5</td>
<td>I</td>
<td>Serial clock input</td>
</tr>
<tr>
<td>OUTA</td>
<td>14</td>
<td>O</td>
<td>DACA output</td>
</tr>
<tr>
<td>OUTB</td>
<td>13</td>
<td>O</td>
<td>DACB output</td>
</tr>
<tr>
<td>OUTC</td>
<td>12</td>
<td>O</td>
<td>DACC output</td>
</tr>
<tr>
<td>OUTD</td>
<td>11</td>
<td>O</td>
<td>DACD output</td>
</tr>
</tbody>
</table>

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

- Supply voltage, \((DV_{DD}, AV_{DD} \text{ to } GND)\) .......................... 7 V
- Supply voltage difference, \((AV_{DD} \text{ to } DV_{DD})\) .......................... –2.8 V to 2.8 V
- Digital input voltage range ................................................................. –0.3 V to \(DV_{DD} + 0.3\) V
- Reference input voltage range .............................................................. –0.3 V to \(AV_{DD} + 0.3\) V
- Operating free-air temperature range, \(T_A:\) TLV5614C ................................. 0°C to 70°C
- TLV5614I ................................................................. –40°C to 85°C
- Storage temperature range, \(T_{stg}\) .................................................... –65°C to 150°C
- Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds ..................... 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
recommended operating conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage, AV&lt;sub&gt;DD&lt;/sub&gt;, DV&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>5-V supply</td>
<td>4.5</td>
<td>5</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>3-V supply</td>
<td>2.7</td>
<td>3</td>
<td>3.3</td>
<td>V</td>
</tr>
<tr>
<td>High-level digital input voltage, V&lt;sub&gt;IH&lt;/sub&gt;</td>
<td>DV&lt;sub&gt;DD&lt;/sub&gt; = 2.7 V</td>
<td>2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>DV&lt;sub&gt;DD&lt;/sub&gt; = 5.5 V</td>
<td>2.4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Low-level digital input voltage, V&lt;sub&gt;L&lt;/sub&gt;</td>
<td>DV&lt;sub&gt;DD&lt;/sub&gt; = 2.7 V</td>
<td>0.6</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>DV&lt;sub&gt;DD&lt;/sub&gt; = 5.5 V</td>
<td>1</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Reference voltage, V&lt;sub&gt;ref&lt;/sub&gt; to REFINAB, REFINCD terminal</td>
<td>5-V supply, See Note 1</td>
<td>0</td>
<td>2.048 V&lt;sub&gt;DD&lt;/sub&gt;–1.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>3-V supply, See Note 1</td>
<td>0</td>
<td>1.024 V&lt;sub&gt;DD&lt;/sub&gt;–1.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Load resistance, R&lt;sub&gt;L&lt;/sub&gt;</td>
<td>2</td>
<td></td>
<td>10</td>
<td></td>
<td>kΩ</td>
</tr>
<tr>
<td>Load capacitance, C&lt;sub&gt;L&lt;/sub&gt;</td>
<td>100</td>
<td></td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>Serial clock rate, SCLK</td>
<td>20</td>
<td></td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>Operating free-air temperature</td>
<td>TLV5614C</td>
<td>0</td>
<td>70</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td>TLV5614I</td>
<td>–40</td>
<td>85</td>
<td></td>
<td>°C</td>
</tr>
</tbody>
</table>

NOTE 1: Voltages greater than AV<sub>DD</sub>/2 cause output saturation for large DAC codes.

electrical characteristics over recommended operating free-air temperature range, supply voltages, and reference voltages (unless otherwise noted)

static DAC specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td></td>
<td>12</td>
<td></td>
<td></td>
<td>bits</td>
</tr>
<tr>
<td>Integral nonlinearity (INL), end point adjusted</td>
<td>See Note 2</td>
<td>±1.5</td>
<td>±4</td>
<td></td>
<td>LSB</td>
</tr>
<tr>
<td>Differential nonlinearity (DNL)</td>
<td>See Note 3</td>
<td>±0.5</td>
<td>±1</td>
<td></td>
<td>LSB</td>
</tr>
<tr>
<td>EZS Zero scale error (offset error at zero scale)</td>
<td>See Note 4</td>
<td>±12</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>Zero scale error temperature coefficient</td>
<td>See Note 5</td>
<td>10</td>
<td></td>
<td></td>
<td>ppm/°C</td>
</tr>
<tr>
<td>EG Gain error</td>
<td>See Note 6</td>
<td></td>
<td>±0.6</td>
<td></td>
<td>% of FS voltage</td>
</tr>
<tr>
<td>Gain error temperature coefficient</td>
<td>See Note 7</td>
<td>10</td>
<td></td>
<td></td>
<td>ppm/°C</td>
</tr>
<tr>
<td>PSRR Power supply rejection ratio</td>
<td>Zero scale</td>
<td>–80</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>Full scale</td>
<td>–80</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
</tbody>
</table>

NOTES: 2. The relative accuracy or integral nonlinearity (INL) sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors.
3. The differential nonlinearity (DNL) sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.
4. Zero-scale error is the deviation from zero voltage output when the digital input code is zero.
5. Zero-scale-error temperature coefficient is given by: EZS TC = [EZS (T<sub>max</sub>) – EZS (T<sub>min</sub>)]/V<sub>ref</sub> × 10<sup>6</sup>/(T<sub>max</sub> – T<sub>min</sub>).
6. Gain error is the deviation from the ideal output (2 V<sub>ref</sub> – 1 LSB) with an output load of 10 kΩ excluding the effects of the zero-error.
7. Gain temperature coefficient is given by: EG TC = [EG(T<sub>max</sub>) – EG (T<sub>min</sub>)]/V<sub>ref</sub> × 10<sup>6</sup>/(T<sub>max</sub> – T<sub>min</sub>).
8. Zero-scale-error rejection ratio (EZS–RR) is measured by varying the AV<sub>DD</sub> from 5 ± 0.5 V and 3 ± 0.3 V dc, and measuring the proportion of this signal imposed on the zero-code output voltage.
9. Full-scale rejection ratio (EG–RR) is measured by varying the AV<sub>DD</sub> from 5 ± 0.5 V and 3 ± 0.3 V dc and measuring the proportion of this signal imposed on the full-scale output voltage after subtracting the zero scale change.
electrical characteristics over recommended operating free-air temperature range, supply voltages, and reference voltages (unless otherwise noted) (continued)

individual DAC output specifications

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_O</td>
<td>Voltage output range</td>
<td>R_L = 10 kΩ</td>
<td>0</td>
<td>AV_DD–0.4 V</td>
<td></td>
</tr>
<tr>
<td>Output load regulation accuracy</td>
<td>R_L = 2 kΩ vs 10 kΩ</td>
<td>0.1</td>
<td>0.25</td>
<td>% of FS voltage</td>
<td></td>
</tr>
</tbody>
</table>

reference inputs (REFINAB, REFINCD)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_I</td>
<td>Input voltage range</td>
<td>See Note 10</td>
<td>0</td>
<td>AV_DD–1.5 V</td>
<td></td>
</tr>
<tr>
<td>R_I</td>
<td>Input resistance</td>
<td>10</td>
<td></td>
<td></td>
<td>MΩ</td>
</tr>
<tr>
<td>C_I</td>
<td>Input capacitance</td>
<td>5</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>Reference feed through</td>
<td>REFIN = 1 Vpp at 1 kHz + 1.024 V dc (see Note 11)</td>
<td>–75</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Reference input bandwidth</td>
<td>REFIN = 0.2 Vpp + 1.024 V dc large signal</td>
<td>Slow</td>
<td>0.5</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast</td>
<td>1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

NOTES: 10. Reference input voltages greater than V_DD/2 cause output saturation for large DAC codes.
11. Reference feedthrough is measured at the DAC output with an input code = 000 hex and a V_ref (REFINAB or REFINCD) input = 1.024 Vdc + 1 Vpp at 1 kHz.

digital inputs (DIN, CS, LDAC, PD)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>IIH High-level digital input current</td>
<td>V_I = V_DD</td>
<td>±1</td>
<td></td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>IL Low-level digital input current</td>
<td>V_I = 0 V</td>
<td>±1</td>
<td></td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>C_I Input capacitance</td>
<td></td>
<td>3</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
</tbody>
</table>

power supply

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>IDD Power supply current</td>
<td>5-V supply, No load, Clock running, All inputs 0 V or V_DD</td>
<td>Slow</td>
<td>1.6</td>
<td>2.4</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast</td>
<td>3.8</td>
<td>5.6</td>
<td></td>
</tr>
<tr>
<td></td>
<td>3-V supply, No load, Clock running, All inputs 0 V or V_DD</td>
<td>Slow</td>
<td>1.2</td>
<td>1.8</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast</td>
<td>3.2</td>
<td>4.8</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Power down supply current (see Figure 12)</td>
<td></td>
<td>10</td>
<td></td>
<td>nA</td>
</tr>
</tbody>
</table>
## Analog Output Dynamic Performance

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>SR</strong> Output slew rate</td>
<td>CL = 100 pF, RL = 10 kΩ, V0 = 10% to 90%, Vref = 2.048 V, 1024 V</td>
<td>Fast</td>
<td>5</td>
<td></td>
<td>V/μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Slow</td>
<td>1</td>
<td></td>
<td>V/μs</td>
</tr>
<tr>
<td><strong>tS</strong> Output settling time</td>
<td>To ± 0.5 LSB, CL = 100 pF, RL = 10 kΩ</td>
<td>Fast</td>
<td>3</td>
<td>5.5</td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Slow</td>
<td>9</td>
<td>20</td>
<td>μs</td>
</tr>
<tr>
<td><strong>tS(c)</strong> Output settling time, code to code</td>
<td>To ± 0.5 LSB, CL = 100 pF, RL = 10 kΩ</td>
<td>Fast</td>
<td>1</td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Slow</td>
<td>2</td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td><strong>Glitch energy</strong></td>
<td>Code transition from 7FF to 800</td>
<td>10</td>
<td></td>
<td></td>
<td>nV-sec</td>
</tr>
<tr>
<td><strong>SNR</strong> Signal-to-noise ratio</td>
<td>Sinewave generated by DAC, Reference voltage = 1.024 at 3 V and 2.048 at 5 V, fS = 400 KSPS</td>
<td>74</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td><strong>S/(N+D)</strong> Signal to noise + distortion</td>
<td></td>
<td>66</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>THD</strong> Total harmonic distortion</td>
<td>fOUT = 1.1 kHz sinewave, CL = 100 pF, RL = 10 kΩ</td>
<td>–68</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>SFDR</strong> Spurious free dynamic range</td>
<td>BW = 20 kHz</td>
<td>70</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**
12. Settling time is the time for the output signal to remain within ±0.5 LSB of the final measured value for a digital input code change of FFF hex to 080 hex for 080 hex to FFF hex.
13. Settling time is the time for the output signal to remain within ±0.5 LSB of the final measured value for a digital input code change of one count.
14. Limits are ensured by design and characterization, but are not production tested.
digital input timing requirements

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{su}(CS-FS)$</td>
<td>10</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{su}(FS-CK)$</td>
<td>8</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{su}(C16-FS)$</td>
<td>10</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{su}(C16-CS)$</td>
<td>8</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{WH}$</td>
<td>25</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{WL}$</td>
<td>25</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{su}(D)$</td>
<td>8</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{H}(D)$</td>
<td>5</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{WH}(FS)$</td>
<td>20</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

PARAMETER MEASUREMENT INFORMATION

Figure 1. Timing Diagram
TYPICAL CHARACTERISTICS

**Figure 2**
Load Regulation

- $V_{DD} = 3\, \text{V}$, $V_{ref} = 1\, \text{V}$, $V_{O} = $ Full Scale
- 3 V Slow Mode, Sink
- 3 V Fast Mode, Sink

**Figure 3**
Load Regulation

- $V_{DD} = 5\, \text{V}$, $V_{ref} = 2\, \text{V}$, $V_{O} = $ Full Scale
- 5 V Slow Mode, Sink
- 5 V Fast Mode, Sink

**Figure 4**
Load Regulation

- $V_{DD} = 5\, \text{V}$, $V_{ref} = 2\, \text{V}$, $V_{O} = $ Full Scale
- 5 V Slow Mode, Source
- 5 V Fast Mode, Source

**Figure 5**
Load Regulation

- $V_{DD} = 3\, \text{V}$, $V_{ref} = 1\, \text{V}$, $V_{O} = $ Full Scale
- 3 V Slow Mode, Source
- 3 V Fast Mode, Source
TYPICAL CHARACTERISTICS

**SUPPLY CURRENT vs TEMPERATURE**

- $V_{DD} = 3\, V$
- $V_{ref} = 1.024\, V$
- $V_{O}$ Full Scale (Worst Case For $I_{DD}$)

- Fast Mode
- Slow Mode

Figure 6

**SUPPLY CURRENT vs TEMPERATURE**

- $V_{DD} = 5\, V$
- $V_{ref} = 1.024\, V$
- $V_{O}$ Full Scale (Worst Case For $I_{DD}$)

- Fast Mode
- Slow Mode

Figure 7

**TOTAL HARMONIC DISTORTION vs FREQUENCY**

- $V_{ref} = 1\, V\, dc + 1\, V\, p/p$ Sinewave,
- Output Full Scale

- Fast Mode

Figure 8

**TOTAL HARMONIC DISTORTION vs FREQUENCY**

- $V_{ref} = 1\, V\, dc + 1\, V\, p/p$ Sinewave,
- Output Full Scale

- Slow Mode

Figure 9
TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION AND NOISE vs FREQUENCY

Figure 10

TOTAL HARMONIC DISTORTION AND NOISE vs FREQUENCY

Figure 11

SUPPLY CURRENT vs TIME (WHEN ENTERING POWER-DOWN MODE)

Figure 12
TYPICAL CHARACTERISTICS

DIFFERENTIAL NONLINEARITY

\[ V_{CC} = 5 \text{ V}, V_{ref} = 2 \text{ V}, \text{SCLK} = 1 \text{ MHz} \]

INTEGRAL NONLINEARITY

\[ V_{CC} = 5 \text{ V}, V_{ref} = 2 \text{ V}, \text{SCLK} = 1 \text{ MHz} \]

Figure 13

Figure 14
APPLICATION INFORMATION

general function

The TLV5614 is a 12-bit single supply DAC based on a resistor string architecture. The device consists of a serial interface, speed and power down control logic, a reference input buffer, a resistor string, and a rail-to-rail output buffer.

The output voltage (full scale determined by external reference) is given by:

\[ \text{output voltage} = \frac{2 \times \text{REF} \times \text{CODE}}{2^n} \text{[V]} \]

where REF is the reference voltage and CODE is the digital input value within the range of 0 to \(2^n - 1\), where \(n=12\) (bits). The 16-bit data word, consisting of control bits and the new DAC value, is illustrated in the data format section. A power-on reset initially resets the internal latches to a defined state (all bits zero).

serial interface

Explanation of data transfer: First, the device has to be enabled with \(\overline{CS}\) set to low. Then, a falling edge of FS starts shifting the data bit-per-bit (starting with the MSB) to the internal register on the falling edges of SCLK. After 16 bits have been transferred or FS rises, the content of the shift register is moved to the DAC latch which updates the voltage output to the new level.

The serial interface of the TLV5614 can be used in two basic modes:
- Four wire (with chip select)
- Three wire (without chip select)

Using chip select (four wire mode), it is possible to have more than one device connected to the serial port of the data source (DSP or microcontroller). The interface is compatible with the TMS320™ DSP family. Figure 15 shows an example with two TLV5614s connected directly to a TMS320 DSP.

![Figure 15. TMS320 Interface](image)

TMS320 is a trademark of Texas Instruments.
serial interface (continued)

If there is no need to have more than one device on the serial bus, then $\overline{CS}$ can be tied low. Figure 16 shows an example of how to connect the TLV5614 to a TMS320, SPI, or Microwire port using only three pins.

![Diagram of serial interface connections](image)

**Figure 16. Three-Wire Interface**

Notes on SPI and Microwire: Before the controller starts the data transfer, the software has to generate a falling edge on the I/O pin connected to FS. If the word width is 8 bits (SPI and Microwire), two write operations must be performed to program the TLV5614. After the write operation(s), the DAC output is updated automatically on the next positive clock edge following the sixteenth falling clock edge.

**serial clock frequency and update rate**

The maximum serial clock frequency is given by:

$$f_{SCLK_{max}} = \frac{1}{t_{WH\text{(min)}} + t_{WL\text{(min)}}} = 20 \text{ MHz}$$

The maximum update rate is:

$$f_{UPDATE_{max}} = \frac{1}{16(t_{WH\text{(min)}} + t_{WL\text{(min)}})} = 1.25 \text{ MHz}$$

Note that the maximum update rate is a theoretical value for the serial interface since the settling time of the TLV5614 has to be considered also.

**data format**

The 16-bit data word for the TLV5614 consists of two parts:

- Control bits $(D_{15} \ldots D_{12})$
- New DAC value $(D_{11} \ldots D_{0})$

| D15 | D14 | D13 | D12 | D11 | D10 | D9  | D8  | D7  | D6  | D5  | D4  | D3  | D2  | D1  | D0  |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| A1  | A0  | PWR | SPD | New DAC value (12 bits) |

X: don’t care
SPD: Speed control bit. $1 \rightarrow$ fast mode $0 \rightarrow$ slow mode
PWR: Power control bit. $1 \rightarrow$ power down $0 \rightarrow$ normal operation
APPLICATION INFORMATION

In power-down mode, all amplifiers within the TLV5614 are disabled. A particular DAC (A, B, C, D) of the TLV5614 is selected by A1 and A0 within the input word.

<table>
<thead>
<tr>
<th>A1</th>
<th>A0</th>
<th>DAC</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>A</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>B</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>C</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>D</td>
</tr>
</tbody>
</table>

Using TLV5614IYE, Bumped Dice

- Melting point of eutectic solder is 183°C.
- Recommended peak reflow temperatures are in the 220°C to 230°C range.
- The use of underfill is required. The use of underfill greatly reduces the risk of thermal mismatch fails.

Underfill is an epoxy/adhesive that may be added during the board assembly process to improve board level/system level reliability. The process is to dispense the epoxy under the dice after die attach reflow. The epoxy adheres to the body of the device and to the printed-circuit board. It reduces stress placed upon the solder joints due to the thermal coefficient of expansion (TCE) mismatch between the board and the component. Underfill material is highly filled with silica or other fillers to increase an epoxy’s modulus, reduce creep sensitivity, and decrease the material’s TCE.

The recommendation for peak flow temperatures of 220°C to 230°C is based on general empirical results that indicate that this temperature range is needed to facilitate good wetting of the solder bump to the substrate or circuit board pad. Lower peak temperatures may cause nonwets (cold solder joints).

NOTE A: All linear dimensions are in millimeters.
NOTE B: This drawing is subject to change without notice.
NOTE C: Scale = 18x

Figure 17. TLV5614IYE Bumped Dice
TLV5614 interfaced to TMS320C203 DSP

**hardware interfacing**

Figure 17 shows an example of how to connect the TLV5614 to a TMS320C203 DSP. The serial port is configured in burst mode, with FSX generated by the TMS320C203 to provide the frame sync (FS) input to the TLV5614. Data is transmitted on the DX line, with the serial clock input on the CLKX line. The general-purpose input/output port bits IO0 and IO1 are used to generate the chip select (CS) and DAC latch update (LDAC) inputs to the TLV5614. The active low power down (PD) is pulled high all the time to ensure the DACs are enabled.

![Diagram of TLV5614 connected to TMS320C203](image)

**Figure 18. TLV5614 Interfaced With TMS320C203**

**software**

The application example outputs a differential in-phase (sine) signal between the VOUTA and VOUTB pins, and its quadrature (cosine) signal as the differential signal between VOUTC and VOUTD.

The on-chip timer is used to generate interrupts at a fixed frequency. The related interrupt service routine pulses LDAC low to update all 4 DACs simultaneously, then fetches and writes the next sample to all 4 DACs. The samples are stored in a look-up table, which describes two full periods of a sine wave.

The synchronous serial port of the DSP is used in burst mode. In this mode, the processor generates an FS pulse preceding the MSB of every data word. If multiple, contiguous words are transmitted, a violation of the tsu(C16–FS) timing requirement occurs. To avoid this, the program waits until the transmission of the previous word has been completed.
APPLICATION INFORMATION

;---------------------------------------------------------------
; Processor: TMS320C203 running at 40 MHz
;
; Description:
;
; This program generates a differential in-phase (sine) on (OUTA-OUTB) and it’s
; quadrature (cosine) as a differential signal on (OUTC-OUTD).
;
; The DAC codes for the signal samples are stored as a table of 64 12-bit values,
; describing 2 periods of a sine function. A rolling pointer is used to address the
; table location in the first period of this waveform, from which the DAC A samples
; are read. The samples for the other 3 DACs are read at an offset to this rolling
; pointer:
;
; DAC Function Offset from rolling pointer
; A sine 0
; B inverse sine 16
; C cosine 8
; D inverse cosine 24
;
; The on-chip timer is used to generate interrupts at a fixed rate. The interrupt
; service routine first pulses LDAC low to update all DACs simultaneously
; with the values which were written to them in the previous interrupt. Then all
; 4 DAC values are fetched and written out through the synchronous serial interface
; Finally, the rolling pointer is incremented to address the next sample, ready for
; the next interrupt.
;
; © 1998, Texas Instruments Inc.

;---------- I/O and memory mapped regs --------------------------
.include "regs.asm"

;--------- jump vectors ----------------------------------------
.ps 0h
   b start
   b int1
   b int23
   b timer_isr;

;--------- variables -------------------------------------------
temp .equ 0060h
r_ptr .equ 0061h
iosr_stat .equ 0062h
DACa_ptr .equ 0063h
DACb_ptr .equ 0064h
DACc_ptr .equ 0065h
DACd_ptr .equ 0066h

;-------- constants---------------------------------------------
; DAC control bits to be OR’ed onto data
; all fast mode
DACa_control .equ 01000h
DACb_control .equ 00040h
DACc_control .equ 00000h
DACd_control .equ 00000h

;-------- tables ---------------------------------------------
.ds 02000h
sinevals
    .word 00800h
    .word 0097Ch
    .word 00AE9h
    .word 00C3Ah
    .word 00D61h
    .word 00E53h
    .word 00F07h
    .word 00F76h
    .word 00F9Ch
    .word 00F76h
    .word 00F07h
    .word 00E53h
APPLICATION INFORMATION

.word 00D61h
.word 00C3Ah
.word 00AE9h
.word 0097Ch
.word 00800h
.word 00684h
.word 00517h
.word 003C6h
.word 0029Fh
.word 001ADh
.word 000F9h
.word 0008Ah
.word 00064h
.word 0008Ah
.word 000F9h
.word 001ADh
.word 0029Fh
.word 003C6h
.word 00517h
.word 00684h
.word 00800h
.word 0097Ch
.word 00AE9h
.word 00C3Ah
.word 00D61h
.word 00E53h
.word 00F07h
.word 00F76h
.word 00F99h
.word 00F76h
.word 00F07h
.word 00E53h
.word 00D61h
.word 00C3Ah
.word 00AE9h
.word 0097Ch
.word 00800h
.word 00684h
.word 00517h
.word 003C6h
.word 0029Fh
.word 001ADh
.word 000F9h
.word 0008Ah
.word 00064h
.word 0008Ah
.word 000F9h
.word 001ADh
.word 0029Fh
.word 003C6h
.word 00517h
.word 00684h
APPLICATION INFORMATION

;-------------------------------------------
; Main Program
;-------------------------------------------
.ps 1000h
.entry
start

; disable interrupts

; set up the timer
; timer period set by values in PRD and TDDR
; period = (CLKOUT1 period) x (1+PRD) x (1+TDDR)
; examples for TMS320C203 with 40MHz main clock
; Timer rate  TDDR  PRD
; 80 kHz  9  24 (18h)
; 50 kHz  9  39 (27h)

prd_val.equ 0018h

; Configure IO0/1 as outputs to be :
; IO0  CS - and set high
; IO1 LDAC - and set high

in temp, ASPCR; configure as output
lac temp
or #0003h
sacl temp
out temp, ASPCR
in temp, IOSR; set them high
lac temp
or #0003h
sacl temp
out temp, IOSR

; set up serial port for
; SSPCR.TXM=1 Transmit mode - generate FSX
; SSPCR.MCM=1 Clock mode - internal clock source
; SSPCR.FSM=1 Burst mode

splk #0000Eh, temp
out temp, SSPCR; reset transmitter
splk #0002Eh, temp
out temp, SSPCR

; reset the rolling pointer

lac #000h
sacl r_ptr

; enable interrupts

clrc INTM ; enable maskable interrupts

; loop forever!
APPLICATION INFORMATION

next idle ; wait for interrupt
b next ;

; all else fails stop here
;
done b done ; hang there
;
Interrupt Service Routines
;
int1 ret ; do nothing and return
int23 ret ; do nothing and return
timer_isr:

in iosr_stat, IOSR; store IOSR value into variable space
lacl iosr_stat ; load acc with iosr status
and #0FFFDh ; reset IO1 - LDAC low
sacl temp ;
out temp, IOSR ;
or #0002h ; set IO1 - LDAC high
sacl temp ;
out temp, IOSR ;
and #0FFFFh ; reset IO0 - CS low
sacl temp ;
out temp, IOSR ;
lacl r_ptr ; load rolling pointer to accumulator
add #sinevals ; add pointer to table start
sacl DACa_ptr ; to get a pointer for next DAC a sample
add #08h ; add 8 to get to DAC C pointer
sacl DACc_ptr
add #08h ; add 8 to get to DAC B pointer
sacl DACb_ptr
add #08h ; add 8 to get to DAC D pointer
sacl DACd_ptr
mar *,ar0 ; set ar0 as current AR
;
; DAC A
lar ar0, DACa_ptr ; ar0 points to DAC a sample
lacl * ; get DAC a sample into accumulator
or #DACa_control; OR in DAC A control bits
sacl temp ;
out temp, SDTR ; send data
;
; We must wait for transmission to complete before writing next word to the SDTR.;
TLV5614/04 interface does not allow the use of burst mode with the full packet; rate, as
we need a CLKX –ve edge to clock in last bit before FS goes high again.; to allow SPI
compatibility.
;
;
rpt #016h ; wait long enough for this configuration
nop ; of MCLK/CLKOUT1 rate
;
; DAC B
lar ar0, dacb_ptr; ar0 points to DAC a sample
lacl * ; get DAC a sample into accumulator
or #DACb_control; OR in DAC B control bits
sacl temp ;
out temp, SDTR ; send data
rpt #016h ; wait long enough for this configuration
nop ; of MCLK/CLKOUT1 rate
;
; DAC C
lar ar0, dacc_ptr; ar0 points to dac a sample
lacl * ; get DAC a sample into accumulator
or #DACc_control; OR in DAC C control bits
sacl temp ;
out temp, SDTR; send data
rpt #016h ; wait long enough for this configuration
nop ; of MCLK/CLKOUT1 rate
APPLICATION INFORMATION

; DAC D
lar ar0, dacd_ptr; ar0 points to DAC a sample
lacl *; get DAC a sample into accumulator
or #dacd_control; OR in DAC D control bits
sacl temp;
out temp, SDTR; send data

lacl r_ptr; load rolling pointer to accumulator
add #1h; increment rolling pointer
and #001Fh; count 0-31 then wrap back round
sacl r_ptr; store rolling pointer
rpt #$10h; wait long enough for this configuration
nop; of MCLK/CLKOUT1 rate

; now take CS high again
lacl iosr_stat; load acc with iosr status
or #$001h; set IO0 - CS high
sacl temp;
out temp, IOSR;
clrc intm; re-enable interrupts
ret; return from interrupt
.end
**APPLICATION INFORMATION**

TLV5614 interfaced to MCS®51 microcontroller

**hardware interfacing**

Figure 18 shows an example of how to connect the TLV5614 to an MCS®51 Microcontroller. The serial DAC input data and external control signals are sent via I/O Port 3 of the controller. The serial data is sent on the RxD line, with the serial clock output on the TxD line. Port 3 bits 3, 4, and 5 are configured as outputs to provide the DAC latch update (LDAC), chip select (CS) and frame sync (FS) signals for the TLV5614. The active low power down pin (PD) of the TLV5614 is pulled high to ensure that the DACs are enabled.

![Diagram of TLV5614 interfaced with MCS®51](image)

**software**

The example is the same as for the TMS320C203 in this data sheet, but adapted for a MCS®51 controller. It generates a differential in-phase (sine) signal between the VOUTA and VOUTB pins, and its quadrature (cosine) signal is the differential signal between VOUTC and VOUTD.

The on-chip timer is used to generate interrupts at a fixed frequency. The related interrupt service routine pulses LDAC low to update all 4 DACs simultaneously, then fetches and writes the next sample to all 4 DACs. The samples are stored as a look-up table, which describes one full period of a sine wave.

The serial port of the controller is used in Mode 0, which transmits 8 bits of data on RxD, accompanied by a synchronous clock on TxD. Two writes concatenated together are required to write a complete word to the TLV5614. The CS and FS signals are provided in the required fashion through control of IO port 3, which has bit addressable outputs.
APPLICATION INFORMATION

;------------------------------------------------------------------
; Processor: 80C51
;
; Description:
;
; This program generates a differential in-phase (sine) on (OUTA-OUTB); and it’s quadrature (cosine)
; as a differential signal on (OUTC-OUTD).
;
; © 1998, Texas Instruments Inc.
;------------------------------------------------------------------

NAME  GENIQ
MAIN  SEGMENT  CODE
ISR   SEGMENT  CODE
SINTBL SEGMENT  CODE
VAR1 SEGMENT  DATA
STACK SEGMENT  IDATA
;------------------------------------------------------------------
; Code start at address 0, jump to start
;------------------------------------------------------------------
CSEG  AT   0
LJMP start ; Execution starts at address 0 on power-up.
;------------------------------------------------------------------
; Code in the timer0 interrupt vector
;------------------------------------------------------------------
CSEG  AT   0BH
LJMP timer0isr ; Jump vector for timer 0 interrupt is 000Bh
;------------------------------------------------------------------
; Global variables need space allocated
;------------------------------------------------------------------
RSEG  VAR1
  temp_ptr: DS 1
  rolling_ptr: DS 1
;------------------------------------------------------------------
Interrupt service routine for timer 0 interrupts
;------------------------------------------------------------------
RSEG  ISR
  timer0isr:
    PUSH PSW
    PUSH ACC
    CLR INT1 ; pulse LDAC low
    SETB INT1 ; to latch all 4 previous values at the same time
    ; 1st thing done in timer isr => fixed period
    CLR T0
    ; set CS low
    ; The signal to be output on each DAC is a sine function.
    ; One cycle of a sine wave is held in a table @ sinevals
    ; as 32 samples of msb, lsb pairs (64 bytes).
    ; We have ; one pointer which rolls round this table, rolling_ptr,
    ; incrementing by 2 bytes (1 sample) on each interrupt (at the end of
    ; this routine).
    ; The DAC samples are read at an offset to this rolling pointer:
    ; DAC Function Offset from rolling_ptr
    ; A sine 0
    ; B inverse sine 32
    ; C cosine 16
    ; D inverse cosine48
    MOV DPTR,#sinevals; set DPTR to the start of the table
    ; of sine signal values
    MOV R7,rolling_ptr; R7 holds the pointer
    ; into the sine table
    MOV A,R7 ; get DAC A msb
    MOVC A,@A+DPTR ; msb of DAC A is in the ACC
    ;
 APPLICATION INFORMATION

CLR T1 ; transmit it - set FS low
MOV SBUF,A ; send it out the serial port

INC R7 ; increment the pointer in R7
MOV A,R7 ; to get the next byte from the table
MOVC A,@A+DPTR ; which is the lsb of this sample, now in ACC

A_MSB_TX:
JNB TI,A_MSB_TX ; wait for transmit to complete
CLR TI ; clear for new transmit
MOV SBUF,A ; and send out the lsb of DAC A

; DAC C next
; DAC C codes should be taken from 16 bytes (8 samples) further on
; in the sine table - this gives a cosine function
MOV A,R7 ; pointer in R7
ADD A,#0FH ; add 15 - already done one INC
ANL A,#03FH ; wrap back round to 0 if > 64
MOV R7,A ; pointer back in R7
MOVC A,@A+DPTR ; get DAC C msb from the table
ORL A,#01H ; set control bits to DAC C address

A_LSB_TX:
JNB TI,A_LSB_TX ; wait for DAC A lsb transmit to complete
SETB T1 ; toggle FS
CLR TI ; clear for new transmit
MOV SBUF,A ; and send out the msb of DAC C

C_MSB_TX:
JNB TI,C_MSB_TX ; wait for transmit to complete
CLR TI ; clear for new transmit
MOV SBUF,A ; and send out the lsb of DAC C

; DAC B next
; DAC B codes should be taken from 16 bytes (8 samples) further on
; in the sine table - this gives an inverted sine function
MOV A,R7 ; pointer in R7
ADD A,#0FH ; add 15 - already done one INC
ANL A,#03FH ; wrap back round to 0 if > 64
MOV R7,A ; pointer back in R7
MOVC A,@A+DPTR ; get DAC B msb from the table
ORL A,#02H ; set control bits to DAC B address

C_LSB_TX:
JNB TI,C_LSB_TX ; wait for DAC C lsb transmit to complete
SETB T1 ; toggle FS
CLR TI ; clear for new transmit
MOV SBUF,A ; and send out the msb of DAC B

; get DAC B LSB
INC R7 ; increment the pointer in R7
MOV A,R7 ; to get the next byte from the table
MOVC A,@A+DPTR ; which is the lsb of this sample, now in ACC

B_MSB_TX:
JNB TI,B_MSB_TX ; wait for transmit to complete
CLR TI ; clear for new transmit
MOV SBUF,A ; and send out the lsb of DAC B

; DAC D next
; DAC D codes should be taken from 16 bytes (8 samples) further on
; in the sine table - this gives an inverted cosine function
APPLICATION INFORMATION

MOV A,R7 ; pointer in R7
ADD A,#0FH ; add 15 - already done one INC
ANL A,#03FH ; wrap back round to 0 if > 64
MOV R7,A ; pointer back in R7
MOVC A,@A+DPTR ; get DAC D msb from the table
ORL A,#03H ; set control bits to DAC D address

B_LSB_TX:
JNB TI,B_LSB_TX ; wait for DAC B lsb transmit to complete
SETB T1 ; toggle FS
CLR TI
CLR T1 ; clear for new transmit
MOV SBUF,A ; and send out the msb of DAC D
INC R7 ; increment the pointer in R7
MOV A,R7 ; to get the next byte from the table
MOVC A,@A+DPTR ; which is the lsb of this sample, now in ACC

D_MSB_TX:
JNB TI,D_MSB_TX ; wait for transmit to complete
CLR TI ; clear for new transmit
MOV SBUF,A ; and send out the lsb of DAC D

; increment the rolling pointer to point to the next sample
; ready for the next interrupt
MOV A,rolling_ptr
ADD A,#02H ; add 2 to the rolling pointer
ANL A,#03FH ; wrap back round to 0 if > 64
MOV rolling_ptr,A ; store in memory again

D_LSB_TX:
JNB TI,D_LSB_TX ; wait for DAC D lsb transmit to complete
CLR TI ; clear for next transmit
SETB T1 ; FS high
SETB T0 ; CS high
POP ACC
POP PSW
RETI

; Stack needs definition
;--------------------------------------------------------
RSEG STACK
DS 10h ; 16 Byte Stack!
;--------------------------------------------------------
; Main program code
;--------------------------------------------------------
RSEG MAIN
start:
MOV SP,#STACK-1 ; first set Stack Pointer
CLR A
MOV SCON,A ; set serial port 0 to mode 0
MOV TMOD,#02H ; set timer 0 to mode 2 - auto-reload
MOV TH0,#038H ; set TH0 for 5kHs interrupts
SETB INT1 ; set LDAC = 1
SETB T1 ; set FS = 1
SETB T0 ; set CS = 1
SETB ET0 ; enable timer 0 interrupts
SETB EA ; enable all interrupts
MOV rolling_ptr,A ; set rolling pointer to 0
SETB TR0 ; start timer 0
always:
SJMP always ; while(1) !
SJMP always
RET
;--------------------------------------------------------
; Table of 32 sine wave samples used as DAC data
;--------------------------------------------------------
RSEG SINTBL
APPLICATION INFORMATION

sinevals:
 DW 01000H
 DW 0903EH
 DW 05097H
 DW 0305CH
 DW 0B086H
 DW 070CAH
 DW 0F0E0H
 DW 0F06EH
 DW 0F039H
 DW 0F06EH
 DW 0F0E0H
 DW 070CAH
 DW 0B086H
 DW 0305CH
 DW 05097H
 DW 0903EH
 DW 01000H
 DW 06021H
 DW 0A0E8H
 DW 0C063H
 DW 040F9H
 DW 080B5H
 DW 0009FH
 DW 00051H
 DW 00026H
 DW 00051H
 DW 0009FH
 DW 080B5H
 DW 040F9H
 DW 0C063H
 DW 0A0E8H
 DW 06021H

END
## Packaging Information

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLV5614CD</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>16</td>
<td>40</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>TLV5614C</td>
<td>Samples</td>
</tr>
<tr>
<td>TLV5614CPW</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>PW</td>
<td>16</td>
<td>90</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>TV5614</td>
<td>Samples</td>
</tr>
<tr>
<td>TLV5614CPWG4</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>PW</td>
<td>16</td>
<td>90</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>TV5614</td>
<td>Samples</td>
</tr>
<tr>
<td>TLV5614CPR</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>PW</td>
<td>16</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>TV5614</td>
<td>Samples</td>
</tr>
<tr>
<td>TLV5614ID</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>16</td>
<td>40</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>TLV5614I</td>
<td>Samples</td>
</tr>
<tr>
<td>TLV5614IDR</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>16</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>TLV5614I</td>
<td>Samples</td>
</tr>
<tr>
<td>TLV5614IPW</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>PW</td>
<td>16</td>
<td>90</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>TY5614</td>
<td>Samples</td>
</tr>
<tr>
<td>TLV5614IPWR</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>PW</td>
<td>16</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>TY5614</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSoLETE:** TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV5614:

• Enhanced Product: TLV5614-EP

NOTE: Qualified Version Definitions:

• Enhanced Product - Supports Defense, Aerospace and Medical Applications
TAPE AND REEL INFORMATION

### TAPE DIMENSIONS

- **K0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLV5614CPWR</td>
<td>TSSOP</td>
<td>PW</td>
<td>16</td>
<td>2000</td>
<td>330.0</td>
<td>12.4</td>
<td>6.9</td>
<td>5.6</td>
<td>1.6</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
<tr>
<td>TLV5614IDR</td>
<td>SOIC</td>
<td>D</td>
<td>16</td>
<td>2500</td>
<td>330.0</td>
<td>16.4</td>
<td>6.5</td>
<td>10.3</td>
<td>2.1</td>
<td>8.0</td>
<td>16.0</td>
<td>Q1</td>
</tr>
<tr>
<td>TLV5614IPWR</td>
<td>TSSOP</td>
<td>PW</td>
<td>16</td>
<td>2000</td>
<td>330.0</td>
<td>12.4</td>
<td>6.9</td>
<td>5.6</td>
<td>1.6</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>

*All dimensions are nominal.*
## TAPE AND REEL BOX DIMENSIONS

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLV5614CPWR</td>
<td>TSSOP</td>
<td>PW</td>
<td>16</td>
<td>2000</td>
<td>350.0</td>
<td>350.0</td>
<td>43.0</td>
</tr>
<tr>
<td>TLV5614IDR</td>
<td>SOIC</td>
<td>D</td>
<td>16</td>
<td>2500</td>
<td>350.0</td>
<td>350.0</td>
<td>43.0</td>
</tr>
<tr>
<td>TLV5614IPWR</td>
<td>TSSOP</td>
<td>PW</td>
<td>16</td>
<td>2000</td>
<td>350.0</td>
<td>350.0</td>
<td>43.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
   © Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.
   ∀ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.
E. Reference JEDEC MS-012 variation AC.
NOTES:  
A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Publication IPC-7351 is recommended for alternate designs.  
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.  
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.
IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated