The TLV701x and TLV702x offer an excellent speed-to-power combination with a propagation delay of 260 ns and a quiescent supply current of 5 µA. This combination of fast response time at micropower enables power conscious systems to monitor and respond quickly to fault conditions. With an operating voltage range of 1.6 V to 6.5 V, these comparators are compatible with 3-V and 5-V systems.

These comparators also feature no output phase inversion with overdriven inputs and internal hysteresis. These features make this family of comparators well suited for precision voltage monitoring in harsh, noisy environments where slow-moving input signals must be converted into clean digital outputs.

The TLV701x have push-pull output stages capable of sinking and sourcing milliamps of current when controlling an LED or driving a capacitive load. The TLV702x have open-drain output stages that can be pulled beyond V_{CC}, making it appropriate for level translators and bipolar to single-ended converters.

### Device Information (1)

<table>
<thead>
<tr>
<th>PART NUMBERS</th>
<th>OUTPUT</th>
<th>( I_q )</th>
<th>( t_{PD} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLV7011, TLV7021</td>
<td>Push-pull / Open-drain</td>
<td>5 µA</td>
<td>260 ns</td>
</tr>
<tr>
<td>TLV7012, TLV7022</td>
<td>Push-pull / Open-drain</td>
<td>335 nA</td>
<td>3 µs</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### TLV70x1 Family of Low Power Comparators

<table>
<thead>
<tr>
<th>PART NUMBERS</th>
<th>OUTPUT</th>
<th>( I_q )</th>
<th>( t_{PD} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLV701x / 2x</td>
<td>Push-pull / Open-drain</td>
<td>5 µA</td>
<td>260 ns</td>
</tr>
<tr>
<td>TLV703x / 4x</td>
<td>Push-pull / Open-drain</td>
<td>335 nA</td>
<td>3 µs</td>
</tr>
</tbody>
</table>

### Propagation Delay vs. Overdrive

\[
T_A = 25^\circ C, V_{CC} = 5 \text{ V}, C_L = 15 \text{ pF}
\]
# Table of Contents

1 Features .............................................................................................................. 1
2 Applications ...................................................................................................... 1
3 Description ........................................................................................................ 1
4 Revision History ................................................................................................ 2
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6 Specifications ..................................................................................................... 5
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   6.2 Absolute Maximum Ratings (Dual) ............................................................ 5
   6.3 ESD Ratings ............................................................................................... 5
   6.4 Recommended Operating Conditions (Single) ........................................... 5
   6.5 Recommended Operating Conditions (Dual) ............................................... 6
   6.6 Thermal Information (Single) ................................................................... 6
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## 4 Revision History

### Changes from Revision E (October 2019) to Revision F

- Added SOT-23 (8) and WSON (8) for dual channel options ........................................... 1
- Added SOT-23 (8) and WSON (8) Pin Functions and Package drawings for dual channel options .......................................................... 4
- Added SOT-23 (8) and WSON (8) Thermal Tables for dual channel options ...................... 5

### Changes from Revision D (February 2019) to Revision E

- Added dual channel options ........................................................................ 1

### Changes from Revision C (March 2018) to Revision D

- Added leaded package option to features ......................................................... 1
- Deleted preview status of SOT23 package ...................................................... 1
- Deleted preview status of SOT23 package ...................................................... 3

### Changes from Revision B (November 2017) to Revision C

- Changed the preview SC70 package to production data ..................................... 1

### Changes from Revision A (July 2017) to Revision B

- Changed propagation delay from: 200 ns to: 260 ns ........................................ 1
- Added preview SC70 and SOT-23 packages to the data sheet .......................... 1
- Added TLV70x1 Family of Micropower Comparators table per marketing request ............................................................................................................................. 1
- Changed the key graphic title from: Propagation Delay vs. Overdrive (TLV7011) to: Propagation Delay vs. Overdrive ............................................................... 1
- Removed (TLV7011 only) text from several Typical Characteristics graphs .......... 10
## 5 Pin Configuration and Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O/P(1)</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>OUT</td>
<td>O</td>
<td>Output</td>
</tr>
<tr>
<td>VCC</td>
<td>P</td>
<td>Positive (highest) power supply</td>
</tr>
<tr>
<td>VEE</td>
<td>P</td>
<td>Negative (lowest) power supply</td>
</tr>
<tr>
<td>IN–</td>
<td>I</td>
<td>Inverting input</td>
</tr>
<tr>
<td>IN+</td>
<td>I</td>
<td>Noninverting input</td>
</tr>
</tbody>
</table>

(1) I = Input, O = Output, P = Power

---

**Changes from Original (May 2017) to Revision A**

- Added Figure 7 ............................................................................................................ 10
- Added Figure 10 ........................................................................................................... 10
- Removed some Typical Characteristics graphs ......................................................... 13
- Added content to the Inputs section ........................................................................... 15
- Added the IR Receiver Analog Front End section ..................................................... 20

---

![Diagram of DPW Package](image1)

DPW Package  
5-Pin X2SON  
Top View

![Diagram of DBV and DCK Package](image2)

DBV and DCK Package  
5-Pin SOT-23 and SC70  
Top View

**Pin Functions**

<table>
<thead>
<tr>
<th>NAME</th>
<th>X2SON</th>
<th>SOT-23, SC70</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>OUT</td>
<td>1</td>
<td>1</td>
<td>O Output</td>
</tr>
<tr>
<td>VCC</td>
<td>2</td>
<td>5</td>
<td>P Positive (highest) power supply</td>
</tr>
<tr>
<td>VEE</td>
<td>3</td>
<td>2</td>
<td>P Negative (lowest) power supply</td>
</tr>
<tr>
<td>IN–</td>
<td>4</td>
<td>4</td>
<td>I Inverting input</td>
</tr>
<tr>
<td>IN+</td>
<td>5</td>
<td>3</td>
<td>I Noninverting input</td>
</tr>
</tbody>
</table>

---

Submit Documentation Feedback
(1) Connect thermal pad to V–.

### Pin Functions: TLV7012/22

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>INA–</td>
<td>2</td>
<td>Inverting input, channel A</td>
</tr>
<tr>
<td>INA+</td>
<td>3</td>
<td>Noninverting input, channel A</td>
</tr>
<tr>
<td>INB–</td>
<td>6</td>
<td>Inverting input, channel B</td>
</tr>
<tr>
<td>INB+</td>
<td>5</td>
<td>Noninverting input, channel B</td>
</tr>
<tr>
<td>OUTA</td>
<td>1</td>
<td>Output, channel A</td>
</tr>
<tr>
<td>OUTB</td>
<td>7</td>
<td>Output, channel B</td>
</tr>
<tr>
<td>VEE</td>
<td>4</td>
<td>Negative (lowest) supply or ground (for single-supply operation)</td>
</tr>
<tr>
<td>VCC</td>
<td>8</td>
<td>Positive (highest) supply</td>
</tr>
</tbody>
</table>
6 Specifications

6.1 Absolute Maximum Ratings (Single)
over operating free-air temperature range (unless otherwise noted) \(^{(1)}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage ((V_s = V_{CC} - V_{EE}))</td>
<td>6 V</td>
<td>6 V</td>
<td>V</td>
</tr>
<tr>
<td>Input pins ((\text{IN+}, \text{IN-})) (^{(2)})</td>
<td>(V_{EE} - 0.3)</td>
<td>6 V</td>
<td>V</td>
</tr>
<tr>
<td>Current into Input pins ((\text{IN+}, \text{IN-})) (^{(2)})</td>
<td>±10 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output (OUT) (TLV7011/7012) (^{(3)})</td>
<td>(V_{EE} - 0.3)</td>
<td>(V_{CC} + 0.3)</td>
<td>V</td>
</tr>
<tr>
<td>Output (OUT) (TLV7021/7022)</td>
<td>(V_{EE} - 0.3)</td>
<td>6 V</td>
<td>V</td>
</tr>
<tr>
<td>Output short-circuit duration (^{(4)})</td>
<td>10 s</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Junction temperature, (T_J)</td>
<td>150°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage temperature, (T_{stg})</td>
<td>–65°C</td>
<td>150°C</td>
<td>°C</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

\(^{(2)}\) Input terminals are diode-clamped to \(V_{EE}\). Input signals that can swing 0.3V below \(V_{EE}\) must be current-limited to 10mA or less.

\(^{(3)}\) Output maximum is \((V_{CC} + 0.3V)\) or 6V, whichever is less.

\(^{(4)}\) Short-circuit to ground, one comparator per package.

6.2 Absolute Maximum Ratings (Dual)
over operating free-air temperature range (unless otherwise noted) \(^{(1)}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage ((V_s = V_{CC} - V_{EE}))</td>
<td>–0.3 V</td>
<td>7 V</td>
<td>V</td>
</tr>
<tr>
<td>Input pins ((\text{IN+}, \text{IN-})) (^{(2)})</td>
<td>(V_{EE} - 0.3)</td>
<td>7 V</td>
<td>V</td>
</tr>
<tr>
<td>Current into Input pins ((\text{IN+}, \text{IN-})) (^{(2)})</td>
<td>±10 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output (OUT) (TLV7012) (^{(3)})</td>
<td>(V_{EE} - 0.3)</td>
<td>(V_{CC} + 0.3)</td>
<td>V</td>
</tr>
<tr>
<td>Output (OUT) (TLV7022)</td>
<td>(V_{EE} - 0.3)</td>
<td>7 V</td>
<td>V</td>
</tr>
<tr>
<td>Output short-circuit duration (^{(4)})</td>
<td>10 s</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Junction temperature, (T_J)</td>
<td>150°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage temperature, (T_{stg})</td>
<td>–65°C</td>
<td>150°C</td>
<td>°C</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

\(^{(2)}\) Input terminals are diode-clamped to \(V_{EE}\). Input signals that can swing 0.3V below \(V_{EE}\) must be current-limited to 10mA or less.

\(^{(3)}\) Output maximum is \((V_{CC} + 0.3V)\) or 7V, whichever is less.

\(^{(4)}\) Short-circuit to ground, one comparator per package.

6.3 ESD Ratings

<table>
<thead>
<tr>
<th>(V_{ESD})</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electrostatic discharge</td>
<td>Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (^{(1)})</td>
<td>±2000</td>
</tr>
<tr>
<td></td>
<td>Charged-device model (CDM), per JEDEC specification JESD22-C101 (^{(2)})</td>
<td>±1000</td>
</tr>
</tbody>
</table>

\(^{(1)}\) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

\(^{(2)}\) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.4 Recommended Operating Conditions (Single)
over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage ((V_s = V_{CC} - V_{EE}))</td>
<td>1.6</td>
<td>5.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Input Voltage Range</td>
<td>(V_{EE} - 0.1)</td>
<td>(V_{CC} + 0.2)</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Ambient temperature, (T_A)</td>
<td>–40</td>
<td>125</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>
6.5 Recommended Operating Conditions (Dual)

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage $V_S = V_{CC} - V_{EE}$</td>
<td>1.6</td>
<td>6.5</td>
<td>V</td>
</tr>
<tr>
<td>Input voltage range</td>
<td>$V_{CC} - 0.1$</td>
<td>$V_{EE} + 0.2$</td>
<td>V</td>
</tr>
<tr>
<td>Ambient temperature, $T_A$</td>
<td>-40</td>
<td>125</td>
<td>°C</td>
</tr>
</tbody>
</table>

6.6 Thermal Information (Single)

<table>
<thead>
<tr>
<th>THERMAL METRIC$^{(1)}$</th>
<th>TLV7011/TLV7021</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>DPW (X2SON)</td>
</tr>
<tr>
<td>$R_{JA}$ (Junction-to-ambient thermal resistance)</td>
<td>497.5</td>
</tr>
<tr>
<td>$R_{JC(top)}$ (Junction-to-case (top) thermal resistance)</td>
<td>275.5</td>
</tr>
<tr>
<td>$R_{JB}$ (Junction-to-board thermal resistance)</td>
<td>372.2</td>
</tr>
<tr>
<td>$\Psi_{JT}$ (Junction-to-top characterization parameter)</td>
<td>55.5</td>
</tr>
<tr>
<td>$\Psi_{JB}$ (Junction-to-board characterization parameter)</td>
<td>370.3</td>
</tr>
<tr>
<td>$R_{JC(bot)}$ (Junction-to-case (bottom) thermal resistance)</td>
<td>165.1</td>
</tr>
</tbody>
</table>

$^{(1)}$ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.7 Thermal Information (Dual)

<table>
<thead>
<tr>
<th>THERMAL METRIC$^{(1)}$</th>
<th>TLV7012/TLV7022</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>DGK (VSSOP)</td>
</tr>
<tr>
<td>$R_{JA}$ (Junction-to-ambient thermal resistance)</td>
<td>211.7</td>
</tr>
<tr>
<td>$R_{JC(top)}$ (Junction-to-case (top) thermal resistance)</td>
<td>96.1</td>
</tr>
<tr>
<td>$R_{JB}$ (Junction-to-board thermal resistance)</td>
<td>133.5</td>
</tr>
<tr>
<td>$\Psi_{JT}$ (Junction-to-top characterization parameter)</td>
<td>28.3</td>
</tr>
<tr>
<td>$\Psi_{JB}$ (Junction-to-board characterization parameter)</td>
<td>131.7</td>
</tr>
<tr>
<td>$R_{JC(bot)}$ (Junction-to-case (bottom) thermal resistance)</td>
<td>N/A</td>
</tr>
</tbody>
</table>

$^{(1)}$ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
6.8 Electrical Characteristics (Single)

V_S = 1.8 V to 5 V, V_CM = V_S / 2; minimum and maximum values are at T_A = –40°C to +125°C (unless otherwise noted). Typical values are at T_A = 25°C.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_IN</td>
<td>Input offset voltage</td>
<td>±0.5</td>
<td>±8</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>V_HYS</td>
<td>Hysteresis</td>
<td>1.2</td>
<td>4.2</td>
<td>14</td>
<td>mV</td>
</tr>
<tr>
<td>V_CM</td>
<td>Common-mode voltage range</td>
<td>V_S 2.5 V to 5 V</td>
<td>VEE</td>
<td>VCC - 0.1</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_S 1.8 V to 2.5 V</td>
<td>VEE + 0.1</td>
<td>VCC + 0.1</td>
<td>V</td>
</tr>
<tr>
<td>I_OS</td>
<td>Input offset current</td>
<td>5</td>
<td>pA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_IB</td>
<td>Input bias current</td>
<td>1</td>
<td>pA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_OH</td>
<td>Output voltage high</td>
<td>4.7</td>
<td>4.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V_DL</td>
<td>Output voltage low</td>
<td>120</td>
<td>220</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>I_OKG</td>
<td>Open-drain output leakage current (TLV7021 only)</td>
<td>78</td>
<td>100</td>
<td>pA</td>
<td></td>
</tr>
<tr>
<td>CMRR</td>
<td>Common-mode rejection ratio</td>
<td>78</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PSRR</td>
<td>Power supply rejection ratio</td>
<td>78</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_SC</td>
<td>Short-circuit current</td>
<td>65</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_CC</td>
<td>Supply current</td>
<td>44</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

6.9 Switching Characteristics (Single)

Typical values are at T_A = 25°C, V_CC = 5 V, V_CM = 2.5 V; C_L = 15 pF, input overdrive = 100 mV (unless otherwise noted).

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_PHL</td>
<td>Propagation delay time, high-to-low</td>
<td>260</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>(R_P = 2.5 kΩ TLV7021 only)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t_PLH</td>
<td>Propagation delay time, low-to-high</td>
<td>310</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>(R_P = 2.5 kΩ TLV7021 only)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t_R</td>
<td>Rise time (for TLV7011 only)</td>
<td>5</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>t_F</td>
<td>Fall time</td>
<td>5</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>t_ON</td>
<td>Power-up time (1)</td>
<td>20</td>
<td>µs</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) During power on, V_S must exceed 1.6 V for t_ON before the output tracks the input.
6.10 Electrical Characteristics (Dual)

\( V_S = 1.8 \text{ V to } 5 \text{ V}, V_{CM} = V_S / 2; \) minimum and maximum values are at \( T_A = -40^\circ \text{C} \) to \( +125^\circ \text{C} \) (unless otherwise noted). Typical values are at \( T_A = 25^\circ \text{C} \).

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{IO} )</td>
<td>Input Offset Voltage</td>
<td>( V_S = 1.8 \text{ V and } 5 \text{ V, } V_{CM} = V_S / 2 )</td>
<td>( \pm 0.1 )</td>
<td>( \pm 8 )</td>
<td>mV</td>
</tr>
<tr>
<td>( V_{HYS} )</td>
<td>Hysteresis</td>
<td>( V_S = 1.8 \text{ V and } 5 \text{ V, } V_{CM} = V_S / 2 )</td>
<td>2</td>
<td>7.2</td>
<td>15</td>
</tr>
<tr>
<td>( V_{CM} )</td>
<td>Common-mode voltage range</td>
<td>( V_{EE} )</td>
<td>( V_{CC} )</td>
<td>0.1</td>
<td>V</td>
</tr>
<tr>
<td>( I_I )</td>
<td>Input bias current</td>
<td>2</td>
<td>pA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{OS} )</td>
<td>Input offset current</td>
<td>1</td>
<td>pA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{OH} )</td>
<td>Output voltage high (for TLV7012 only)</td>
<td>( V_S = 5 \text{ V, } V_{EE} = 0 \text{ V, } I_O = 3 \text{ mA} )</td>
<td>4.65</td>
<td>4.8</td>
<td>V</td>
</tr>
<tr>
<td>( V_{OL} )</td>
<td>Output voltage low</td>
<td>( V_S = 5 \text{ V, } V_{EE} = 0 \text{ V, } I_O = 3 \text{ mA} )</td>
<td>250</td>
<td>350</td>
<td>mV</td>
</tr>
<tr>
<td>( I_{KG} )</td>
<td>Open-drain output leakage current (TLV7022 only)</td>
<td>( V_S = 5 \text{ V, } V_{ID} = \pm 0.1 \text{ V (output high), } V_{PULLUP} = V_{CC} )</td>
<td>100</td>
<td></td>
<td>pA</td>
</tr>
<tr>
<td>CMRR</td>
<td>Common-mode rejection ratio</td>
<td>( V_{EE} &lt; V_{CM} &lt; V_{CC}, V_S = 5 \text{ V} )</td>
<td>73</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>PSRR</td>
<td>Power supply rejection ratio</td>
<td>( V_S = 1.8 \text{ V to } 5 \text{ V, } V_{CM} = V_S / 2 )</td>
<td>77</td>
<td></td>
<td>dB</td>
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<tr>
<td>( I_{SC} )</td>
<td>Short-circuit current</td>
<td>( V_S = 5 \text{ V, sourcing (for TLV7012 only) )</td>
<td>29</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_S = 5 \text{ V, sinking )</td>
<td>33</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{CC} )</td>
<td>Supply current / Channel</td>
<td>( V_S = 1.8 \text{ V, no load, } V_{ID} = -0.1 \text{ V (Output Low) )</td>
<td>4.7</td>
<td>9</td>
<td>( \mu \text{A} )</td>
</tr>
</tbody>
</table>

6.11 Switching Characteristics (Dual)

Typical values are at \( T_A = 25^\circ \text{C}, V_S = 5 \text{ V, } V_{CM} = V_S / 2; \) CL = 15 \( \text{pF}, \) input overdrive = 100 \( \text{mV} \) (unless otherwise noted).

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
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<tbody>
<tr>
<td>( t_{PHL} )</td>
<td>Propagation delay time, high to low (( RP = 4.99 \text{ k\Omega} ) TLV7022 only)</td>
<td>Midpoint of input to midpoint of output, ( V_{OD} = 100 \text{ mV} )</td>
<td>310</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{PLH} )</td>
<td>Propagation delay time, low-to high (( RP = 4.99 \text{ k\Omega} ) TLV7022 only)</td>
<td>Midpoint of input to midpoint of output, ( V_{OD} = 100 \text{ mV} )</td>
<td>260</td>
<td></td>
<td>ns</td>
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<tr>
<td>( t_{R} )</td>
<td>Rise time (TLV7012 only)</td>
<td>Measured from 20% to 80%</td>
<td>5</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{F} )</td>
<td>Fall time</td>
<td>Measured from 20% to 80%</td>
<td>5</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{ON} )</td>
<td>Power-up time</td>
<td>During power on, ( V_{CC} \text{ must exceed } 1.6 \text{ V for } 20 \mu \text{ s before the output is in a correct state.} )</td>
<td>20</td>
<td></td>
<td>( \mu \text{s} )</td>
</tr>
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</table>

(1) The lower limit for \( RP \) is 650 \( \Omega \)

6.12 Timing Diagrams

![Timing Diagram](image-url)

Figure 1. Start-Up Time Timing Diagram (IN+ > IN–)
Timing Diagrams (continued)

Figure 2. Propagation Delay Timing Diagram
6.13 Typical Characteristics

\[ T_A = 25^\circ C, V_{CC} = 5 \text{ V}, V_{EE} = 0 \text{ V}, V_{CM} = V_{CC}/2, C_L = 15 \text{ pF} \]

- **Figure 3. Input Offset vs. Temperature**
  - \( V_{CC} = 1.8 \text{ - 5.0V} \)

- **Figure 4. Input Offset Voltage vs. \( V_{CM} \)**
  - \( V_{CC} = 1.8 \text{ V}, 50 \text{ devices} \)

- **Figure 5. Input Offset Voltage vs. \( V_{CM} \)**
  - \( V_{CC} = 3.3 \text{ V}, 50 \text{ devices} \)

- **Figure 6. Input Offset Voltage vs. \( V_{CM} \)**
  - \( V_{CC} = 5 \text{ V}, 50 \text{ devices} \)

- **Figure 7. Input Offset Voltage Histogram**
  - Distribution Taken From 10,777 Comparators
  - \( V_{CC} = 1.8V - 5.0V \)

- **Figure 8. TLV70x1 Hysteresis vs. Temperature**
  - \( V_{CC} = 1.8V - 5.0V \)
Typical Characteristics (continued)

\[ T_A = 25^\circ C, \ V_{CC} = 5 \ V, \ V_{EE} = 0 \ V, \ V_{CM} = V_{CC}/2, \ C_L = 15 \ pF \]

\[ V_{CC} = 5.0V \]

\[ V_{CC} = 1.8V - 5.0V \]

\[ V_{CC} = 3.3V \]

\[ V_{CC} = 1.8V \]

\[ V_{CM} = 0V \]
\[ V_{CM} = V_{CC}/2 \]
\[ V_{CM} = V_{CC} \]

Figure 9. TLV70x1 Hysteresis vs. \( V_{CM} \)

Figure 10. TLV70x1 Hysteresis Histogram

Figure 11. TLV70x2 Hysteresis vs. Temperature

Figure 12. TLV70x2 Hysteresis vs. \( V_{CM} \)

Figure 13. Input Bias Current vs. Temperature

Figure 14. TLV701x Output Voltage High vs. Output Source Current
Typical Characteristics (continued)

$T_A = 25°C$, $V_{CC} = 5 V$, $V_{EE} = 0 V$, $V_{CM} = V_{CC}/2$, $C_L = 15 \text{pF}$

Figure 15. TLV701x Output Voltage High vs. Output Source Current

Figure 16. Output Voltage Low vs. Output Sink Current

Figure 17. Output Voltage Low vs. Output Sink Current

Figure 18. Output Short-Circuit (Sink) Current vs. Temperature

Figure 19. TLV701x Output Short-Circuit (Source) Current vs. Temperature

Figure 20. Output Short Circuit (Sink) vs. $V_{CC}$
Typical Characteristics (continued)

$T_A = 25^\circ C$, $V_{CC} = 5 \, V$, $V_{EE} = 0 \, V$, $V_{CM} = V_{CC}/2$, $C_L = 15 \, pF$

$V_{CM} = V_{CC}/2$

Figure 21. TLV701x Output Short Circuit (Source) vs. $V_{CC}$

$V_{CM} = V_{CC}/2$

Figure 22. $I_{CC}$ vs. Temperature

$V_{CM} = V_{CC}/2$

Figure 23. $I_{CC}$ vs. $V_{CC}$

$V_{OD} = 100\, mV$

Figure 25. TLV701x Output Rise Time vs. Load Capacitance

$V_{OD} = 100\, mV$

Figure 26. Output Fall Time vs. Load Capacitance
Typical Characteristics (continued)

$T_A = 25°C$, $V_{CC} = 5 V$, $V_{EE} = 0 V$, $V_{CM} = V_{CC}/2$, $C_L = 15$ pF

**Figure 27. TLV701x Propagation Delay (L-H) vs. Input Overdrive**

$V_{CC} = 5 V$

**Figure 29. TLV701x Propagation Delay (L-H) vs. Input Overdrive**

$R_{pull-up} = 2.5k$

**Figure 31. TLV702x Propagation Delay (L-H) vs. Input Overdrive**
7 Detailed Description

7.1 Overview

The TLV701x and TLV702x devices are single-channel, micro-power comparators with push-pull and open-drain outputs. Operating down to 1.6 V and consuming only 5 µA, the TLV701x and TLV702x are ideally suited for portable and industrial applications. The comparators are available in leadless and leaded packages to offer significant board space saving in space-challenged designs.

7.2 Functional Block Diagram

![Functional Block Diagram](image)

7.3 Feature Description

The TLV701x (push-pull) and TLV702x (open-drain) devices are micro-power comparators that are capable of operating at low voltages. The TLV701x and TLV702x feature a rail-to-rail input stage capable of operating up to 100 mV beyond the VCC power supply rail. The comparators also feature a push-pull and open-drain output stage with internal hysteresis.

7.4 Device Functional Modes

The TLV701x and TLV702x have a Power-on-Reset (POR) circuit. While the power supply (V_S) is ramping up or ramping down, the POR circuitry will be activated.

For the TLV701x, the POR circuit will hold the output low (at V_{EE}) while activated.

For the TLV702x, the POR circuit will keep the output high impedance (logical high) while activated.

When the supply voltage is greater than, or equal to, the minimum supply voltage, the comparator output reflects the state of the differential input (V_{ID}).

7.4.1 Inputs

The TLV701x and TLV702x input common-mode extends from V_{EE} to 100 mV above V_{CC}. The differential input voltage (V_{ID}) can be any voltage within these limits. No phase-inversion of the comparator output will occur when the input pins exceed V_{CC} and V_{EE}. 
Device Functional Modes (continued)

While TI recommends operating the TLV701x and TLV702x within the specified common-mode range, the inputs are fault tolerant to voltages up to 5.5 V independent of the applied $V_{CC}$ value. Fault tolerant is defined as maintaining the same high input impedance when $V_{CC}$ is unpowered or within the recommended operating range. Because the inputs of the TLV701x and TLV702x are fault tolerant, the inputs to the comparator can be any value between 0 V and 5.5 V while $V_{CC}$ is ramping up. This feature allows any supply and input driven sequence as long as the input value and supply are within the specified ranges. In this case, no current limiting resistor is required. This is possible since the $V_{CC}$ is isolated from the inputs such that it maintains its value even when a higher voltage is applied to the input.

The input bias current is typically 1 pA for input voltages between $V_{CC}$ and $V_{EE}$. The comparator inputs are protected from undervoltage by internal diodes connected to $V_{EE}$. As the input voltage goes under $V_{EE}$, the protection diodes become forward biased and begin to conduct causing the input bias current to increase exponentially. Input bias current typically doubles for 10°C temperature increases.

### 7.4.2 Internal Hysteresis

The device hysteresis transfer curve is shown in Figure 32. This curve is a function of three components: $V_{TH}$, $V_{OS}$, and $V_{HYST}$:

- $V_{TH}$ is the actual set voltage or threshold trip voltage.
- $V_{OS}$ is the internal offset voltage between $V_{IN+}$ and $V_{IN-}$. This voltage is added to $V_{TH}$ to form the actual trip point at which the comparator must respond to change output states.
- $V_{HYST}$ is the internal hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise (4.2 mV for the TLV7011).

![Hysteresis Transfer Curve](image)

#### Figure 32. Hysteresis Transfer Curve

### 7.4.3 Output

The TLV701x feature a push-pull output stage eliminating the need for an external pull-up resistor. On the other hand, the TLV702x feature an open-drain output stage enabling the output logic levels to be pulled up to an external source independent of the supply voltage.
8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV701x and TLV702x are micro-power comparators with reasonable response time. The comparators have a rail-to-rail input stage that can monitor signals beyond the positive supply rail with integrated hysteresis. When higher levels of hysteresis are required, positive feedback can be externally added. The push-pull output stage of the TLV701x is optimal for reduced power budget applications and features no shoot-through current. When level shifting or wire-ORing of the comparator outputs is needed, the TLV702x with its open-drain output stage is well suited to meet the system needs. In either case, the wide operating voltage range, low quiescent current, and micro-package of the TLV701x and TLV702x make these comparators excellent candidates for battery-operated and portable, handheld designs.

8.1.1 Inverting Comparator With Hysteresis for TLV701x

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage (V\text{CC}), as shown in Figure 33. When V\text{IN} at the inverting input is less than V\text{A}, the output voltage is high (for simplicity, assume V\text{O} switches as high as V\text{CC}). The three network resistors can be represented as R1 || R3 in series with R2. Equation 1 defines the high-to-low trip voltage (V\text{A1}).

\[
V_{A1} = \frac{V_{CC} \times R_2}{(R_1 || R_3) + R_2}
\]  

(1)

When V\text{IN} is greater than V\text{A}, the output voltage is low, very close to ground. In this case, the three network resistors can be presented as R2 || R3 in series with R1. Use Equation 2 to define the low to high trip voltage (V\text{A2}).

\[
V_{A2} = \frac{V_{CC} \times R_2 || R_3}{R_1 + (R_2 || R_3)}
\]  

(2)

Equation 3 defines the total hysteresis provided by the network.

\[
\Delta V_A = V_{A1} - V_{A2}
\]  

(3)

Figure 33. TLV701x in an Inverting Configuration With Hysteresis
Application Information (continued)

8.1.2 Noninverting Comparator With Hysteresis for TLV701x

A noninverting comparator with hysteresis requires a two-resistor network, as shown in Figure 34, and a voltage reference ($V_{REF}$) at the inverting input. When $V_{IN}$ is low, the output is also low. For the output to switch from low to high, $V_{IN}$ must rise to $V_{IN1}$. Use Equation 4 to calculate $V_{IN1}$.

$$V_{IN1} = R1 \times \frac{V_{REF}}{R2} + V_{REF}$$  \hspace{1cm} (4)

When $V_{IN}$ is high, the output is also high. For the comparator to switch back to a low state, $V_{IN}$ must drop to $V_{IN2}$ such that $V_A$ is equal to $V_{REF}$. Use Equation 5 to calculate $V_{IN2}$.

$$V_{IN2} = \frac{V_{REF} (R1 + R2) - V_{CC} \times R1}{R2}$$  \hspace{1cm} (5)

The hysteresis of this circuit is the difference between $V_{IN1}$ and $V_{IN2}$, as shown in Equation 6.

$$\Delta V_{IN} = V_{CC} \times \frac{R1}{R2}$$  \hspace{1cm} (6)

Figure 34. TLV701x in a Noninverting Configuration With Hysteresis
8.2 Typical Applications

8.2.1 Window Comparator

Window comparators are commonly used to detect undervoltage and overvoltage conditions. Figure 35 shows a simple window comparator circuit.

![Figure 35. Window Comparator](image)

8.2.1.1 Design Requirements

For this design, follow these design requirements:

- Alert (logic low output) when an input signal is less than 1.1 V
- Alert (logic low output) when an input signal is greater than 2.2 V
- Alert signal is active low
- Operate from a 3.3-V power supply

8.2.1.2 Detailed Design Procedure

Configure the circuit as shown in Figure 35. Connect $V_{CC}$ to a 3.3-V power supply and $V_{EE}$ to ground. Make R1, R2 and R3 each 10-MΩ resistors. These three resistors are used to create the positive and negative thresholds for the window comparator ($V_{TH^+}$ and $V_{TH^-}$). With each resistor being equal, $V_{TH^+}$ is 2.2 V and $V_{TH^-}$ is 1.1 V. Large resistor values such as 10-MΩ are used to minimize power consumption. The sensor output voltage is applied to the inverting and noninverting inputs of the two TLV702x's. The TLV7021 is used for its open-drain output configuration. Using the TLV702x allows the two comparator outputs to be Wire-Ored together. The respective comparator outputs will be low when the sensor is less than 1.1 V or greater than 2.2 V. $V_{OUT}$ will be high when the sensor is in the range of 1.1 V to 2.2 V.
Typical Applications (continued)

8.2.1.3 Application Curve

![Application Curve Diagram]

Figure 36. Window Comparator Results

8.2.2 IR Receiver Analog Front End

A single TLV7011 device can be used to build a complete IR receiver analog front end (AFE). The nanoamp quiescent current and low input bias current make it possible to be powered with a coin cell battery, which could last for years.

![IR Receiver Analog Front End Diagram]

Figure 37. IR Receiver Analog Front End Using TLV7011
Typical Applications (continued)

8.2.2.1 Design Requirements

For this design, follow these design requirements:

- Use a proper resistor ($R_1$) value to generate an adequate signal amplitude applied to the inverting input of the comparator.
- The low input bias current $I_B$ (2 pA typical) ensures that a greater value of $R_1$ to be used.
- The RC constant value ($R_2$ and $C_1$) must support the targeted data rate (that is, 9,600 bauds) to maintain a valid tripping threshold.
- The hysteresis introduced with $R_3$ and $R_4$ helps to avoid spurious output toggles.

8.2.2.2 Detailed Design Procedure

The IR receiver AFE design is highly streamlined and optimized. $R_1$ converts the IR light energy induced current into voltage and applies to the inverting input of the comparator. Because a reverse biased IR LED is used as the IR receiver, a higher I/V transimpedance gain is required to boost the amplitude of reduced current. A 10M resistor is used as $R_1$ to support a 1-V, 100-nA transimpedance gain. This is made possible with the picoamps input bias current $I_B$ (5pA typical). The RC network of $R_2$ and $C_1$ establishes a reference voltage $V_{ref}$ which tracks the mean amplitude of the IR signal. The RC constant of $R_2$ and $C_1$ (about 4.7 ms) is chosen for $V_{ref}$ to track the received IR current fluctuation but not the actual data bit stream. The noninverting input is connected to $V_{ref}$ and the output over the $R_3$ and $R_4$ resistor network which provides additional hysteresis for improved guard against spurious toggles.

To reduce the current drain from the coin cell battery, data transmission must be short and infrequent.

8.2.2.3 Application Curve

![Figure 38. IR Receiver AFE Waveforms](image-url)
Typical Applications (continued)

8.2.3 Square-Wave Oscillator

Square-wave oscillator can be used as low cost timing reference or system supervisory clock source.

![Square-Wave Oscillator Diagram](image)

**Figure 39. Square-Wave Oscillator**

8.2.3.1 Design Requirements

The square-wave period is determined by the RC time constant of the capacitor and resistor. The maximum frequency is limited by propagation delay of the device and the capacitance load at the output. The low input bias current allows a lower capacitor value and larger resistor value combination for a given oscillator frequency, which may help to reduce BOM cost and board space.

8.2.3.2 Detailed Design Procedure

The oscillation frequency is determined by the resistor and capacitor values. The following calculation provides details of the steps.

![Square-Wave Oscillator Timing Thresholds](image)

**Figure 40. Square-Wave Oscillator Timing Thresholds**

First consider the output of Figure 39 is high which indicates the inverted input $V_C$ is lower than the noninverting input ($V_A$). This causes the $C_1$ to be charged through $R_4$, and the voltage $V_C$ increases until it is equal to the noninverting input. The value of $V_A$ at the point is calculated by Equation 7.

$$V_{A1} = \frac{V_{CC} \times R_2}{R_2 + R_1 R_3}$$

(7)

if $R_1 = R_2 = R_3$, then $V_{A1} = 2 \frac{V_{CC}}{3}$
Typical Applications (continued)

At this time the comparator output trips pulling down the output to the negative rail. The value of $V_A$ at this point is calculated by Equation 8.

$$V_{A2} = \frac{V_{CC}(R_2IR_3)}{R_1+R_2IR_3} \quad (8)$$

if $R_1 = R_2 = R_3$, then $V_{A2} = V_{CC}/3$

The $C_1$ now discharges though the $R_4$, and the voltage $V_{CC}$ decreases until it reaches $V_{A2}$. At this point, the output switches back to the starting state. The oscillation period equals to the time duration from for $C_1$ from $2V_{CC}/3$ to $V_{CC}/3$ then back to $2V_{CC}/3$, which is given by $R_4C_1 \times \ln 2$ for each trip. Therefore, the total time duration is calculated as $2R_4C_1 \times \ln 2$. The oscillation frequency can be obtained by Equation 9:

$$f = \frac{1}{(2 \ R_4 \times C_1 \times \ln 2)} \quad (9)$$

8.2.3.3 Application Curve

Figure 41 shows the simulated results of tan oscillator using the following component values:

- $R_1 = R_2 = R_3 = R_4 = 100 \text{ k}\Omega$
- $C_1 = 100 \text{ pF}$, $C_L = 20 \text{ pF}$
- $V+ = 5 \text{ V}$, $V– = \text{GND}$
- $C_{\text{stray}}$ (not shown) from $V_A$ TO GND = 10 pF

Figure 41. Square-Wave Oscillator Output Waveform
9 Power Supply Recommendations

The TLV701x and TLV702x have a recommended operating voltage range (V_S) of 1.6 V to 5.5 / 6.5 V. V_S is defined as V_{CC} – V_{EE}. Therefore, the supply voltages used to create V_S can be single-ended or bipolar. For example, single-ended supply voltages of 5 V and 0 V and bipolar supply voltages of +2.5 V and –2.5 V create comparable operating voltages for V_S. However, when bipolar supply voltages are used, it is important to realize that the logic low level of the comparator output is referenced to V_{EE}.

Output capacitive loading and output toggle rate will cause the average supply current to rise over the quiescent current.

10 Layout

10.1 Layout Guidelines

To reduce PCB fabrication cost and improve reliability, TI recommends using a 4-mil via at the center pad connected to the ground trace or plane on the bottom layer.

A power-supply bypass capacitor of 100 nF is recommended when supply output impedance is high, supply traces are long, or when excessive noise is expected on the supply lines. Bypass capacitors are also recommended when the comparator output drives a long trace or is required to drive a capacitive load. Due to the fast rising and falling edge rates and high-output sink and source capability of the TLV7011 and TLV7021 output stages, higher than normal quiescent current can be drawn from the power supply. Under this circumstance, the system would benefit from a bypass capacitor across the supply pins.

10.2 Layout Example

![Layout Example Diagram]

Figure 42. Layout Example
11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Module

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TLV70x1 device family. The TLV7011 Micro-Power Comparator Dip Adaptor Evaluation Module can be requested at the Texas Instruments website through the product folder or purchased directly from the TI eStore.

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

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</table>

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.5 Trademarks

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11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

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<th>Op Temp (°C)</th>
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(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.
(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead finish/Ball material** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION

### REEL DIMENSIONS

- **Reel Diameter**
- **Reel Width (W1)**
- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

### TAPE DIMENSIONS

- **Cavity**
- **A0**
- **B0**
- **K0**
- **W**

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

- **Pocket Quadrants**
- **Sprocket Holes**
- **User Direction of Feed**

### Pack Materials-Page 1

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*All dimensions are nominal*
### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

2. This drawing is subject to change without notice.

3. Referne CEDEC MO-203.

4. Support pin may differ or may not be present.

5. Lead width does not comply with JEDEC.

6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side.
NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

10. Board assembly site may have different recommendations for stencil design.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

PowerPAD is a trademark of Texas Instruments.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.
Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).
NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.
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