TLV709 150mA, 30V, 3.2µA Quiescent Current, Low-Dropout Linear Regulator

1 Features

- Input voltage range: 2.5V to 30V
- Available output voltage options:
  - Fixed: 1.2V to 5V
  - Adjustable: 1.2V to 28V
- Output current: Up to 150mA
- Very-low I_Q: 3.2µA at 150mA load current
- Stable with output capacitor ≥ 0.47µF
- Overcurrent protection
- Packages:
  - 4-pin SOT-89 (PK) (fixed configuration only)
  - 5-pin SOT-23 (DBV) (both fixed and adjustable configurations)
- Operating junction temperature: –40°C to +125°C

2 Applications

- Home and building automation
- Retail automation and payment
- Grid infrastructure
- Medical applications
- Lighting applications

3 Description

The TLV709 low-dropout (LDO) linear voltage regulator is a low quiescent current device. This device offers the benefits of a wide input voltage range and low-power operation in miniaturized packaging. The TLV709 is optimized to power microcontrollers and other low power loads for battery-powered applications.

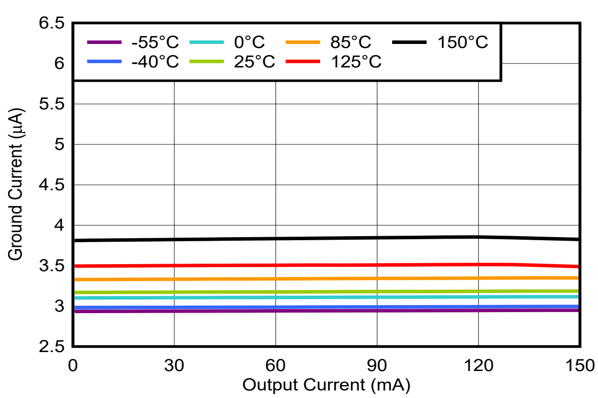
The TLV709 LDO supports a low dropout of typically 600mV at 100mA of load current. The low quiescent current (3.2µA typically) does not vary across the entire range of output load current (0mA to 150mA). The TLV709 also features an internal soft-start to lower inrush current during start-up. The built-in overcurrent limit protection helps protect the regulator in the event of a load short or fault condition.

The TLV709 is available in a 2.9mm × 2.8mm, 5-pin SOT-23 (DBV) package for fixed and adjustable outputs. The TLV709 is also available in a 4.5mm × 2.5mm, 3-pin SOT-89 (PK) package for fixed outputs.

Package Information

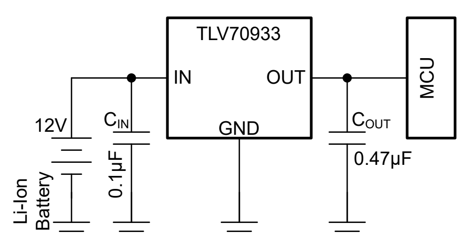
PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TLV709	DBV (SOT-23, 5)	2.9mm × 2.8mm
	PK (SOT-89, 3)	4.5mm × 4.095mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



V_{IN} = 4.3V, V_{OUT} = 3.3V

Quiescent Current vs Load Current



Typical Application

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4 Pin Configuration and Functions

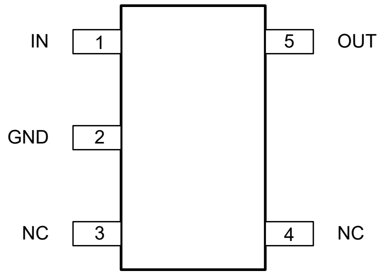


Figure 4-1. DBV Package (Fixed), 5-Pin SOT-23 (Top View)

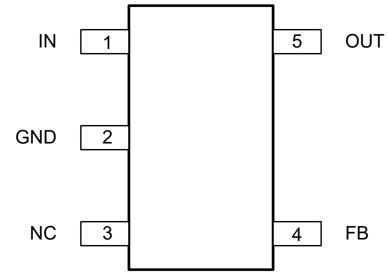


Figure 4-2. DBV Package (Adjustable), 5-Pin SOT-23 (Top View)

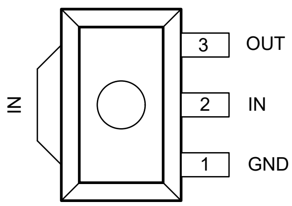


Figure 4-3. TLV709xxPKR PK Package (IN Tab), 3-Pin SOT-89 (Top View)

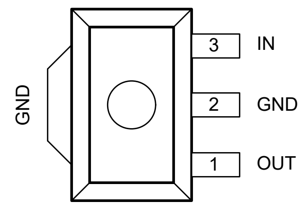


Figure 4-4. TLV709AxxPKR PK Package (GND Tab), 3-Pin SOT-89 (Top View)

Table 4-1. Pin Functions

PIN					TYPE	DESCRIPTION
NAME	DBV (Fixed)	DBV (Adj)	PK (IN Tab)	PK (GND Tab)		
GND	2	2	1	2, tab	—	Ground pin.
IN	1	1	2, tab	3	I	Input supply pin. See the *Recommended Operating Conditions* table and the *Input and Output Capacitor Requirements* section for more information.
OUT	5	5	3	1	O	Output of the regulator. See the *Recommended Operating Conditions* table and the *Input and Output Capacitor Requirements* section for more information.
FB	—	4	—	—	I	In the adjustable configuration, this pin sets the output voltage with the help of a feedback divider.
NC	3, 4	3	—	—	—	Not internally connected. Leave this pin open or tied to ground for improved thermal performance.

5 Specifications

5.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)[1] [2]

		MIN	MAX	UNIT
Voltage	V_{IN}	–0.3	30	V
	V_{OUT} (for fixed device only)	–0.3	2 × $V_{OUT(typ)}$ or V_{IN} + 0.3 or 5.5 (whichever is lower)	
	V_{OUT} (for adjustable device only)	–0.3	V_{IN} + 0.3	
	V_{FB}	–0.3	2.4	
Current	Peak output current	Internally limited		
Temperature	Junction, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the ground terminal.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	2.5		30	V
V_{OUT}	Output voltage (for adjustable device only)	1.205		28	
	Output voltage (for fixed device only)	1.205		5.0	
I_{OUT}	Output current	0		150	mA
C_{IN}	Input capacitor[2]		0.47		µF
C_{OUT}	Output capacitor[3]	1			
T_J	Operating junction temperature	–40		125	°C

(1) All voltages are with respect to GND.
(2) An input capacitor is not required for LDO stability. However, an input capacitance with an effective value of 0.1µF minimum is recommended to counteract the effect of source resistance and inductance, which may in some cases cause symptoms of systemlevel instability such as ringing or oscillation, especially in the presence of load transients.
(3) All capacitor values listed are the nominal value and the effective capacitance is assumed to derate to 50% of the nominal capacitor value.

5.4 Thermal Information

THERMAL METRIC[1]		TLV709 [2]			UNIT
		DBV [SOT-23]	PK [SOT-89]	AxxPK [SOT-89]	
		5 PINS	4 PINS	4 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	195.7	131.7	72.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	88.2	65.8	121.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.7	32.4	37.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	11.2	69.8	29.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	40.5	96.2	36.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC package thermal metrics application note.
(2) Thermal performance results are based on the JEDEC standard of 2s2p PCB configuration. These thermal metric parameters can be further improved by 35-55% based on thermally optimized PCB layout designs. See the analysis of the Impact of board layout on LDO thermal performance application note.

5.5 Electrical Characteristics

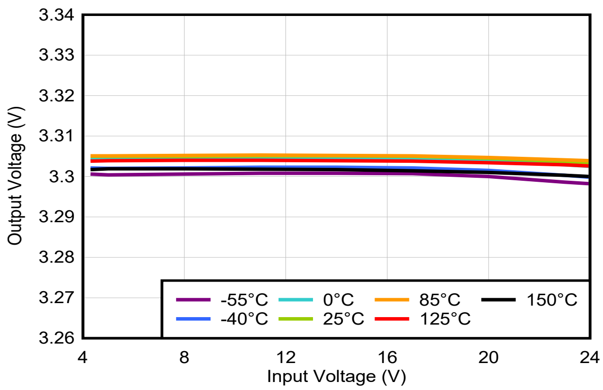
over operating junction temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 1V, I_{OUT} = 100µA, and C_{OUT} = 1µF (unless otherwise noted); typical values are at T_J = 25°C [(1)]

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage [(2)]		I_O = 10mA	2.5		30	V
			10mA ≤ I_O < 50mA	3.0		30	
			50mA ≤ I_O ≤ 150mA	3.5		30	
V_{OUT}	Output voltage range (TLV709A01)			1.205		28	V
V_{FB}	Internal reference [(2)]			1.152	1.205	1.24	
V_{OUT} [(5)]	Output voltage accuracy [(1) (2) (3)]	Over V_{IN}, I_{OUT}, and temp	V_{OUT} + 1.0V ≤ V_{IN} ≤ 30V 100µA ≤ I_{OUT} ≤ 150mA	–4		4	%
		Over V_{IN}, temp and I_{OUT} = 10mA	V_{OUT} + 1.0V ≤ V_{IN} ≤ 30V I_{OUT} = 10mA	-4		4	
		Over V_{IN} , I_{OUT}, and T_J = 25℃	V_{OUT} + 1V ≤ V_{IN} ≤ 30V 100µA ≤ I_{OUT} ≤ 150mA and T_J = 25℃	–2		2	
I_{GND}	Ground pin current[(1) (4)]		I_{OUT} = 0mA		3.2		µA
			100µA ≤ I_{OUT} ≤ 150mA , V_{IN} = 30V			10	
	Ground pin current[(1) (4)] (For A version only)		100µA ≤ I_{OUT} ≤ 150mA , T_J = –40°C to 85°C		3.2	4.2	
			100µA ≤ I_{OUT} ≤ 150mA		3.2	4.8	
	Ground pin current[(1) (4)] (For non-A version only)		100µA ≤ I_{OUT} ≤ 150mA , T_J = –40°C to 85°C		3.4	4.3	
			100µA ≤ I_{OUT} ≤ 150mA		3.4	5.8	
$\Delta V_{OUT\ (\Delta IOUT)}$	Load regulation [(1)]		V_{OUT} ≥ 3.3V, 100µA < I_{OUT} < 10mA		1		%/A
			V_{OUT} ≥ 3.3V, 100µA < I_{OUT} < 50mA		1		
			V_{OUT} ≥ 3.3V, 100µA < I_{OUT} < 150mA		1	2.5	
$\Delta V_{OUT\ (\Delta VIN)}$	Line regulation [(2)]		$V_{OUT(NOM)}$ + 1V ≤ V_{IN} ≤ 30V		0.02	0.05	%/V
V_n	Output noise voltage	BW = 10Hz to 100kHz, C_{OUT} = 10µF	I_{OUT} = 1mA		487		µVrms
			I_{OUT} = 50mA		577		
I_{CL}	Output current limit		V_{OUT} = 0V, V_{IN} ≥ 3.5V	160		1000	mA
			V_{OUT} = 0V, V_{IN} < 3.5V	90		1000	
PSRR	Power-supply ripple rejection		f = 100kHz, C_{OUT} = 10µF		60		dB
V_{DO}	Dropout voltage		V_{IN} = $V_{OUT(nom)}$ – 0.1V, I_{OUT} = 10mA		75	150	mV
			V_{IN} = $V_{OUT(nom)}$ – 0.1V, I_{OUT} = 50mA		400		
			V_{IN} = $V_{OUT(nom)}$ – 0.1V, I_{OUT} = 150mA		1000	1600	

(1) TLV709 is stable and fuctional over the entire load current range from 0mA to I_{CL}.
(2) Minimum V_{IN} = V_{OUT} + 1V or the value shown for *Input voltage* in this table, whichever is greater.
(3) For adjustable device, output accuracy excludes the tolerance and mismatch associated with external resistors used for setting up the output voltage.
(4) See Leakage null control circuit . The TLV709 employs a leakage null control circuit. This circuit is active only if output current is less than pass transistor leakage current. The circuit is typically active when output load is less than 5µA, V_{IN} is greater than 18V, and die temperature is greater than 100°C.
(5) Minimum V_{IN} used for I_{OUT} = 150mA is V_{OUT} + 1.6V.

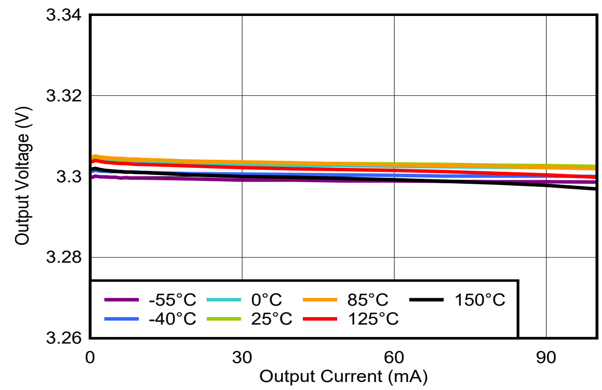
5.6 Typical Characteristics

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0V or 2.5V (whichever is greater), V_{OUT}(typ) = 3.3V, I_{OUT} = 1mA, C_{IN} = 1µF, and C_{OUT} = 1µF (unless otherwise noted)



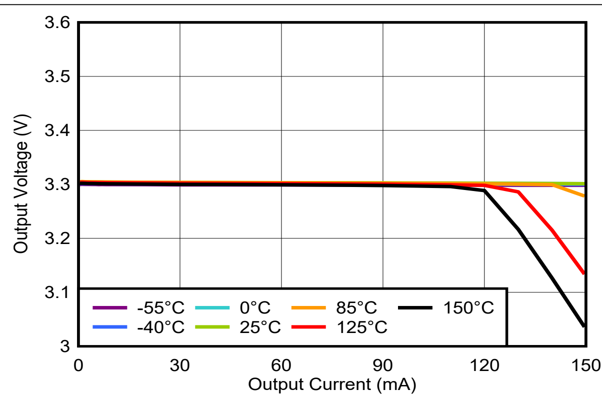
V_{OUT} = 3.3V, I_{OUT} = 5mA

Figure 5-1. Line Regulation



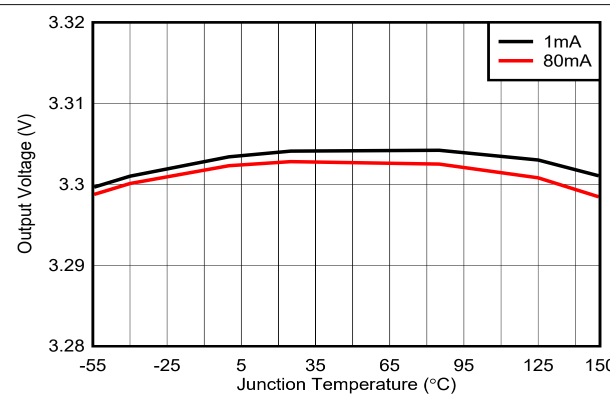
V_{IN} = 4.3V, V_{OUT} = 3.3V, 0mA ≤ I_{OUT} ≤ 100mA

Figure 5-2. Load Regulation



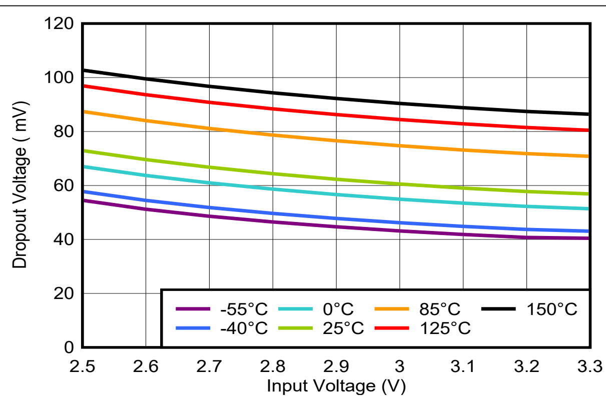
V_{IN} = 4.3V, V_{OUT} = 3.3V, 0mA ≤ I_{OUT} ≤ 150mA

Figure 5-3. Load Regulation



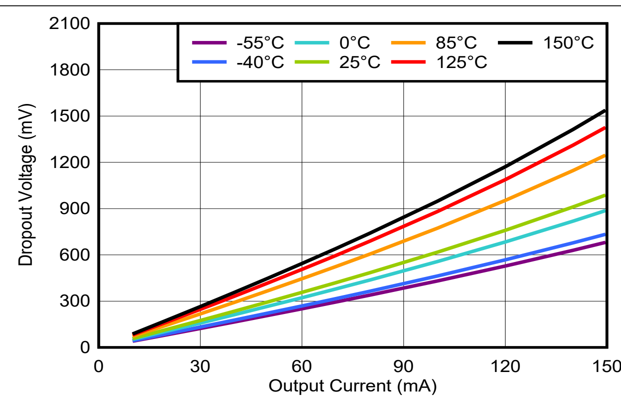
V_{IN} = 4.3V, V_{OUT} = 3.3V

Figure 5-4. V_{OUT} vs Temperature and I_{OUT}



V_{OUT} = 3.3V, I_{OUT} = 10mA

Figure 5-5. V_{DO} vs V_{IN}

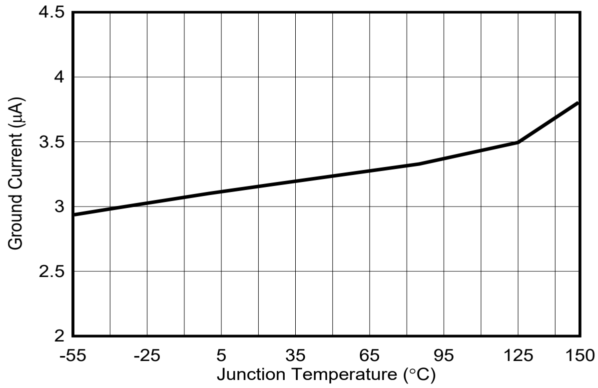


V_{OUT} = 3.3V

Figure 5-6. V_{DO} vs I_{OUT}

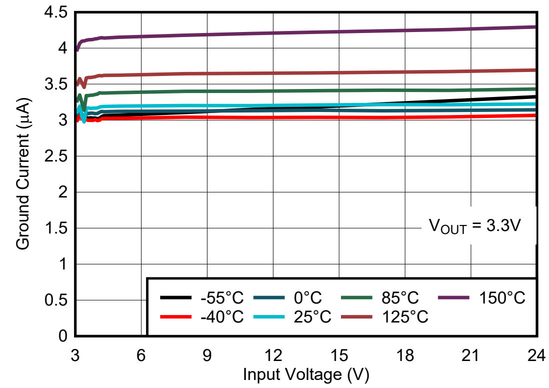
5.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0V or 2.5V (whichever is greater), V_{OUT}(typ) = 3.3V, I_{OUT} = 1mA, C_{IN} = 1µF, and C_{OUT} = 1µF (unless otherwise noted)



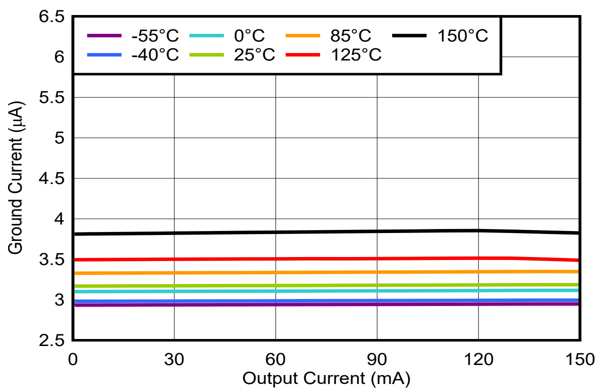
V_{IN} = 4.3V, V_{OUT} = 3.3V, I_{OUT} = 0mA, C_{OUT} = 1µF

Figure 5-7. Ground Current vs Temperature



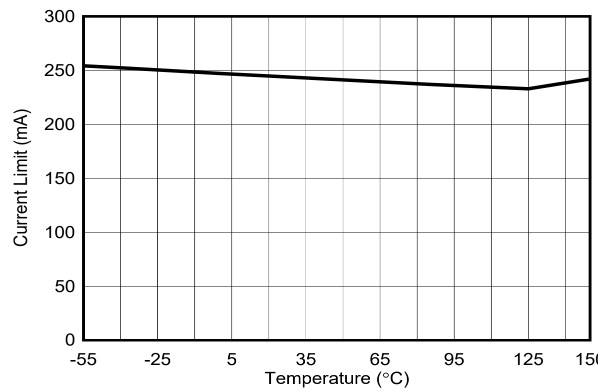
V_{OUT} = 3.3V, I_{OUT} = 0mA, C_{OUT} = 1µF

Figure 5-8. Ground Current vs V_{IN}



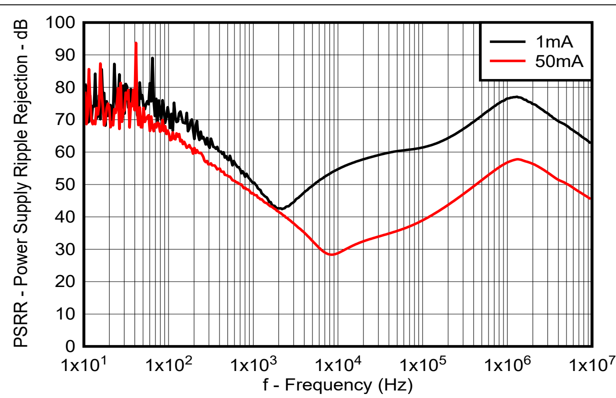
V_{IN} = 4.3V, V_{OUT} = 3.3V, C_{OUT} = 1µF

Figure 5-9. Ground Current vs I_{OUT}



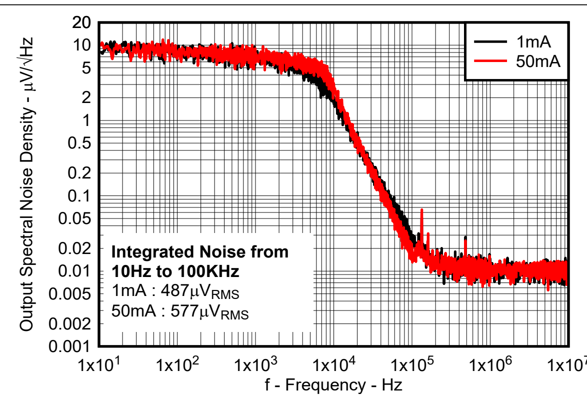
V_{IN} = 4.8V, V_{OUT} = 3.3V

Figure 5-10. I_{CL} vs Temperature



V_{IN} = 4.3V, V_{OUT} = 3.3V, C_{OUT} = 10µF

Figure 5-11. PSRR vs Frequency

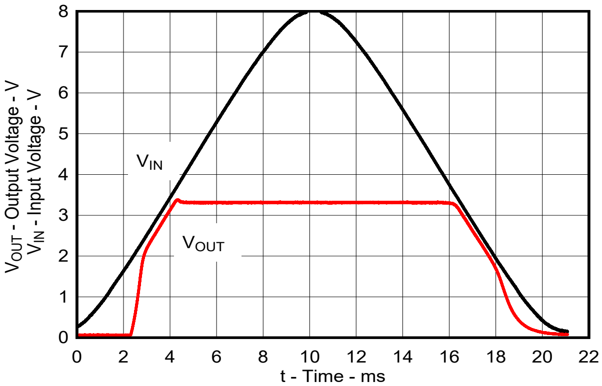


V_{IN} = 4.3V, V_{OUT} = 3.3V, C_{OUT} = 10µF

Figure 5-12. Output Noise (V_N) vs Frequency

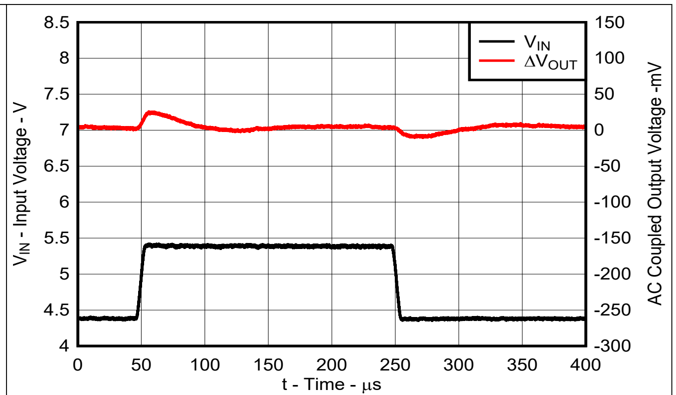
5.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0V or 2.5V (whichever is greater), V_{OUT}(typ) = 3.3V, I_{OUT} = 1mA, C_{IN} = 1µF, and C_{OUT} = 1µF (unless otherwise noted)



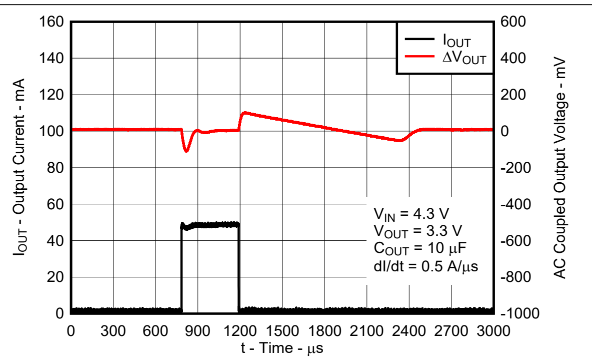
V_{IN} = 4.3V, V_{OUT} = 3.3V, C_{OUT} = 10µF, I_{OUT} = 50mA

Figure 5-13. Power-Up, Power-Down With V_{IN} Ramp



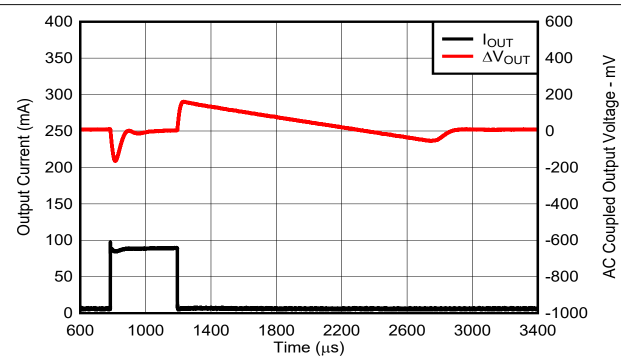
V_{OUT} = 3.3V, C_{OUT} = 10µF, ramp rate = 0.2V/µs

Figure 5-14. V_{IN} Line Transient Response (4.3V to 5.3V)



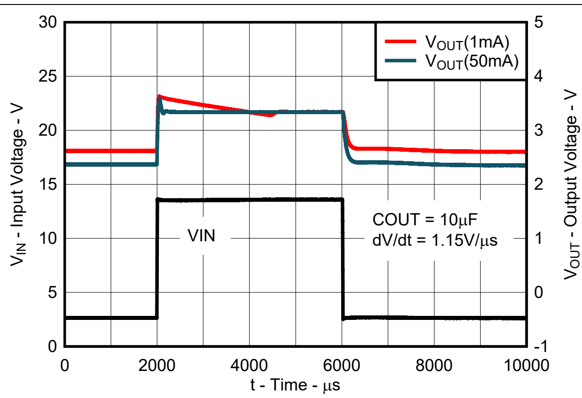
V_{IN} = 4.3V, V_{OUT} = 3.3V, C_{OUT} = 10µF, ramp rate = 0.5A/µs

Figure 5-15. I_{OUT} Transient From 1mA to 50mA



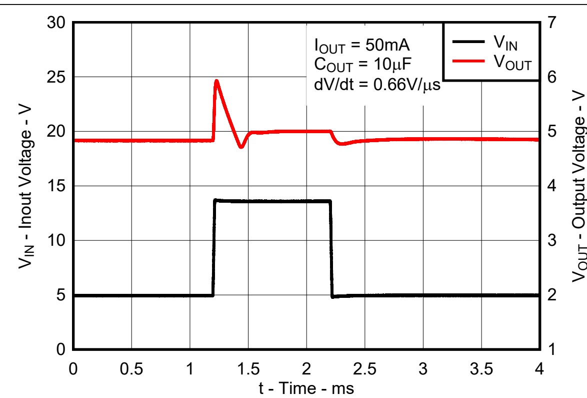
V_{IN} = 4.3V, V_{OUT} = 3.3V, C_{OUT} = 10µF ramp rate = 0.5A/µs

Figure 5-16. I_{OUT} Transient From 1mA to 80mA



V_{OUT} = 5V, C_{OUT} = 10µF, ramp rate = 1.15V/µs

Figure 5-17. Dropout Exit Line Transient (2.5V to 14V for V_{OUT} = 5V)



V_{OUT} = 5V, C_{OUT} = 10µF, ramp rate = 0.66V/µs

Figure 5-18. V_{IN} Line Transient (5V to 14V for V_{OUT} = 5V)

6 Detailed Description

6.1 Overview

The TLV709 low-dropout regulator (LDO) consumes only 3.2µA (typ) of quiescent current across the entire output current range. The device offers a wide input voltage range and low-dropout voltage in small packaging. The device, which operates over an input range of 2.5V to 30V, is stable with any output capacitor greater than or equal to 1µF. The low quiescent current across the complete load current range makes the TLV709 designed for powering battery-operated applications. The TLV709 has an internal soft-start to control inrush current into the output capacitor. This LDO also has overcurrent protection during a load-short or fault condition on the output.

6.2 Functional Block Diagrams

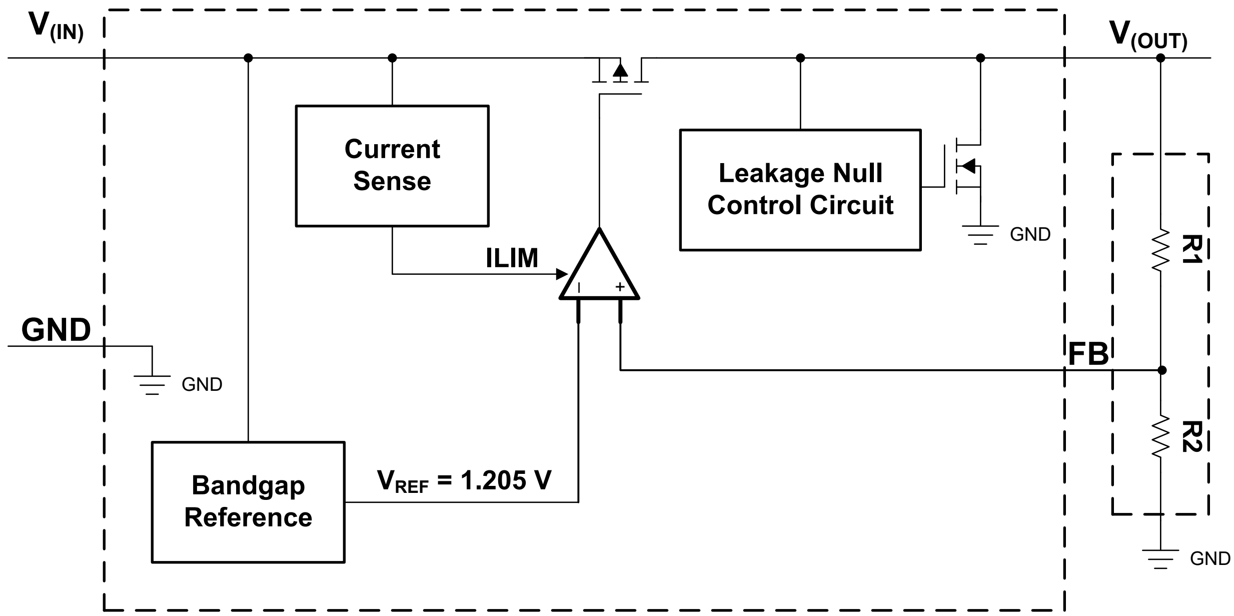


Figure 6-1. Functional Block Diagram: Adjustable Version

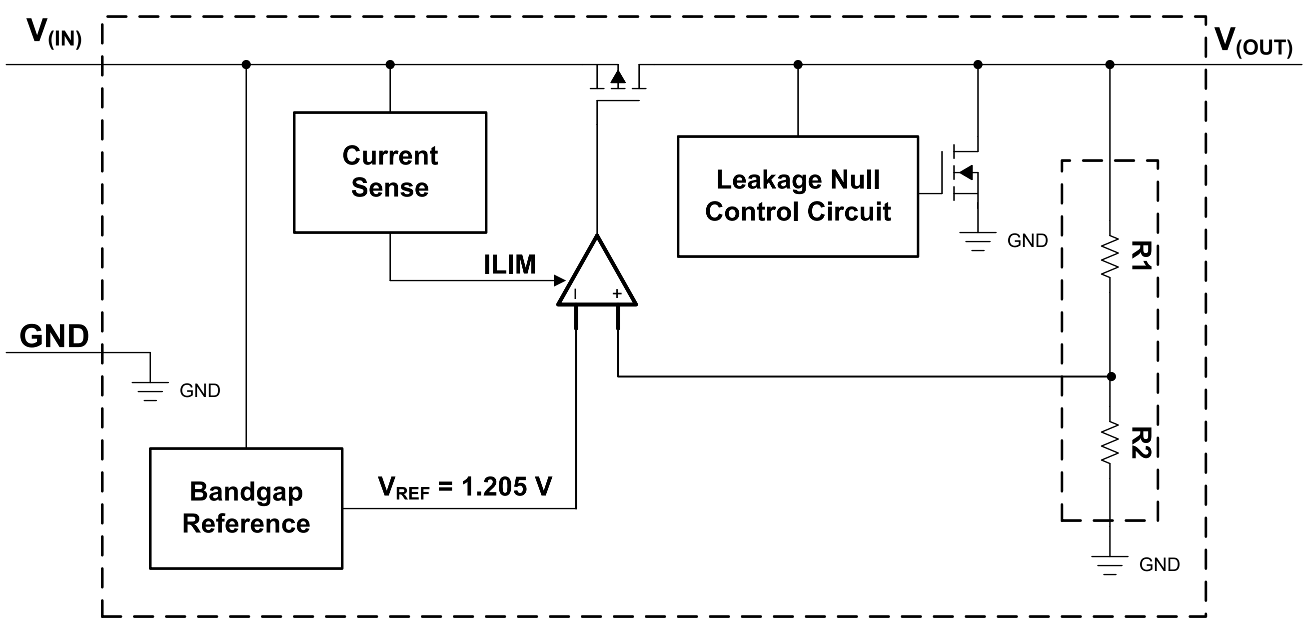


Figure 6-2. Functional Block Diagram: Fixed Version

6.3 Feature Description

6.3.1 Wide Supply Range

This device has an operational input supply range of 2.5V to 30V, allowing for a wide range of applications. This wide supply range is designed for applications that have either large transients or high DC voltage supplies.

6.3.2 Low Quiescent Current

This device only requires 3.2µA (typical) of quiescent current across the complete load current range (0mA to 150mA). This requirement is at room temperature and 4.8µA (max) across the temperature range of –40°C to +125°C.

6.3.3 Dropout Voltage (V_{DO})

Dropout voltage (V_{DO}) is defined as V_{IN} – V_{OUT} at the rated output current (I_{RATED}), where the pass transistor is fully on. V_{IN} is the input voltage, V_{OUT} is the output voltage, and I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. In dropout operation, the pass transistor is in the ohmic or triode region of operation, and acts as a switch. Dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage where the output voltage is expected to stay in regulation. If the input voltage falls to less than the value required to maintain output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source, on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. Use Equation 1 to calculate the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \tag{1}$$

6.3.4 Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a brick-wall scheme. In a high-load current fault, the brick-wall scheme limits the output current to the current limit (I_{CL}). I_{CL} is listed in the *Electrical Characteristics* table.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{CL}]. For more information on current limits, see the *Know Your Limits* application note.

Figure 6-3 shows a diagram of the current limit.

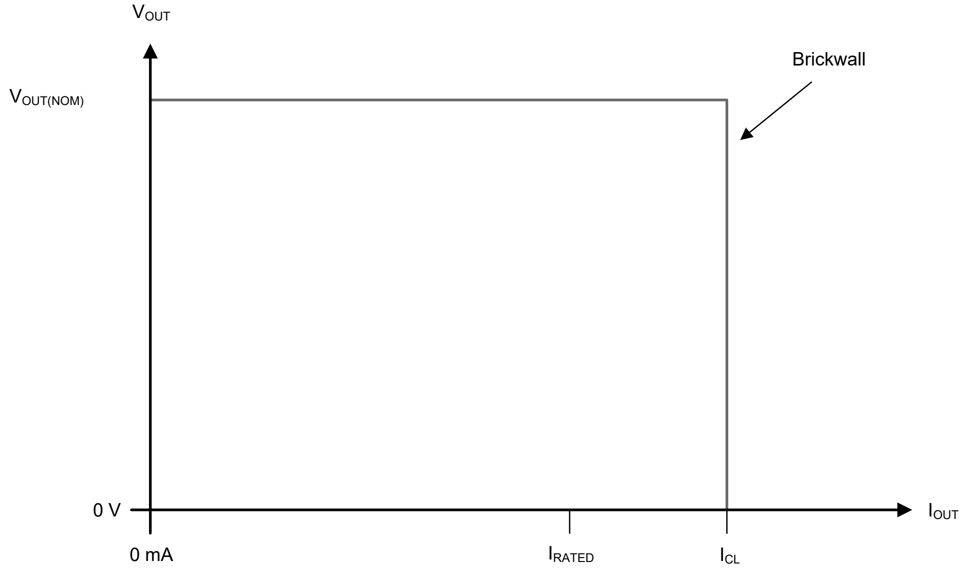


Figure 6-3. Current Limit

6.3.5 Leakage Null Control Circuit

This device has a built-in leakage-null control circuit. At high temperatures, pass-transistor leakage increases and starts impacting the V_{OUT} accuracy at no-load (I_{OUT} = 0mA) conditions. This leakage becomes more aggravated with higher headroom across the LDO (V_{IN} – V_{OUT}). The TLV709 has a built-in leakage-null control circuit that detects pass-transistor leakage and provides a ground discharge path for the leakage. This circuitry helps the TLV709 maintain much tighter V_{OUT} accuracy across wide V_{IN} and temperature (–40°C to +125°C) ranges.

6.4 Device Functional Modes

Table 6-1 provides a quick comparison between the normal and dropout modes of operation.

Table 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER	
	V_{IN}	I_{OUT}
Normal	$V_{IN} > V_{OUT(nom)} + V_{DO}$	$I_{OUT} < I_{CL}$
Dropout	$V_{IN} < V_{OUT(nom)} + V_{DO}$	$I_{OUT} < I_{CL}$

6.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is greater than –40°C and less than +125°C

6.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, the device operates in dropout mode. However, make sure all other conditions are met for normal operation. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded. The pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout result in large output voltage deviations.

When the device is in a steady dropout state, the pass transistor is driven into the ohmic or triode region. This state is defined as when the device is in dropout, directly after being in a normal regulation state, but *not* during start up. Dropout occurs when $V_{IN} < V_{OUT(NOM)} + V_{DO}$. When the input voltage returns to a value $\geq V_{OUT(NOM)} + V_{DO}$, the output voltage overshoots for a short period of time. $V_{OUT(NOM)}$ is the nominal output voltage and V_{DO} is the dropout voltage. During this time, the device pulls the pass transistor back into the linear region.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TLV709 LDO regulator is a good choice for battery-powered applications. This device is a good supply for low-power microcontrollers, such as the MSP430, because of the device low I_Q performance across load current range. The ultra-low-supply current of the TLV709 maximizes efficiency at light loads. The device provides high input voltage range and flexibility of output voltage selection in the adjustable configuration and fixed output levels. These features make the device optimal as a supply in building automation and power tools.

7.2 Typical Application

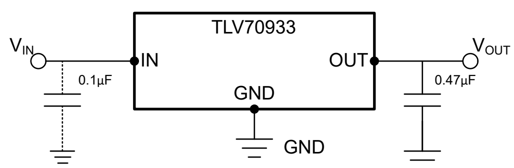


Figure 7-1. Typical Application Circuit (Fixed-Voltage Version)

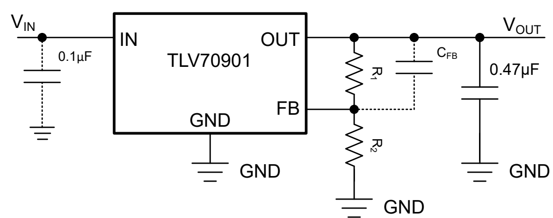


Figure 7-2. TLV70901 Adjustable LDO Regulator Programming

NOTE: Dotted lines indicate an optional input capacitor. See the *Recommended Operating Conditions* table and the *Input and Output Capacitor Requirements* section.

Table 7-1. Adjustable Output Voltage for Resistors R1 and R2

OUTPUT VOLTAGE (V)	R1 (MΩ)	R2 (MΩ)
1.8	0.499	1
2.8	1.33	1
5.0	3.16	1

7.2.1 Design Requirements

Table 7-2 summarizes the design requirements for Figure 7-1.

Table 7-2. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	12V
Output voltage	3.3V
Output current	100mA

7.2.2 Detailed Design Procedure

7.2.2.1 Setting V_{OUT} for the TLV70901 Adjustable LDO

As illustrated in Figure 7-2, the TLV709 contains an adjustable version (the TLV70901) that sets the output voltage using an external resistor divider. The output voltage operating range is 1.2V to 28V, and is calculated using:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right) \quad (2)$$

where:

- V_{REF} = 1.205V (typical)

Choose resistors R1 and R2 to allow approximately 1.5µA of current through the resistor divider. Lower value resistors provide improved noise performance, but consume more power. Avoid higher resistor values. Leakage current into or out of FB across R1 / R2 creates an offset voltage proportional to V_{OUT} divided by V_{REF}. The recommended design procedure is to choose R2 = 1MΩ to set the divider current at 1.5µA, and then calculate R1 using Equation 3:

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R2 \quad (3)$$

Figure 7-2 depicts this configuration.

7.2.2.2 External Capacitor Requirements

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but use good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature. However, using Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. Generally, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors listed in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

7.2.2.3 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. Use an input capacitor if the source impedance is more than 0.5Ω. Use a higher-value capacitor if large, fast rise-time load or line transients are anticipated. Additionally, use a higher-value capacitor if the device is located several inches from the input power source.

Dynamic device performance is improved by using a larger output capacitor. The TLV709 requires a 1µF or larger output capacitor (0.47µF or larger capacitance) for stability and an equivalent series resistance (ESR) between 0.001Ω and 1Ω. For best transient performance, use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and ESR over temperature. When choosing a capacitor for a specific application, be mindful of the DC bias characteristics for the capacitor. Higher output voltages cause a significant derating of the capacitor. Use an output capacitor within the range specified in the *Recommended Operating Conditions* table for stability.

7.2.2.4 Reverse Current

Excessive reverse current potentially damages this device. Reverse current flows through the intrinsic body diode of the PMOS pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current occurs are outlined in this section, all of which exceed the absolute maximum rating of $V_{OUT} \le V_{IN} + 0.3V$. These conditions are:

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, use external protection to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated. Limit reverse current to 5% or less of the rated output current of the device in the event this current cannot be avoided.

Figure 7-3 shows one approach for protecting the device.

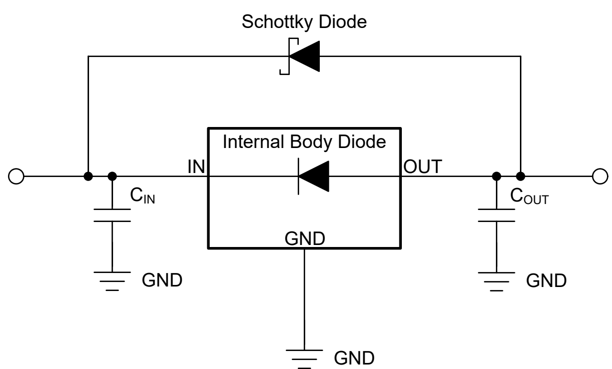


Figure 7-3. Example Circuit for Reverse Current Protection Using a Schottky Diode

7.2.2.5 Feed-Forward Capacitor (C_{FF})

For the adjustable-voltage version device, connect a feed-forward capacitor (C_{FF}) from the OUT pin to the FB pin. C_{FF} improves transient, noise, and PSRR performance, but is not required for regulator stability. Recommended C_{FF} values are listed in the *Recommended Operating Conditions* table. Using a higher capacitance C_{FF} causes the start-up time to increase. For a detailed description of C_{FF} tradeoffs, see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application note.

C_{FF} and R_1 form a zero in the loop gain at frequency f_Z. C_{FF}, R_1, and R_2 form a pole in the loop gain at frequency f_P. C_{FF} zero and pole frequencies are calculated from the following equations:

$$f_Z = 1 / (2 \times \pi \times C_{FF} \times R_1) \quad (4)$$

$$f_P = 1 / (2 \times \pi \times C_{FF} \times (R_1 \parallel R_2)) \quad (5)$$

$C_{FF} \ge 10pF$ is required for stability if the feedback divider current is less than 5μA. Equation 6 calculates the feedback divider current.

$$I_{FB\_Divider} = V_{OUT} / (R_1 + R_2) \quad (6)$$

To avoid start-up time increases from C_{FF}, limit the product $C_{FF} \times R_1 < 50\mu s$.

For an output voltage of 1.205V with the FB pin tied to the OUT pin, no C_{FF} is used.

7.2.2.6 Power Dissipation (P_D)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct thermal plane sizing. Make sure the PCB area around the regulator has few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation (P_D).

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \tag{7}$$

Note

Power dissipation is minimized, and therefore greater efficiency achieved, by correct selection of the system voltage rails. For the lowest power dissipation, use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. Make sure this pad area contains an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. According to the following equation, power dissipation and junction temperature are most often related by several factors. These factors are the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \tag{8}$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design. Therefore, $R_{\theta JA}$ varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area. This thermal resistance is used as a relative measure of package thermal performance. $R_{\theta JA}$ is improved by 35% to 55% compared to the *Thermal Information* table value with the PCB board layout optimization. See the *An empirical analysis of the impact of board layout on LDO thermal performance* application note for further details.

7.2.2.7 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics. These metrics estimate the junction temperatures of the linear regulator when in-circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The *Thermal Information* table lists the primary thermal metrics, which are the junction-to-top characterization parameter (ψ_{JT}) and junction-to-board characterization parameter (ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J), as described in the following equations. Use the junction-to-top characterization parameter (ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. Use the junction-to-board characterization parameter (ψ_{JB}) with the PCB surface temperature 1mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + \psi_{JT} \times P_D \tag{9}$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

$$T_J = T_B + \psi_{JB} \times P_D \quad (10)$$

where:

- T_B is the PCB surface temperature measured 1mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see the *Semiconductor and IC Package Thermal Metrics* application note.

7.3 Best Design Practices

Place at least one 0.47µF capacitor as close as possible to the OUT and GND pins of the regulator.

Do not connect the output capacitor to the regulator using a long, thin trace.

Connect an input capacitor as close as possible to the IN and GND pins of the regulator for best performance.

Do not exceed the absolute maximum ratings.

7.4 Power Supply Recommendations

The TLV709 is designed to operate from an input voltage supply range between 2.5V and 30V. The input voltage range provides adequate headroom for the device to have a regulated output. If the input supply is noisy, additional input capacitors with low ESR help improve the output noise performance.

7.5 Layout

7.5.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the printed circuit board (PCB). Make sure these components are placed as near as practical to the respective LDO pin connections. Place ground return connections for the input and output capacitors as close to the GND pin as possible, using wide, component-side, copper planes. Do not use vias and long traces to create LDO circuit connections to the input capacitor, output capacitor, or the resistor divider. This practice negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load current transients, minimizes noise, and increases circuit stability. Use a ground reference plane either embedded in the PCB or located on the bottom side of the PCB opposite the components. This reference plane provides accuracy of the output voltage and shields the LDO from noise.

7.5.1.1 Power Dissipation

To provide reliable operation, make sure worst-case junction temperature does not exceed 125°C. This restriction limits the power dissipation the regulator handles in any given application. To make sure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D. Make sure P_D is less than or equal to $P_{D(max)}$.

Equation 11 determines the maximum-power-dissipation limit:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}} \quad (11)$$

where:

- $T_J$max is the maximum allowable junction temperature
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package (see the *Thermal Information*table)
- T_A is the ambient temperature

Equation 12 calculates the regulator dissipation:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (12)$$

7.5.2 Layout Examples

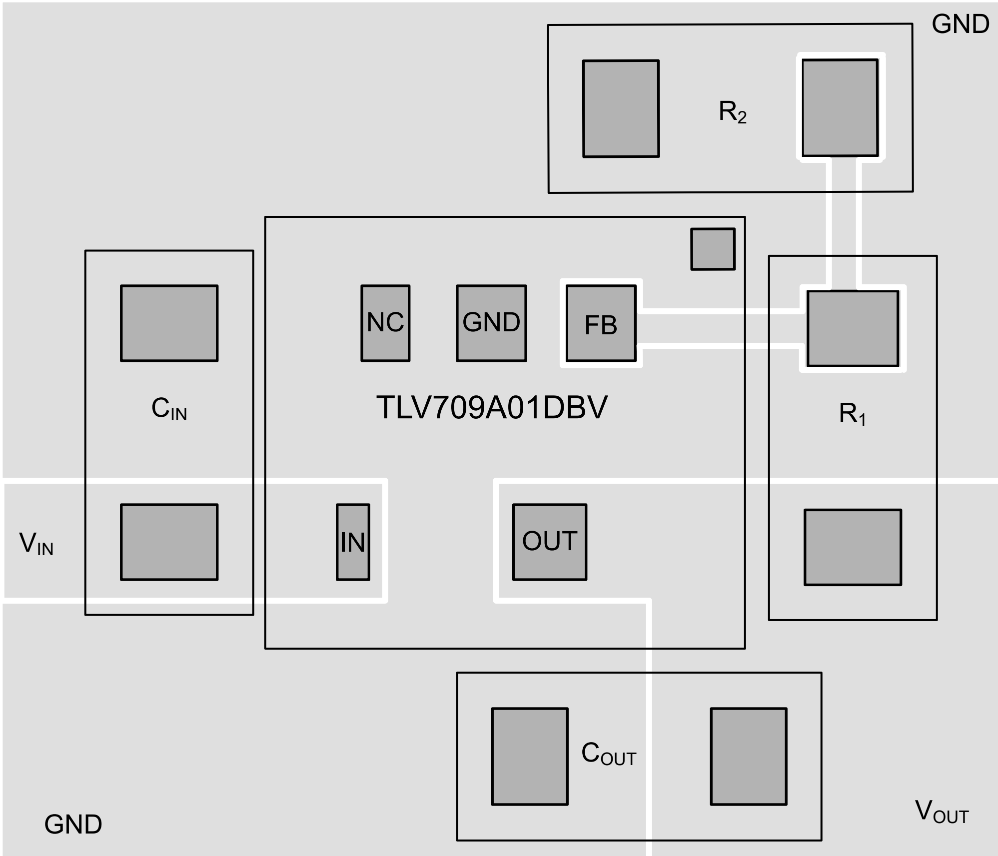


Figure 7-4. Example Layout for the TLV709A01DBV

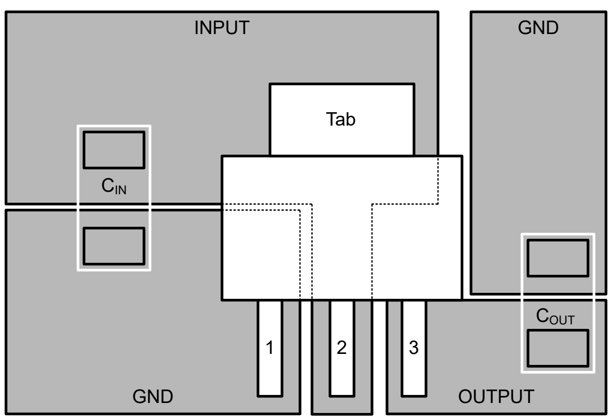


Figure 7-5. Example Layout for the TLV709xxPK (IN Tab)

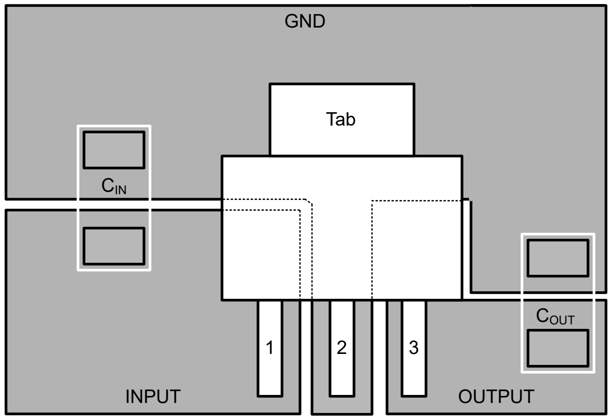


Figure 7-6. Example Layout for the TLV709AxxPK (GND Tab)

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 Evaluation Module

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TLV709. Request the TPS71533EVM evaluation module (and related user's guide) at the TI website through the product folders or purchased directly from the TI eStore.

8.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TLV709 is available through the product folders under *Tools & Software*.

8.1.2 Device Nomenclature

Table 8-1. Device Nomenclature[(1)]

PRODUCT	V_{OUT}
TLV709A**xx**DBV**z**	In the SOT-23 (DBV) package: **XX** is the nominal output voltage (for example, 33 = 3.3V, 50 = 50V, 01 = Adjustable). **Z** is the package quantity.
TLV709**xx**PK**z**	In the SOT-89 (PK) package with an IN tab: **XX** is the nominal output voltage (for example, 33 = 3.3V, 50 = 50V). **Z** is the package quantity.
TLV709A**xx**PK**z**	In the SOT-89 (PK) package with a GND tab: **XX** is the nominal output voltage (for example, 33 = 3.3V, 50 = 50V). **Z** is the package quantity.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPS71533EVM LDO Regulator Evaluation Module* user guide

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (January 2024) to Revision E (April 2024) **Page**

- Corrected minimum spec limits to 1.152V for Internal reference....................6

Changes from Revision C (November 2023) to Revision D (January 2024) **Page**

- Updated ground pin current parameter for non-A version devices....................6

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTLV709A33DBVR	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		Samples
TLV70933PKR	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	NS	Samples
TLV70950PKR	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	NV	Samples
TLV709A01DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2V8F	Samples
TLV709A33DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2V6F	Samples
TLV709A33PKR	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	NT	Samples
TLV709A50DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2V7F	Samples
TLV709A50PKR	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	NW	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

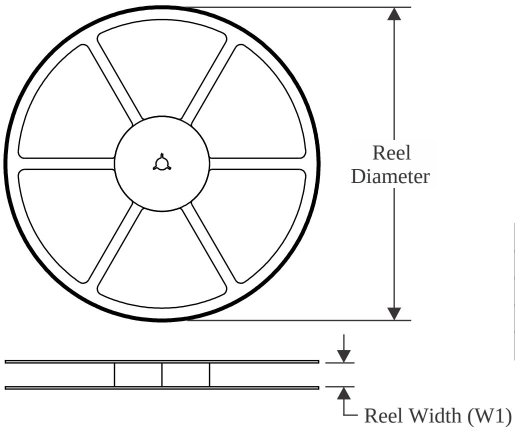
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

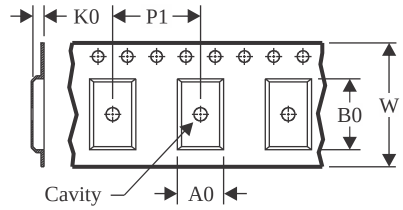
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

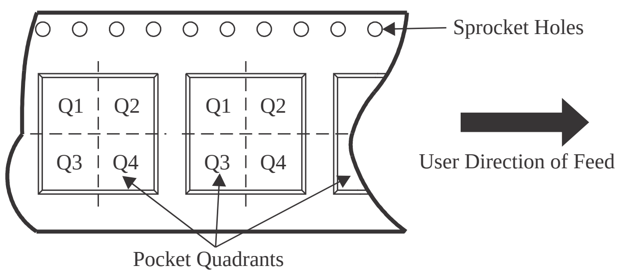


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

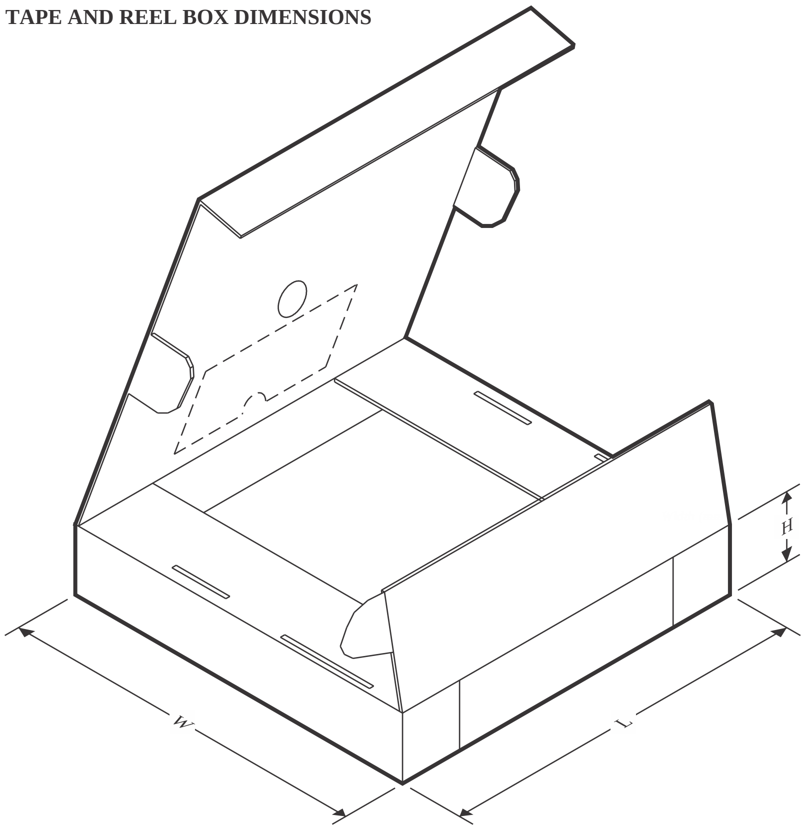
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV70933PKR	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
TLV70950PKR	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
TLV709A01DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV709A33DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV709A33PKR	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
TLV709A50DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV709A50PKR	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3

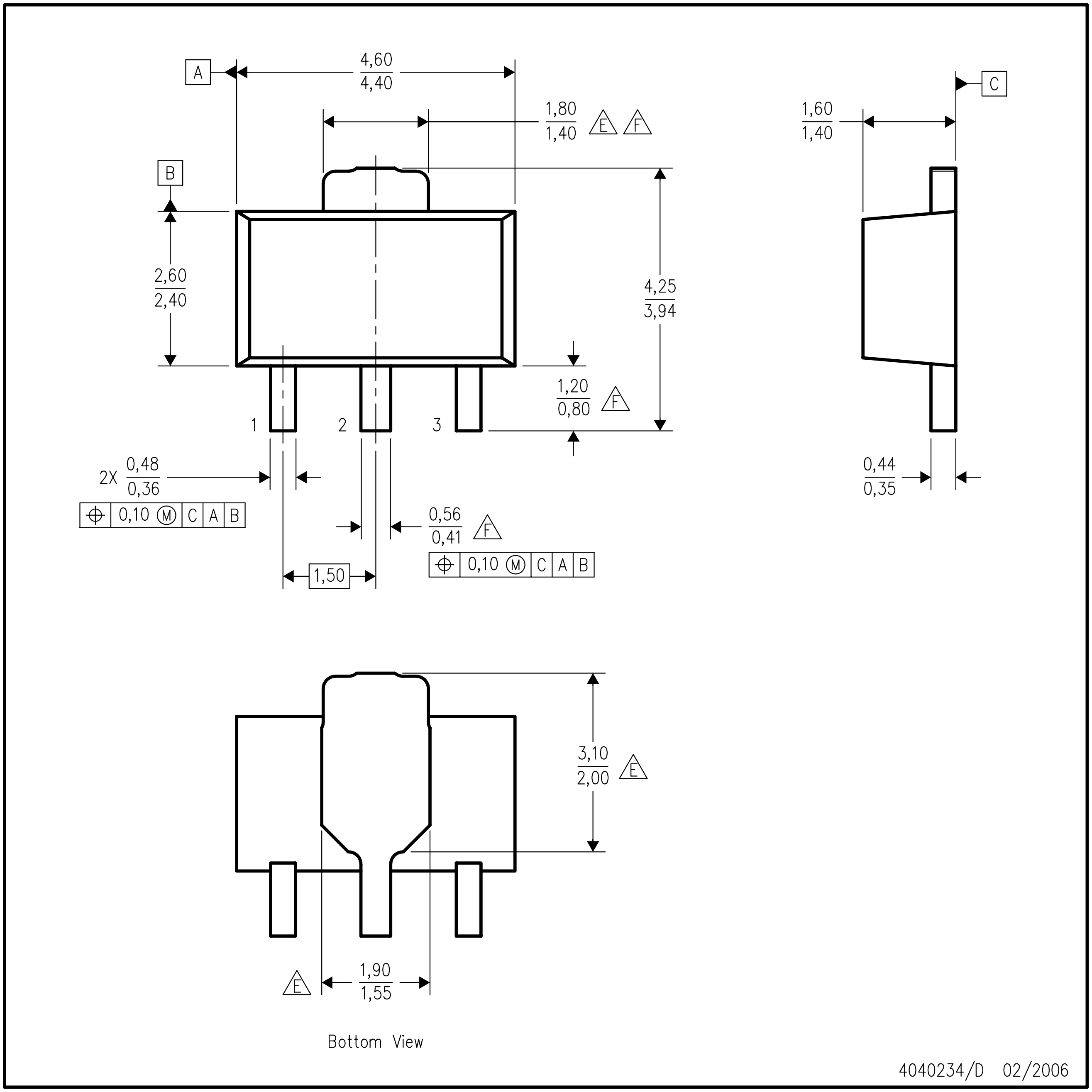
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

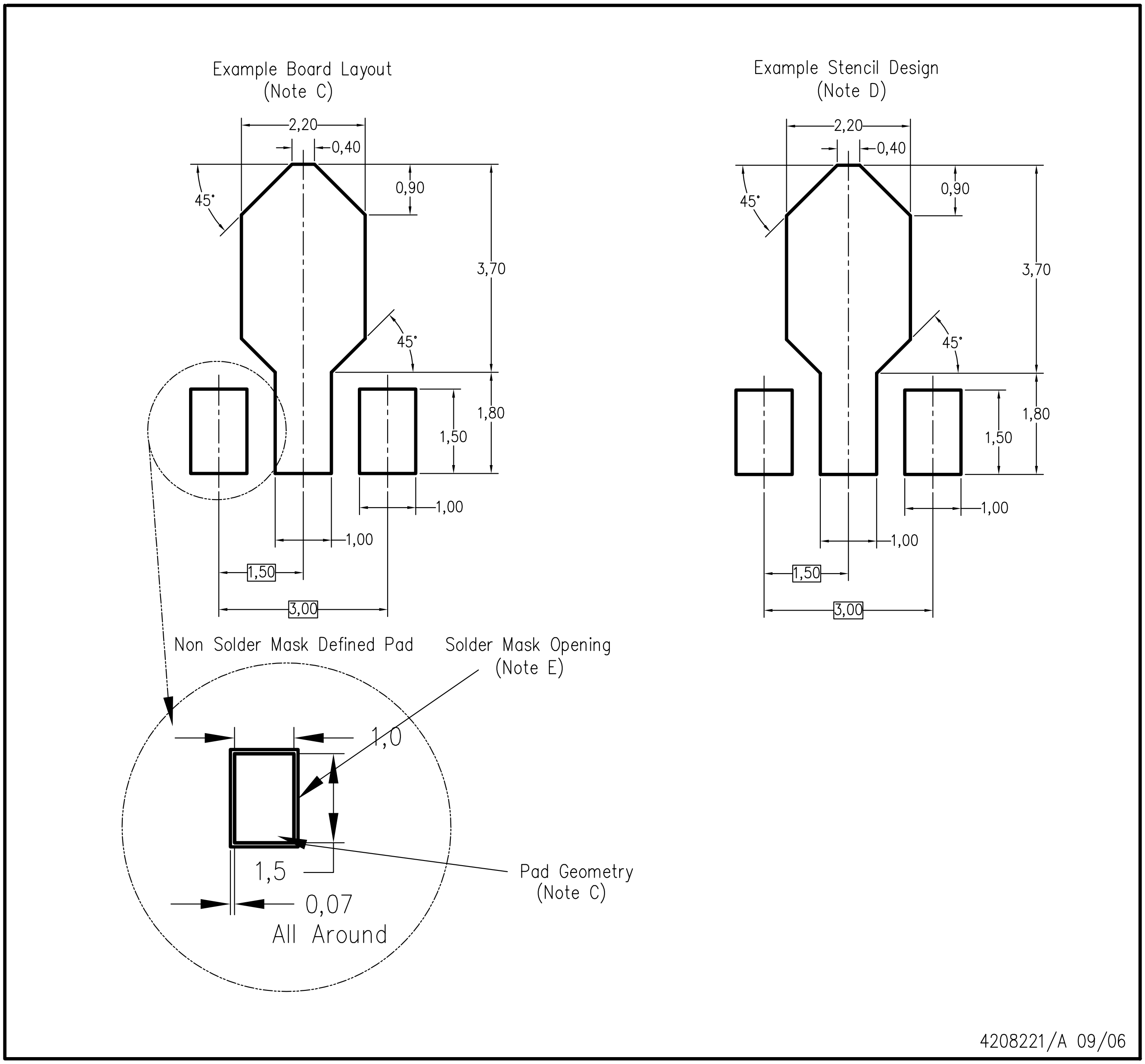
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV70933PKR	SOT-89	PK	3	1000	190.0	190.0	30.0
TLV70950PKR	SOT-89	PK	3	1000	190.0	190.0	30.0
TLV709A01DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV709A33DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV709A33PKR	SOT-89	PK	3	1000	190.0	190.0	30.0
TLV709A50DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV709A50PKR	SOT-89	PK	3	1000	190.0	190.0	30.0

PK (R–PSSO–F3) PLASTIC SINGLE–IN–LINE PACKAGE

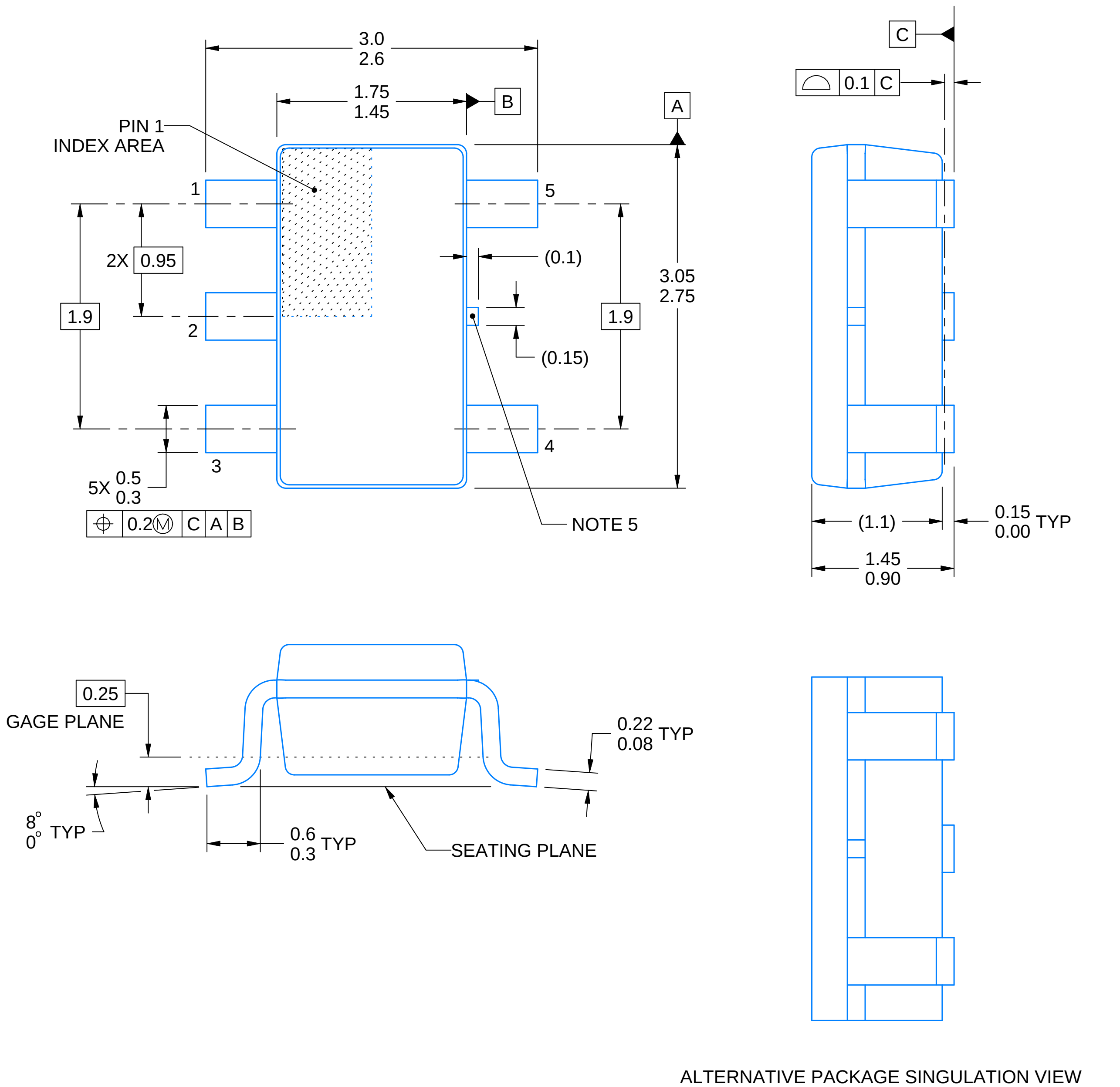


NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the tab.
D. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion not to exceed 0.15 per side.
E. Thermal pad contour optional within these dimensions.
F. Falls within JEDEC TO–243 variation AA, except minimum lead length, pin 2 minimum lead width, minimum tab width.

PK (R–PDSO–G3)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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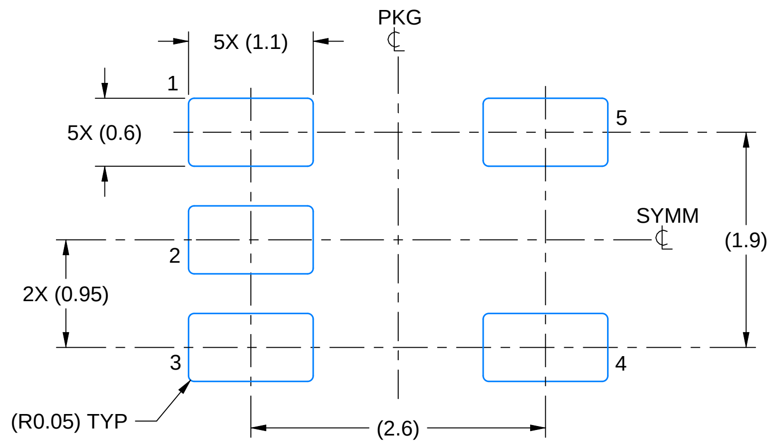
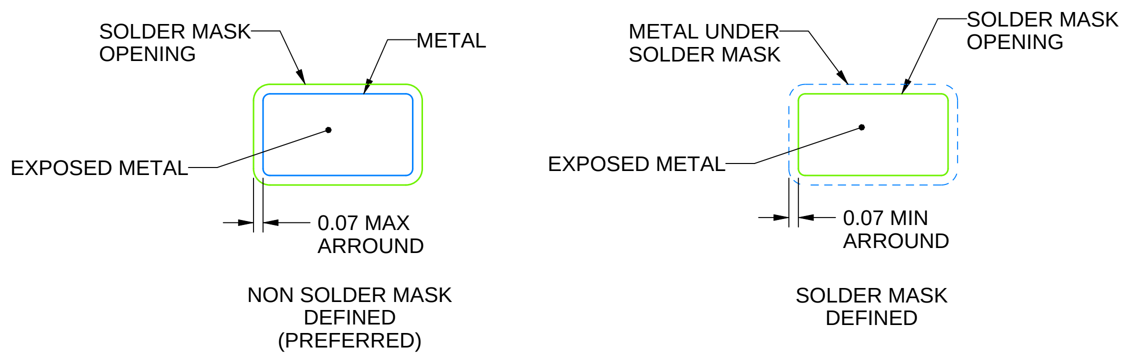
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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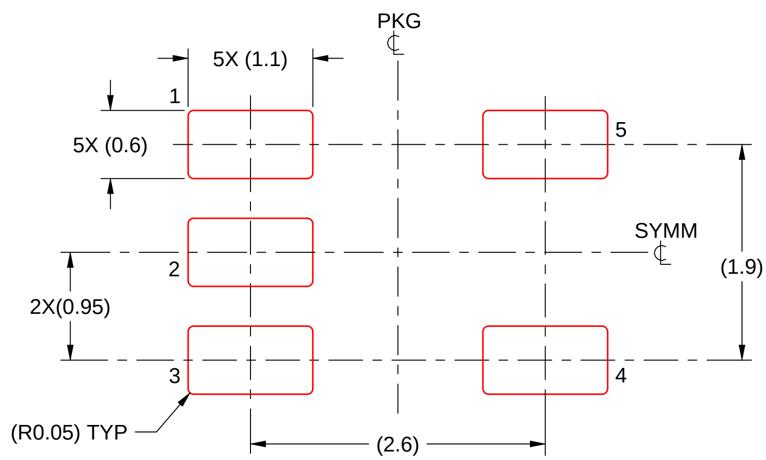
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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