1 Features
Qualified for automotive applications:
- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to +125°C ambient operating temperature
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C7B

Designed for high performance:
- Nano supply current : 120 nA (Typ)
- High accuracy: ±0.5% (Typ)
- Built-in hysteresis (V_HYS): 5% (Typ)
- Fixed threshold voltage (V_IT): 0.8 V to 5.4 V

Designed for a wide range of applications:
- Operating voltage range : 0.7 V to 6 V
- Fixed (V_IT) voltage: 0.8 V to 5.4 V in 0.1 V steps
- Programmable reset time delay (t_D)
  - Min time delay: 40 µs (typ) without capacitor
  - Active-low manual reset (MR)

Multiple output topologies / Package type:
- Four output topologies (RESET / RESET):
  - TLV840MADL-Q1: open-drain, active-low
  - TLV840MAPL-Q1: push-pull, active-low
  - TLV840MADH-Q1: open-drain, active-high
  - TLV840MAPH-Q1: push-pull, active-high
- Package: SOT23-5 (DBV)

2 Applications
- Surround view system, front camera
- Automotive gateway
- Radar ECU
- Automotive head unit
- ADAS controller
- Emergency call
- Telematics control unit

3 Description
The TLV840-Q1 device is a voltage supervisor or reset IC that can operate at wide input voltage levels from 0.7 V to 6 V while maintaining very low quiescent current across the whole VDD and temperature range. TLV840-Q1 offers the best combination of low power consumption, high accuracy and low propagation delay (t_{pHL} = 30 µs typical).

Reset output signal is asserted when the voltage at VDD drops below the negative voltage threshold (V_{IT}). Reset signal is cleared when VDD rise above V_{IT} plus hysteresis (V_{HYS}) and the reset time delay (t_D) expires. Reset time delay can be programmed by connecting a capacitor between the CT pin and ground. For a minimum reset delay time the CT pin can be left floating. The TLV840-Q1, with its manual reset pin (MR), offers program flexibility by forcing the system into a hard reset when the pin is asserted.

Additional features: Low power-on reset voltage (V_{POR}), built-in glitch immunity protection for VDD, built-in hysteresis, low open-drain output leakage current (I_{LKG(OD)}). TLV840-Q1 is a perfect voltage monitoring solution for automotive applications and battery-powered / low-power applications.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE (1)</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLV840-Q1</td>
<td>SOT-23 (5) (DBV)</td>
<td>2.90 mm × 1.60 mm</td>
</tr>
</tbody>
</table>

(1) For package details, see the mechanical drawing addendum at the end of the data sheet.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.
# Table of Contents

1 Features ............................................................................ 1
2 Applications ....................................................................... 1
3 Description ......................................................................... 1
4 Revision History .................................................................. 2
5 Device Comparison .............................................................. 3
6 Pin Configuration and Functions ........................................... 4
7 Specifications ....................................................................... 5
7.1 Absolute Maximum Ratings ............................................. 5
7.2 ESD Ratings ..................................................................... 5
7.3 Recommended Operating Conditions .................................. 5
7.4 Thermal Information ......................................................... 5
7.5 Electrical Characteristics ................................................. 6
7.6 Timing Requirements ....................................................... 7
7.7 Timing Diagrams .............................................................. 8
7.8 Typical Characteristics ..................................................... 10
8 Detailed Description .......................................................... 12
8.1 Overview ........................................................................ 12
8.2 Functional Block Diagram .............................................. 12
8.3 Feature Description .......................................................... 12
8.4 Device Functional Modes ................................................ 17
9 Application and Implementation .......................................... 18
9.1 Application Information .................................................... 18
9.2 Typical Application .......................................................... 18
10 Power Supply Recommendations ....................................... 21
11 Layout .............................................................................. 22
12 Device and Documentation Support ..................................... 23
12.1 Device Nomenclature ....................................................... 23
12.2 Receiving Notification of Documentation Updates .......... 24
12.3 Support Resources .......................................................... 24
12.4 Trademarks ..................................................................... 24
13 Mechanical, Packaging, and Orderable Information .......... 24

# 4 Revision History

Changes from Revision * (November 2020) to Revision A (April 2021)

- RTM release ........................................................................ 1
5 Device Comparison

*Figure 5-1* shows the device naming nomenclature to compare the different device variants. See Section 12.1 for a more detailed explanation.

**Figure 5-1. Device Naming Nomenclature**
6 Pin Configuration and Functions

![Pin Configuration and Functions](image)

**Figure 6-1. Pin Configuration TLV840M-Q1
DBV Package 5-Pin SOT-23
TLV840M-Q1 Top View**

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIN NO.</td>
<td>TLV840MAxL-Q1</td>
<td>TLV840MAxH-Q1</td>
</tr>
<tr>
<td>1</td>
<td>RESET</td>
<td>N/A</td>
</tr>
<tr>
<td>2</td>
<td>VDD</td>
<td>VDD</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
<td>GND</td>
</tr>
<tr>
<td>4</td>
<td>MR</td>
<td>MR</td>
</tr>
<tr>
<td>5</td>
<td>CT</td>
<td>CT</td>
</tr>
</tbody>
</table>

**Table 6-1. Pin Functions**

**Active-Low Output Reset Signal:** This pin is driven logic low when VDD voltage falls below the negative voltage threshold ($V_{IT-}$). RESET remains low (asserted) for the delay time period ($t_D$) after VDD voltage rises above $V_{IT+} = V_{IT-} + V_{HYS}$.

**Active-High Output Reset Signal:** This pin is driven logic high when VDD voltage falls below the negative voltage threshold ($V_{IT-}$). RESET remains high (asserted) for the delay time period ($t_D$) after VDD voltage rises above $V_{IT+} = V_{IT-} + V_{HYS}$.

**Input Supply Voltage:** TLV840-Q1 monitors VDD voltage.

**Manual Reset:** Pull this pin to a logic low to assert a reset signal in the RESET output pin. After PIN pin is left floating or pulls to logic high, the RESET output deasserts to the nominal state after the reset delay time ($t_D$) expires.

**Capacitor Time Delay Pin:** The CT pin offers a user-programmable delay time. Connect an external capacitor on this pin to adjust time delay. When not in use leave pin floating for the smallest fixed time delay.
7 Specifications

7.1 Absolute Maximum Ratings
over operating free-air temperature range, unless otherwise noted

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage VDD</td>
<td>–0.3</td>
<td>6.5</td>
<td>V</td>
</tr>
<tr>
<td>Voltage CT, MR (2), RESET (TLV840MAPL), RESET (TLV840MAPH)</td>
<td>–0.3 $V_{DD} + 0.3$ (3)</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>RESET (TLV840MADL)</td>
<td>–0.3</td>
<td>6.5</td>
<td>V</td>
</tr>
<tr>
<td>Current RESET, RESET pin</td>
<td>–20</td>
<td>20</td>
<td>mA</td>
</tr>
<tr>
<td>Temperature (4) Operating ambient temperature, $T_A$</td>
<td>–40</td>
<td>125</td>
<td>°C</td>
</tr>
<tr>
<td>Temperature (4) Storage, $T_{STG}$</td>
<td>–65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

1) Stresses beyond those listed under Absolute Maximum Rating may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Condition. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2) If the logic signal driving MR is less than VDD, then $I_{DD}$ current increases based on voltage differential.

3) The absolute maximum rating is $(V_{DD} + 0.3)$ V or 6.5 V, whichever is smaller

4) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.

7.2 ESD Ratings

<table>
<thead>
<tr>
<th>$V_{(ESD)}$</th>
<th>Electrostatic discharge</th>
<th>Human body model (HBM), per AEC Q100-002(1)</th>
<th>Charged device model (CDM), per AEC Q100-011</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>±2000</td>
<td>±750</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions
over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage VDD (TLV840MAxL)</td>
<td>0.7</td>
<td>6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>CT, RESET (TLV840MAxL), RESET (TLV840MAPH) , MR</td>
<td>0</td>
<td>6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Current RESET and RESET pin current</td>
<td>–5</td>
<td>5</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$T_A$ Operating ambient temperature</td>
<td>–40</td>
<td>125</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

7.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>TLV840-Q1 DBV (SOT23-5)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{JUA}$ Junction-to-ambient thermal resistance</td>
<td>193.5</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{JUC(top)}$ Junction-to-case (top) thermal resistance</td>
<td>117.9</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{JB}$ Junction-to-board thermal resistance</td>
<td>98.5</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\psi_{JT}$ Junction-to-top characterization parameter</td>
<td>43.4</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\psi_{JB}$ Junction-to-board characterization parameter</td>
<td>97.8</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{JUC(bottom)}$ Junction-to-case (bottom) thermal resistance</td>
<td>N/A</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
7.5 Electrical Characteristics

At $0.7 \, \text{V} \leq V_{\text{DD}} \leq 6 \, \text{V}$, $\text{CT} = \text{MR} = \text{Open}$, $\text{RESET}$ pull-up resistor ($R_{\text{pull-up}}$) = 100 kΩ to $V_{\text{DD}}$, output reset load ($C_{\text{LOAD}}$) = 10 pF and over operating free-air temperature range $-40^\circ\text{C}$ to $125^\circ\text{C}$, unless otherwise noted. $V_{\text{DD}}$ ramp rate $\leq 100 \, \text{mV/\mu s}$. Typical values are at $T_A = 25^\circ\text{C}$.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>COMMON PARAMETERS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{\text{DD}}$</td>
<td>Input supply voltage</td>
<td>TLV840MAXL</td>
<td>0.7</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>$V_{\text{IT}-}$</td>
<td>Negative-going input threshold accuracy</td>
<td>$V_{\text{IT}} = 0.8 , \text{V}$ to $1.7 , \text{V}$</td>
<td>$-2.5 \pm 0.5 , %$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{\text{IT}} = 1.8 , \text{V}$ to $5.4 , \text{V}$</td>
<td>$-2 \pm 0.5 , %$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{\text{HYS}}$</td>
<td>Hysteresis on $V_{\text{IT-}}$ pin</td>
<td></td>
<td>2.5</td>
<td>5</td>
<td>7</td>
</tr>
<tr>
<td>$I_{\text{DD}}$</td>
<td>Supply current into $V_{\text{DD}}$ pin</td>
<td>$V_{\text{DD}} = 2 , \text{V}$; $V_{\text{IT-}} = 0.8 , \text{V}$ to $1.8 , \text{V}$</td>
<td>0.12</td>
<td>1.0</td>
<td>\mu A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{\text{DD}} = 6 , \text{V}$; $V_{\text{IT-}} = 0.8 , \text{V}$ to $5.4 , \text{V}$</td>
<td>0.15</td>
<td>1.2</td>
<td>\mu A</td>
</tr>
<tr>
<td>$V_{\text{MR-L}}$</td>
<td>Manual reset logic low input</td>
<td></td>
<td></td>
<td>0.3$V_{\text{DD}}$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{\text{MR-H}}$</td>
<td>Manual reset logic high input</td>
<td></td>
<td></td>
<td>$0.7V_{\text{DD}}$</td>
<td>V</td>
</tr>
<tr>
<td>$R_{\text{CT}}$</td>
<td>Manual reset internal pull-up resistance</td>
<td></td>
<td>100</td>
<td></td>
<td>kΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>500</td>
<td></td>
<td>kΩ</td>
</tr>
</tbody>
</table>

TLV840MADL (Open-drain active-low)

| $V_{\text{POR}}$ | Power on Reset Voltage | $V_{\text{OL(max)}} = 300 \, \text{mV}$ | 700 | mV |
| | | $I_{\text{OUT(Sink)}} = 15 \, \mu \text{A}$ | | |
| $V_{\text{OL}}$ | Low level output voltage | $V_{\text{DD}} = 0.7 \, \text{V}$; $0.8 \, \text{V} \leq V_{\text{IT-}} \leq 1.5 \, \text{V}$ | $I_{\text{OUT(Sink)}} = 15 \, \mu \text{A}$ | 300 | mV |
| | | $V_{\text{DD}} = 1.5 \, \text{V}$; $1.6 \, \text{V} \leq V_{\text{IT-}} \leq 3.3 \, \text{V}$ | $I_{\text{OUT(Sink)}} = 500 \, \mu \text{A}$ | 300 | mV |
| | | $V_{\text{DD}} = 3.3 \, \text{V}$; $3.4 \, \text{V} \leq V_{\text{IT-}} \leq 5.5 \, \text{V}$ | $I_{\text{OUT(Sink)}} = 2 \, \text{mA}$ | 300 | |
| $I_{\text{ILK(OD)}}$ | Open-Drain output leakage current | $V_{\text{DD}} = V_{\text{PULLUP}} = 6 \, \text{V}$ | $T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$ | 10 | 100 | nA |

TLV840MAPL (Push-pull active-low)

| $V_{\text{POR}}$ | Power on Reset Voltage | $V_{\text{OL(max)}} = 300 \, \text{mV}$ | 700 | mV |
| | | $I_{\text{OUT(Sink)}} = 15 \, \mu \text{A}$ | | |
| $V_{\text{OL}}$ | Low level output voltage | $V_{\text{DD}} = 0.7 \, \text{V}$; $0.8 \, \text{V} \leq V_{\text{IT-}} \leq 1.5 \, \text{V}$ | $I_{\text{OUT(Sink)}} = 15 \, \mu \text{A}$ | 300 | mV |
| | | $V_{\text{DD}} = 1.5 \, \text{V}$; $1.6 \, \text{V} \leq V_{\text{IT-}} \leq 3.3 \, \text{V}$ | $I_{\text{OUT(Sink)}} = 500 \, \mu \text{A}$ | 300 | mV |
| | | $V_{\text{DD}} = 3.3 \, \text{V}$; $3.4 \, \text{V} \leq V_{\text{IT-}} \leq 5.5 \, \text{V}$ | $I_{\text{OUT(Sink)}} = 2 \, \text{mA}$ | 300 | |
| $V_{\text{OH}}$ | High level output voltage | $V_{\text{DD}} = 1.8 \, \text{V}$; $0.8 \, \text{V} \leq V_{\text{IT-}} \leq 1.4 \, \text{V}$ | $I_{\text{OUT(Source)}} = 500 \, \mu \text{A}$ | 0.8$V_{\text{DD}}$ | V |
| | | $V_{\text{DD}} = 3.3 \, \text{V}$; $1.5 \, \text{V} \leq V_{\text{IT-}} \leq 3.0 \, \text{V}$ | $I_{\text{OUT(Source)}} = 500 \, \mu \text{A}$ | 0.8$V_{\text{DD}}$ | |
| | | $V_{\text{DD}} = 6 \, \text{V}$; $3.1 \, \text{V} \leq V_{\text{IT-}} \leq 5.5 \, \text{V}$ | $I_{\text{OUT(Source)}} = 2 \, \text{mA}$ | 0.8$V_{\text{DD}}$ | |
7.5 Electrical Characteristics (continued)
At 0.7 V ≤ V_{DD} ≤ 6 V, CT = MR = Open, RESET pull-up resistor (R_{pull-up}) = 100 kΩ to VDD, output reset load (C_{LOAD}) = 10 pF and over operating free-air temperature range –40°C to 125°C, unless otherwise noted. VDD ramp rate ≤ 100 mV/µs. Typical values are at T_A = 25°C.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
</table>
| V_{POR} (Power on Reset Voltage) | V_{OH(min)} = 0.8V_{DD} V  
I_{OUT (Source)} = 15 µA | 900  | mV   |      |      |
|                             | VDD=3.3 V  
0.8 V ≤ V_{IT} ≤ 3.0 V  
I_{OUT(Sink)} = 500 µA | 300  | mV   |      |      |
|                             | VDD=6 V  
3.1 V ≤ V_{IT} ≤ 5.5 V  
I_{OUT(Sink)} = 2 mA | 300  | mV   |      |      |
| V_{OL} (Low level output voltage) | VDD=3.3 V  
0.8 V ≤ V_{IT} ≤ 1.5 V  
I_{OUT(Sink)} = 15 µA | 0.8V_{DD} | V   |      |      |
|                             | VDD=1.5 V  
1.6 V ≤ V_{IT} ≤ 3.3 V  
I_{OUT(Sink)} = 500 µA | 0.8V_{DD} | V   |      |      |
|                             | VDD=3.3 V  
3.4 V ≤ V_{IT} ≤ 5.5 V  
I_{OUT(Sink)} = 2 mA | 0.8V_{DD} | V   |      |      |

(1) V_{IT–} threshold voltage range from 0.8 V to 5.4 V (for DL, PL versions) in 100 mV steps
(2) If the logic signal driving MR is less than VDD, then I_{DD} current increases based on voltage differential
(3) V_{POR} is the minimum V_{DD} voltage level for a controlled output state

7.6 Timing Requirements
At 0.7 V ≤ V_{DD} ≤ 6 V, CT = MR = Open, RESET pull-up resistor (R_{pull-up}) = 100 kΩ to VDD, output reset load (C_{LOAD}) = 10 pF and over operating free-air temperature range –40°C to 125°C, unless otherwise noted. VDD ramp rate ≤ 100 mV/µs. Typical values are at T_A = 25°C.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_{P_HL} (Propagation detect delay for VDD falling below V_{IT–})</td>
<td>VDD : (V_{IT–} + 10%) to (V_{IT–} – 10%)</td>
<td>30</td>
<td>µs</td>
<td>50</td>
<td>µs</td>
</tr>
</tbody>
</table>
| t_{D} (Reset time delay)   | CT pin = Open or NC  
(V_{IT–} - 10%) to (V_{IT+} + 10%) | 40   | µs   | 80   | µs   |
|                            | CT pin = 10 nF | 6.2  | ms   |      |      |
|                            | CT pin = 1 µF | 619  | ms   |      |      |
| I_{GL_VIT–} (Glitch immunity V_{IT–}) | 5% V_{IT–} overdrive(2) | 10   | µs   |      |      |
| I_{STRT} (Startup Delay)   | CT pin = Open or NC | 300  | µs   |      |      |
| t_{MR_PW} (MR pin pulse duration to assert reset)   | V_{DD} = 3.3 V  
MR = V_{MR-L} to V_{MR-H} | 500  | ns   |      |      |
| t_{MR_RES} (Propagation delay from MR low to reset assertion) | V_{DD} = 3.3 V  
MR = V_{MR-H} to V_{MR-L} | 1    | µs   |      |      |
| t_{MR_ID} (Delay from MR release to reset deassertion) | V_{DD} = 3.3 V  
MR = V_{MR-L} to V_{MR-H} | t_{D} | ms   |      |      |

(1) t_{P_HL} measured from threshold trip point (V_{IT–}) to RESET assert. V_{IT+} = V_{IT–} + V_{HYS}
(2) Overdrive % = [(V_{DD}/ V_{IT–}) – 1] × 100%
(3) When VDD starts from less than the specified minimum V_{DD} and then exceeds V_{IT–}, reset is release after the startup delay (t_{STRT}), a capacitor at CT pin will add t_{D} delay to t_{STRT} time
(4) Refer section on Manual Reset Input for min pulse width needed on MR pin
7.7 Timing Diagrams

(1) \( t_D \) (no cap) is included in \( t_{STRT} \) time delay. If \( t_D \) delay is programmed by an external capacitor connected to CT pin then \( t_D \) programmed time will be added to the startup time, VDD slew rate = 100 mV / \( \mu \)s.

(2) Open-Drain timing diagram where RESET is pulled up to VDD via an external pull-up resistor.

(3) RESET output is undefined when \( V_{DD} \) is < \( V_{POR} \).

(4) \( t_D \) (no cap) is included in \( t_{STRT} \) time delay. If \( t_D \) delay is programmed by an external capacitor connected to CT pin then \( t_D \) programmed time will be added to the startup time, VDD slew rate = 100 mV / \( \mu \)s.

(5) RESET output is undefined when \( V_{DD} \) is < \( V_{POR} \) and limited to \( V_{OL} \) for \( V_{DD} \) slew rate = 100 mV / \( \mu \)S.

Figure 7-1. Timing Diagram TLV840MADL-Q1 (Open-Drain Active-Low)

Figure 7-2. Timing Diagram TLV840MAPL-Q1 (Push-Pull Active-Low)
Figure 7-3. Timing Diagram TLV840MAPH-Q1 (Push-Pull Active-High)

(6) \( t_D \) (no cap) is included in \( t_{\text{STR}} \) time delay. If \( t_D \) delay is programmed by an external capacitor connected to CT pin then \( t_D \) programmed time will be added to the startup time, VDD slew rate = 100 mV / \( \mu \)s.
7.8 Typical Characteristics

Typical characteristics show the typical performance of the TLV840-Q1 device. Test conditions are \( T_A = 25^\circ C \), \( VDD = 3.3 \) V, \( R_{\text{Pull-Up}} = 100 \) k\( \Omega \), \( C_{\text{LOAD}} = 50 \) pF, unless otherwise noted.

**Figure 7-4. Supply Current vs Supply Voltage**

**Figure 7-5. \( V_{IT} \), Accuracy vs Temperature**

**Figure 7-6. \( V_{\text{HYS}} \) vs Temperature**

**Figure 7-7. Propagation Delay vs Temperature**

**Figure 7-8. Reset Time Delay vs Temperature**

**Figure 7-9. Reset Time Delay vs CT Capacitance**
7.8 Typical Characteristics (continued)

Typical characteristics show the typical performance of the TLV840-Q1 device. Test conditions are $T_A = 25^\circ C$, $VDD = 3.3$ V, $R_{Pull-Up} = 100$ kΩ, $C_{LOAD} = 50$ pF, unless otherwise noted.

![Figure 7-10. $V_{OL}$ vs $I_{OL}$](image)

![Figure 7-11. $V_{OL}$ vs Temperature](image)
8 Detailed Description

8.1 Overview

The TLV840-Q1 is a family of nano-quiescent current voltage detectors with fixed threshold voltage. TLV840-Q1 features include programable reset time delay using external capacitor, active-low manual reset, 0.5% typical monitor threshold accuracy with hysteresis and glitch immunity.

Fixed negative threshold voltages (\(V_{IT^-}\)) can be factory set from 0.8 V to 5.4 V. TLV840-Q1 is available in SOT-23 5-pin industry standard package.

8.2 Functional Block Diagram

![Functional Block Diagram](image)

8.3 Feature Description

8.3.1 Input Voltage (VDD)

VDD pin is monitored by the internal comparator to indicate when VDD falls below the fixed threshold voltage. VDD also functions as the supply for the internal bandgap, internal regulator, state machine, buffers and other control logic blocks. Good design practice involve placing a 0.1 \(\mu\)F to 1 \(\mu\)F bypass capacitor at VDD input for noisy applications to ensure enough charge is available for the device to power up correctly.
8.3.1.1 VDD Hysteresis

The internal comparator has built-in hysteresis to avoid erroneous output reset release. If the voltage at the VDD pin falls below $V_{IT-}$, the output reset is asserted. When the voltage at the VDD pin goes above $V_{IT+}$ plus hysteresis ($V_{HYS}$) the output reset is deasserted after $t_D$ delay.

![Hysteresis Diagram](image)

**Figure 8-1. Hysteresis Diagram**

8.3.1.2 VDD Transient Immunity

The TLV840-Q1 is immune to quick voltage transients or excursion on VDD. Sensitivity to transients depends on both pulse duration ($t_{GI_VIT-}$) found in Section 7.6 and overdrive. Overdrive is defined by how much VDD deviates from the specified threshold. Threshold overdrive is calculated as a percent of the threshold in question, as shown in Equation 1.

$$\text{Overdrive} = |(V_{\text{DD}} / V_{\text{IT-}}) - 1| \times 100\%$$

![Overdrive Diagram](image)

**Figure 8-2. Overdrive vs Pulse Duration**
8.3.2 User-Programmable Reset Time Delay

The reset time delay can be set to a minimum value of 80 µs by leaving the CT pin floating, or a maximum value of approximately 6.2 seconds by connecting 10 µF delay capacitor. The reset time delay \( t_D \) can be programmed by connecting a capacitor no larger than 10 µF between CT pin and GND.

The relationship between external capacitor \( C_{CT} \) in µF at CT pin and the time delay \( t_D \) in seconds is given by Equation 2:

\[
 t_D \text{(typ)} = -\ln (0.29) \times R_{CT} \times C_{CT} + t_D \text{(no cap)}
\]  

Equation 3 solves for external capacitor (µF) by plugging \( R_{CT} \) and \( t_D \) (CT pin = Open) given in Section 7.5 section:

\[
 C_{CT} = (t_D - 80 \text{ µs}) \div 618937
\]  

The reset delay varies according to three variables: the external capacitor \( C_{CT} \), CT pin internal resistance \( R_{CT} \) provided in Section 7.5, and a constant. The minimum and maximum variance due to the constant is show in Equation 4 and Equation 5:

\[
 t_D \text{(min)} = -\ln (0.37) \times R_{CT \text{ (min)}} \times C_{CT\_EXT \text{ (min)}} + t_D \text{(no cap)}
\]

\[
 t_D \text{(max)} = -\ln (0.25) \times R_{CT \text{ (max)}} \times C_{CT\_EXT \text{ (max)}} + t_D \text{(no cap)}
\]

The recommended maximum delay capacitor for the TLV840-Q1 is limited to 10 µF as this ensures there is enough time for the capacitor to fully discharge when the reset condition occurs. When a voltage fault occurs, the previously charged up capacitor discharges, and if the monitored voltage returns from the fault condition before the delay capacitor discharges completely, the reset delay will be shorter than expected because the delay capacitor will begin charging from a voltage above zero. Larger delay capacitors can be used so long as the capacitor has enough time to fully discharge during the duration of the voltage fault. The amount of time required to discharge the delay capacitor relative to the reset delay increases as VDD overdrive increases as shown in Figure 8-3. From the graph below, to ensure the CT capacitor is fully discharged, the time period or duration of the voltage fault needs to be greater than 10% of the programmed reset time delay.

\[\text{Figure 8-3. } C_{CT} \text{ Discharge Time During Fault Condition (} V_{IT} = 2 \text{ V, } C_{CT} = 1 \text{ µF)}\]
8.3.3 Manual Reset (MR) Input

The manual reset (MR) input allows a processor GPIO or other logic circuits to initiate a reset. A logic low on MR with pulse duration longer than $t_{MR_{PW}}$ will cause the reset output to assert. After MR returns to a logic high ($V_{MR_{H}}$) and VDD is above $V_{IT+}$, reset is deasserted after the user programmed reset time delay ($t_D$) expires.

The minimum duration for which MR is held under $V_{MR_{L}}$ must be at least 1% of $t_{MR_{ID}}$. Otherwise, the effective reset delay will be shorter roughly by the difference between 1% of $t_{MR_{ID}}$ and the actual MR pulse width. For large capacitor based delays this difference could be noticeable unless care is taken to lengthen the MR pulse width.

MR is internally connected to VDD through a pull-up resistor $R_{MR}$ shown in Section 8.2. If the logic signal controlling MR is less than VDD, then additional current flows from VDD into MR internally. For minimum current consumption, drive MR to either VDD or GND. $V_{MR}$ should not be higher than VDD voltage.

![Figure 8-4. Timing Diagram MR and RESET](image-url)

(1) $t_{MR_{PW}}$ pulse width too small to assert RESET
(2) $V_{MR}$ voltage not low enough to assert RESET
8.3.4 Output Logic

8.3.4.1 RESET Output, Active-Low

RESET (Active-Low) applies to TLV840DL-Q1 (Open-Drain) and TLV840PL-Q1 (Push-Pull) hence the “L” in the device name. RESET remains high (deasserted) as long as VDD is above the negative threshold (V_{IT-}) and the MR pin is floating or above V_{MR_H}. If VDD falls below the negative threshold (V_{IT-}) or if MR is driven low, then RESET is asserted.

When MR is again logic high or floating and VDD rise above V_{IT+}, the delay circuit will hold RESET low for the specified reset time delay (t_D). When the reset time delay has elapsed, the RESET pin goes back to logic high voltage (V_{OH}).

The TLV840DL-Q1 (Open-Drain) version, denoted with "D" in the device name, requires an external pull-up resistor to hold RESET pin high. Connect the external pull-up resistor to the desired pull-up voltage source and RESET can be pulled up to any voltage up to 6.5 V independent of the VDD voltage. To ensure proper voltage levels, give some consideration when choosing the pull-up resistor values. The external pull-up resistor value determines the actual V_{OL}, the output capacitive loading, and the output leakage current (I_{lkg(OD)}).

The Push-Pull variants (TLV840PL-Q1 and TLV840PH-Q1), denoted with "P" in the device name, does not require an external pull-up resistor.

8.3.4.2 RESET Output, Active-High

RESET (Active-High), denoted with no bar above the pin label, applies to TLV840DH-Q1 (Open-Drain) and TLV840PH-Q1 push-pull active-high version, hence the "H" in the device name. RESET remains low (deasserted) as long as VDD is above the negative threshold (V_{IT-}) and the MR pin is floating or above V_{MR_H}. If VDD falls below the negative threshold (V_{IT-}) or if MR is driven low, then RESET is asserted driving the RESET pin to high voltage (V_{OH}).

When MR is again logic high or floating and VDD rise above V_{IT+} the delay circuit will hold RESET high for the specified reset time delay (t_D). When the reset time delay has elapsed, the RESET pin goes back to logic low voltage (V_{OL}).

The TLV840DH-Q1 (Open-Drain) version, denoted with "D" in the device name, requires an external pull-up resistor to hold RESET pin high. Connect the external pull-up resistor to the desired pull-up voltage source and RESET can be pulled up to any voltage up to 6.5 V independent of the VDD voltage. To ensure proper voltage levels, give some consideration when choosing the pull-up resistor values. The external pull-up resistor value determines the actual V_{OL}, the output capacitive loading, and the output leakage current (I_{lkg(OD)}).

The Push-Pull variants (TLV840PL-Q1 and TLV840PH-Q1), denoted with "P" in the device name, does not require an external pull-up resistor.
8.4 Device Functional Modes

Table 8-1 summarizes the various functional modes of the device. Logic high is represented by "H" and logic low is represented by "L".

<table>
<thead>
<tr>
<th>VDD</th>
<th>MR</th>
<th>RESET</th>
<th>RESET</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD &lt; V\text{POR}</td>
<td>Ignored</td>
<td>Undefined</td>
<td>Undefined</td>
</tr>
<tr>
<td>V_{\text{POR}} &lt; VDD &lt; V_{\text{IT.}}</td>
<td>Ignored</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>VDD ≥ V_{\text{IT.}}</td>
<td>L</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>VDD ≥ V_{\text{IT.}}</td>
<td>H</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>VDD ≥ V_{\text{IT.}}</td>
<td>Floating</td>
<td>L</td>
<td>H</td>
</tr>
</tbody>
</table>

### 8.4.1 Normal Operation (VDD > V\text{POR})

When VDD is greater than V_{\text{POR}}, the reset signal is determined by the voltage on the VDD pin with respect to the trip point (V_{\text{IT.}}):

- MR high: the reset signal corresponds to VDD with respect to the threshold voltage.
- MR low: in this mode, the reset is asserted regardless of the threshold voltage.

### 8.4.2 Below Power-On-Reset (VDD < V\text{POR})

When the voltage on VDD is lower than V_{\text{POR}}, the device does not have enough bias voltage to internally pull the asserted output low or high and reset voltage level is undefined.
9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The following sections describe in detail how to properly use this device, depending on the requirements of the final application.

9.2 Typical Application

9.2.1 Design 1: Dual Rail Monitoring with Power-up Sequencing

A typical application for the TLV840-Q1 is voltage rail monitoring and power-up sequencing as shown in Figure 9-1. The TLV840-Q1 can be used to monitor any rail above 0.9 V. In this design application, two TLV840-Q1 devices monitor two separate voltage rails and sequences the rails upon power-up. The TLV840MAPL29-Q1 is used to monitor the 3.3-V main power rail and the TLV840MADL10-Q1 is used to monitor the 1.2-V rail provided by the LDO for other system peripherals. The RESET output of the TLV840MAPL29-Q1 is connected to the enable (EN) input of the LDO. A reset event is initiated on either voltage supervisor when the VDD voltage is less than $V_{IT}$. For a system-wide reset event, both MR pins are tied to the SYS_RST. For the purpose of this application, the design detail on MR are not covered. For more information on the function of MR, please see Section 8.3.3.

Figure 9-1. TLV840-Q1 Voltage Rail Monitor and Power-Up Sequencer Design Block Diagram
9.2.1.1 Design Requirements

This design requires voltage supervision on two separate rails: 3.3-V and 1.2-V rails. The voltage rail needs to sequence upon power up with the 3.3-V rail coming up first followed by the 1.2-V rail at least 25 ms after.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>DESIGN REQUIREMENT</th>
<th>DESIGN RESULT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Two Rail Voltage Supervision</td>
<td>Monitor 3.3-V and 1.2-V rails</td>
<td>Two TLV840-Q1 devices provide voltage monitoring with 1% accuracy with device options available in 0.1 V variations</td>
</tr>
<tr>
<td>Voltage Rail Sequencing</td>
<td>Power up the 3.3-V rail first followed by 1.2-V rail 25 ms after</td>
<td>The CT capacitor on TLV840MAPL29-Q1 is set to 0.047 µF for a reset time delay of 29 ms typical</td>
</tr>
<tr>
<td>Maximum device current</td>
<td>1 µA</td>
<td>Each TLV840-Q1 requires 120 nA typical</td>
</tr>
<tr>
<td>consumption</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

9.2.1.2 Detailed Design Procedure

The primary constraint for this application is choosing the correct device to monitor the supply voltage of the microprocessor. The TLV840-Q1 can monitor any voltage between 0.8 V and 5.4 V. Depending on how far away from the nominal voltage rail the user wants the voltage supervisor to trigger determines the correct voltage supervisor variant to choose. In this example, the first TLV840-Q1 triggers when the 3.3-V rail falls to 2.9 V. The second TLV840-Q1 triggers a reset when the 1.2-V rail falls to 0.9 V. The secondary constraint for this application is the reset time delay that must be at least 25 ms to allow the microprocessor, and all other devices using the 3.3-V rail, enough time to startup correctly before the 1.2-V rail is enabled via the LDO. Because a minimum time is required, the user must account for capacitor tolerance. For applications with ambient temperatures ranging from –40°C to +125°C, \( C_{CT} \) can be calculated using \( R_{CT} \) and solving for \( C_{CT} \) in Equation 2. Solving Equation 2 for 25 ms gives a minimum capacitor value of 0.0403 µF which is rounded up to a standard value 0.047 µF to account for capacitor tolerance.

A 1 µF decoupling capacitor is connected to the VDD pin as a good analog design practice. The pull-up resistor is only required for the Open-Drain device variants and is calculated to ensure that \( V_{OL} \) does not exceed max limit given the Isink possible at the expected supply voltage. In this design example nominal VDD is 1.2 V but dropping to 0.9 V. In Section 7.5, max \( V_{OL} \) provides 15 µA l sink for 0.7 V VDD, which is the closest voltage to this design example. Using 15 µA of Isink and 300 mV max \( V_{OL} \) gives us 40 kΩ for the pull-up resistor. Any value higher than 40 kΩ would ensure that \( V_{OL} \) will not exceed 300 mV max specification.

9.2.1.3 Application Curves

![Figure 9-2. Startup Sequence Highlighting the Delay Between 3.3 V and 1.2 V Rails](image-url)
9.2.2 Application Curve: Adjusting Output Reset Delay on TLV840EVM

These application curves are taken with the TLV840EVM and they display a change in reset delay time with different capacitor values. The output reset delay time was designed with the ease of programability for the customer. Figure 9-3 displays an output reset delay time of 57.6 μs with no capacitor on the CT pin. Figure 9-4 and Figure 9-5 have output reset delay times of 5.42 ms and 56.8 ms, respectively. Both the output delay times and capacitors used resulted in an order of magnitude difference. Please see the TLV840EVM User Guide for more information.

![Figure 9-3. TLV840EVM RESET Time Delay (t_D) with No Capacitor](image)

![Figure 9-4. TLV840EVM RESET Time Delay (t_D) with 0.01-μF Capacitor](image)

![Figure 9-5. TLV840EVM RESET Time Delay (t_D) with 0.1-μF Capacitor](image)
10 Power Supply Recommendations

The TLV840 is designed to operate from an input supply with a voltage range between 0.7 V and 6 V. TI recommends an input supply capacitor between the VDD pin and GND pin. This device has a 6.5 V absolute maximum rating on the VDD pin. If the voltage supply providing power to VDD is susceptible to any large voltage transient that can exceed 6.5 V, additional precautions must be taken.
11 Layout

11.1 Layout Guidelines

Make sure that the connection to the VDD pin is low impedance. Good analog design practice recommends placing a minimum 0.1 µF ceramic capacitor as near as possible to the VDD pin. If a capacitor is not connected to the CT pin, then minimize parasitic capacitance on this pin so the rest time delay is not adversely affected.

- Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a > 0.1 µF ceramic capacitor as near as possible to the VDD pin.
- If a $C_{CT}$ capacitor is used, place these components as close as possible to the CT pin. If the CT pin is left unconnected, make sure to minimize the amount of parasitic capacitance on the pin to < 5 pF.
- Place the pull-up resistors on RESET pin as close to the pin as possible.

11.2 Layout Example

The layout example in shows how the TLV840DL-Q1 is laid out on a printed circuit board (PCB) with a user-defined delay.

![Figure 11-1. TLV840M-Q1 Recommended Layout](image)
12 Device and Documentation Support

12.1 Device Nomenclature

Table 12-1 shows how to decode the function of the device based on its part number.

<table>
<thead>
<tr>
<th>DESCRIPTION</th>
<th>NOMENCLATURE</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Generic Part number</td>
<td>TLV840</td>
<td>TLV840</td>
</tr>
<tr>
<td>Feature Option</td>
<td>M 1</td>
<td>Manual Reset option in addition to CT pin</td>
</tr>
<tr>
<td>Delay Option</td>
<td>A</td>
<td>40 μs (Default internal reset time delay)</td>
</tr>
<tr>
<td>Variant code (Output Topology)</td>
<td>DL</td>
<td>Open-Drain, Active-Low</td>
</tr>
<tr>
<td></td>
<td>PL</td>
<td>Push-Pull, Active-Low</td>
</tr>
<tr>
<td></td>
<td>DH</td>
<td>Open-Drain, Active-High</td>
</tr>
<tr>
<td></td>
<td>PH</td>
<td>Push-Pull, Active-High</td>
</tr>
<tr>
<td>Detect Voltage Option</td>
<td>## (two characters)</td>
<td>Example: 12 stands for 1.2 V threshold</td>
</tr>
<tr>
<td>Package</td>
<td>DBV</td>
<td>SOT23-5</td>
</tr>
<tr>
<td>Reel</td>
<td>R</td>
<td>Large Reel</td>
</tr>
<tr>
<td>Automotive Version</td>
<td>Q1</td>
<td>AEC-Q100</td>
</tr>
</tbody>
</table>

1. Orderable part numbers with TLV840M-Q1 are only available with the delay option A. However, longer delays can be achieved through an external capacitor on the CT pin. Leaving the CT pin floating will result in typical 40 μs delay feature option.
12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

12.4 Trademarks

All trademarks are the property of their respective owners.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead finish/Ball material</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>P840MADL13DBVRQ1</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>3000</td>
<td>Non-RoHS &amp; Non-Green</td>
<td>Call TI</td>
<td>Call TI</td>
<td>-40 to 125</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TLV840MADL22DBVRQ1</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>3000</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>2HOF</td>
<td>Samples</td>
</tr>
<tr>
<td>TLV840MADL30DBVRQ1</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>3000</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>2HPF</td>
<td>Samples</td>
</tr>
<tr>
<td>TLV840MADL31DBVRQ1</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>3000</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>2HMF</td>
<td>Samples</td>
</tr>
<tr>
<td>TLV840MADL40DBVRQ1</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>3000</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>2HDF</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE:** Product device recommended for new designs.
- **LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
- **RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
- **Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead finish/Ball material** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TLV840-Q1:**

- Catalog : TLV840

**NOTE:** Qualified Version Definitions:

- Catalog - TI's standard catalog product
## TAPE AND REEL INFORMATION

*All dimensions are nominal.*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLV840MADL22DBVRQ1</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>3000</td>
<td>180.0</td>
<td>8.4</td>
<td>3.2</td>
<td>3.2</td>
<td>1.4</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
</tr>
<tr>
<td>TLV840MADL30DBVRQ1</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>3000</td>
<td>180.0</td>
<td>8.4</td>
<td>3.2</td>
<td>3.2</td>
<td>1.4</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
</tr>
<tr>
<td>TLV840MADL31DBVRQ1</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>3000</td>
<td>180.0</td>
<td>8.4</td>
<td>3.2</td>
<td>3.2</td>
<td>1.4</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
</tr>
<tr>
<td>TLV840MADL40DBVRQ1</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>3000</td>
<td>180.0</td>
<td>8.4</td>
<td>3.2</td>
<td>3.2</td>
<td>1.4</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
</tr>
</tbody>
</table>
### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLV840MADL22DBVRQ1</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>3000</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
<tr>
<td>TLV840MADL30DBVRQ1</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>3000</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
<tr>
<td>TLV840MADL31DBVRQ1</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>3000</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
<tr>
<td>TLV840MADL40DBVRQ1</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>3000</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
design recommendations.
8. Board assembly site may have different recommendations for stencil design.
IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (https://www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2021, Texas Instruments Incorporated