TLV900x-Q1 Low-Power RRIO 1-MHz Automotive Operational Amplifier

1 Features

- AEC-Q100 qualified for automotive applications
  - Temperature grade 1: –40°C to +125°C, T_A
  - Device HBM ESD classification level 3A
  - Device CDM ESD classification level C6
- Scalable CMOS amplifier for low-cost applications
- Rail-to-rail input and output
- Low input offset voltage: ±0.4 mV
- Unity-gain bandwidth: 1 MHz
- Low broadband noise: 27 nV/√Hz
- Low input bias current: 5 pA
- Low quiescent current: 60 µA/Ch
- Unity-gain stable
- Internal RFI and EMI filter
- Operational at supply voltages as low as 1.8 V
- Easier to stabilize with higher capacitive load due to resistive open-loop output impedance

2 Applications

- Optimized for AEC-Q100 grade 1 applications
- Infotainment
- Passive safety
- Body electronics and lighting
- HEV/EV inverter and motor control
- Sensor signal conditioning
- Power modules
- Active filters
- Low-side current sensing

3 Description

The TLV900x-Q1 family includes dual (TLV9002-Q1) and quad-channel (TLV9004-Q1) low-voltage (1.8 V to 5.5 V) operational amplifiers (op amps) with rail-to-rail input and output swing capabilities. These op amps provide a cost-effective solution for space-constrained automotive applications such as infotainment and lighting where low-voltage operation and high capacitive-load drive are required. The capacitive-load drive of the TLV900x-Q1 family is 500 pF, and the resistive open-loop output impedance makes stabilization easier with much higher capacitive loads. These op amps are designed specifically for low-voltage operation (1.8 V to 5.5 V) with performance specifications similar to the TLV600x-Q1 devices.

The robust design of the TLV900x-Q1 family simplifies circuit design. The op amps feature unity-gain stability, an integrated RFI and EMI rejection filter, and no-phase reversal in overdrive conditions.

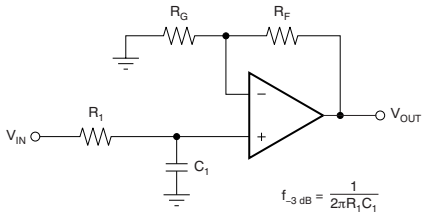
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV9002-Q1	SOIC (8)(2)	3.91 mm × 4.90 mm
	TSSOP (8)(2)	3.00 mm × 4.40 mm
	VSSOP (8)(2)	3.00 mm × 3.00 mm
TLV9004-Q1	SOIC (14)(2)	8.65 mm × 3.91 mm
	TSSOP (14)(2)	4.40 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) Package is for preview only.

Single-Pole, Low-Pass Filter



$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR_1C_1}\right)$$

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2019	*	Initial release.

5 Device Comparison Table

DEVICE	NO. OF CHANNELS	PACKAGE LEADS		
		SOIC D	TSSOP PW	VSSOP DGK
TLV9002-Q1	2	8	8	8
TLV9004-Q1	4	14	14	—

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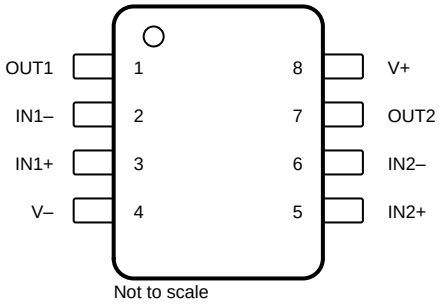
6 Pin Configuration and Functions

TLV9002-Q1 D, DGK, PW Packages
8-Pin SOIC, VSSOP, TSSOP
Top View



Not to scale

Pin Functions: TLV9002-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1–	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2–	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V–	4	I or —	Negative (low) supply or ground (for single-supply operation)
V+	8	I	Positive (high) supply

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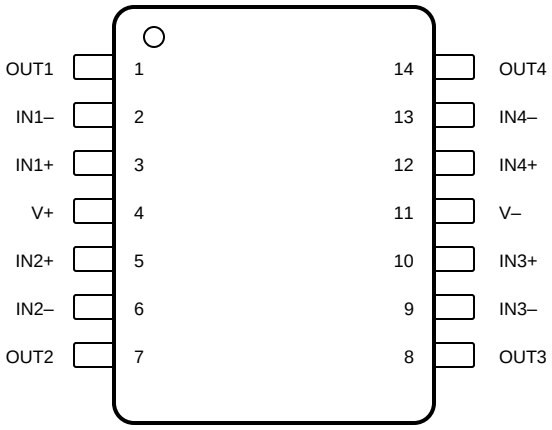
TLV9004-Q1 D, PW Packages
14-Pin SOIC, TSSOP
Top View



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Pin Functions: TLV9004-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1–	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2–	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
IN3–	9	I	Inverting input, channel 3
IN3+	10	I	Noninverting input, channel 3
IN4–	13	I	Inverting input, channel 4
IN4+	12	I	Noninverting input, channel 4
NC	—	—	No internal connection
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
OUT3	8	O	Output, channel 3
OUT4	14	O	Output, channel 4
V–	11	I or —	Negative (low) supply or ground (for single-supply operation)
V+	4	I	Positive (high) supply

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7 Specifications

7.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Supply voltage (V+) – (V–)				6	V
Signal input pins	Voltage(2)	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential		(V+) – (V–) + 0.2	V
	Current(2)		–10	10	mA
Output short-circuit(3)			Continuous		
Operating, T_A			–55	150	°C
Junction, T_J				150	°C
Storage, T_{stg}			–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC-Q100-002(1) HBM ESD Classification Level 3A	±2000	V
		Charged-device model (CDM), per AEC-Q100-011 CDM ESD Classification Level C4B	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage	1.8	5.5	V
T_A	Specified temperature	–40	125	°C

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7.4 Thermal Information: TLV9002-Q1

THERMAL METRIC(1)		TLV9002-Q1			UNIT
		D (SOIC)	DGK (VSSOP)	PW (TSSOP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	207.9	201.2	200.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	92.8	85.7	95.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	129.7	122.9	128.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	26	21.2	27.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	127.9	121.4	127.2	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

7.5 Thermal Information: TLV9004-Q1

THERMAL METRIC(1)		TLV9004-Q1		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	102.1	148.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.8	68.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	58.5	92.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	20.5	16.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	58.1	91.8	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

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7.6 Electrical Characteristics

For V_S = (V+) – (V–) = 1.8 V to 5.5 V (±0.9 V to ±2.75 V), T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, and V_{CM} = V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 5 V		±0.4	±1.6	mV
		V_S = 5 V, T_A = –40°C to 125°C			±2	mV
dV_{OS}/dT	V_{OS} vs temperature	T_A = –40°C to 125°C		±0.6		µV/°C
PSRR	Power-supply rejection ratio	V_S = 1.8 to 5.5 V, V_{CM} = (V–)	80	105		dB
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	No phase reversal, rail-to-rail input	(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	V_S = 1.8 V, (V–) – 0.1 V < V_{CM} < (V+) – 1.4 V T_A = –40°C to 125°C		86		dB
		V_S = 5.5 V, (V–) – 0.1 V < V_{CM} < (V+) – 1.4 V T_A = –40°C to 125°C		95		
		V_S = 5.5 V, (V–) – 0.1 V < V_{CM} < (V+) + 0.1 V T_A = –40°C to 125°C	63	77		
		V_S = 1.8 V, (V–) – 0.1 V < V_{CM} < (V+) + 0.1 V T_A = –40°C to 125°C		68		
INPUT BIAS CURRENT						
I_B	Input bias current	V_S = 5 V		±5		pA
I_{OS}	Input offset current			±2		pA
NOISE						
E_n	Input voltage noise (peak-to-peak)	f = 0.1 Hz to 10 Hz, V_S = 5 V		4.7		μV_{PP}
e_n	Input voltage noise density	f = 1 kHz, V_S = 5 V		30		nV/√Hz
		f = 10 kHz, V_S = 5 V		27		
i_n	Input current noise density	f = 1 kHz, V_S = 5 V		23		fA/√Hz
INPUT CAPACITANCE						
C_{ID}	Differential			1.5		pF
C_{IC}	Common-mode			5		pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	V_S = 5.5 V, (V–) + 0.05 V < V_O < (V+) – 0.05 V R_L = 10 kΩ	104	117		dB
		V_S = 1.8 V, (V–) + 0.04 V < V_O < (V+) – 0.04 V R_L = 10 kΩ		100		
		V_S = 1.8 V, (V–) + 0.1 V < V_O < (V+) – 0.1 V, R_L = 2 kΩ		115		
		V_S = 5.5 V, (V–) + 0.15 V < V_O < (V+) – 0.15 V R_L = 2 kΩ		130		
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	V_S = 5 V		1		MHz
φ_m	Phase margin	V_S = 5.5 V, G = 1		78		°
SR	Slew rate	V_S = 5 V		2		V/µs
t_S	Settling time	To 0.1%, V_S = 5 V, 2-V step , G = +1, C_L = 100 pF		2.5		µs
		To 0.01%, V_S = 5 V, 2-V step , G = +1, C_L = 100 pF		3		
t_{OR}	Overload recovery time	V_S = 5 V, V_{IN} × gain > V_S		0.85		µs
THD+N	Total harmonic distortion + noise	V_S = 5.5 V, V_{CM} = 2.5 V, V_O = 1 V_{RMS}, G = +1 f = 1 kHz, 80-kHz measurement BW		0.004%		
OUTPUT						
V_O	Voltage output swing from supply rails	V_S = 5.5 V, R_L = 10 kΩ		10	20	mV
		V_S = 5.5 V, R_L = 2 kΩ		35	55	
I_{SC}	Short-circuit current	V_S = 5.5 V		±40		mA
Z_O	Open-loop output impedance	V_S = 5 V, f = 1 MHz		1200		Ω

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Electrical Characteristics (continued)

For V_S = (V+) – (V–) = 1.8 V to 5.5 V (±0.9 V to ±2.75 V), T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, and V_{CM} = V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_S	Specified voltage range		1.8 (±0.9)		5.5 (±2.75)	V
I_Q	Quiescent current per amplifier	I_O = 0 mA, V_S = 5.5 V		60	80	µA
		I_O = 0 mA, V_S = 5.5 V, T_A = –40°C to 125°C			85	

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7.7 Typical Characteristics

at T_A = 25°C, V+ = 2.75 V, V– = –2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

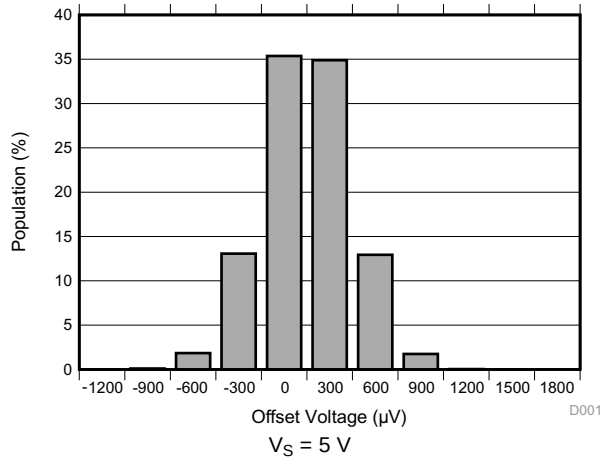


Figure 1. Offset Voltage Distribution Histogram

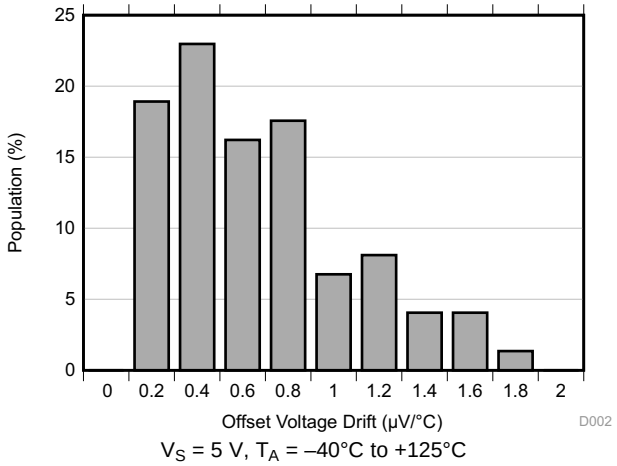


Figure 2. Offset Voltage Drift Distribution Histogram

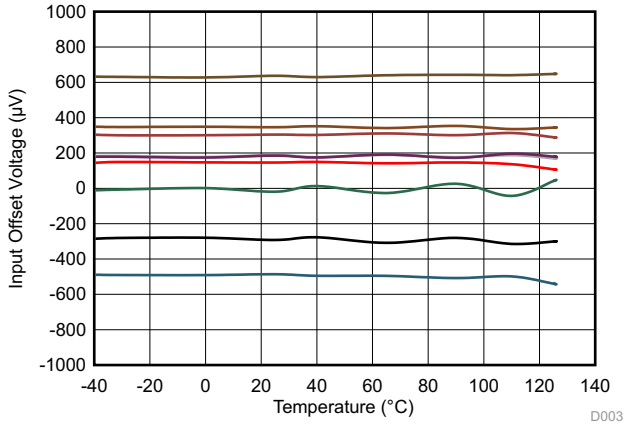


Figure 3. Input Offset Voltage vs Temperature

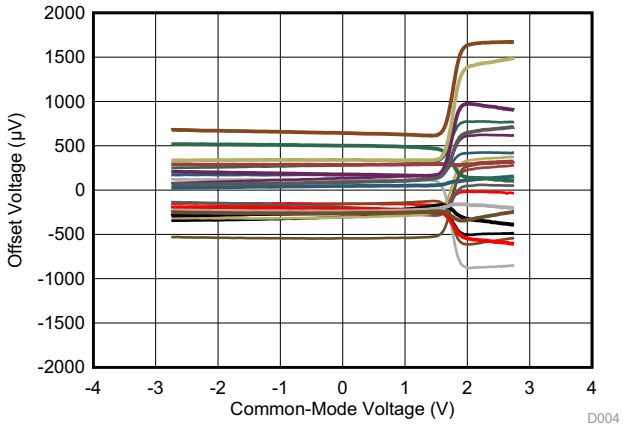


Figure 4. Offset Voltage vs Common-Mode

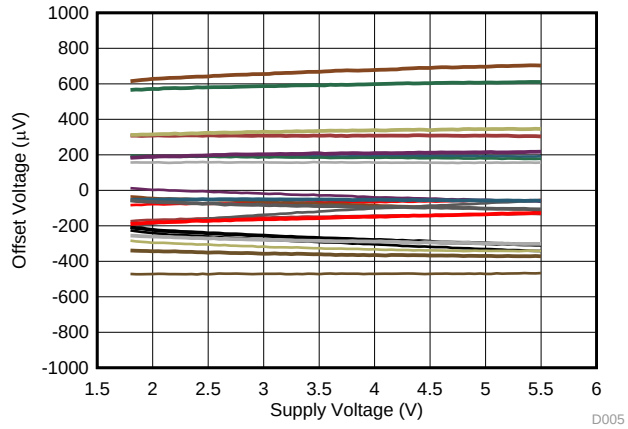


Figure 5. Offset Voltage vs Supply Voltage

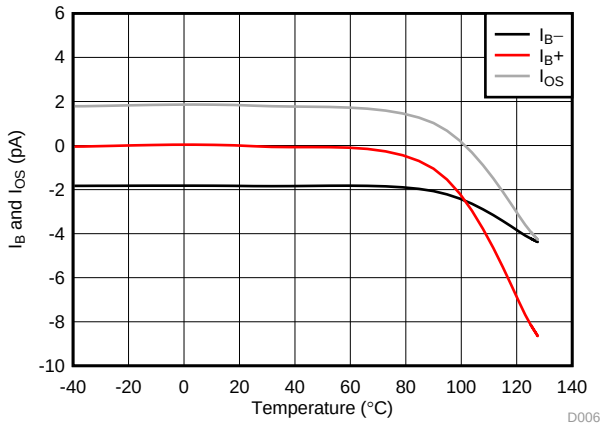


Figure 6. I_B and I_{OS} vs Temperature

ADVANCE INFORMATION

Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75 V, V– = –2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

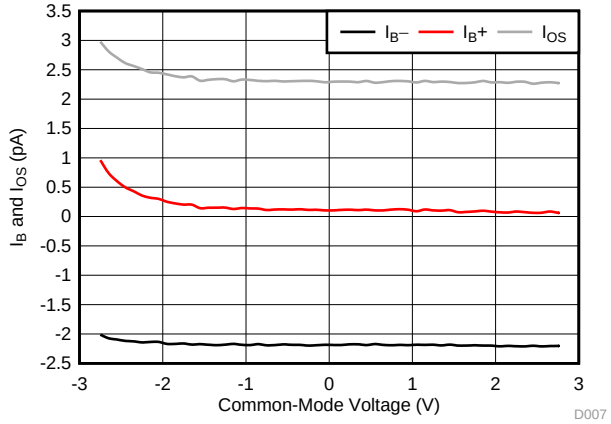


Figure 7. I_B and I_{OS} vs Common-Mode Voltage

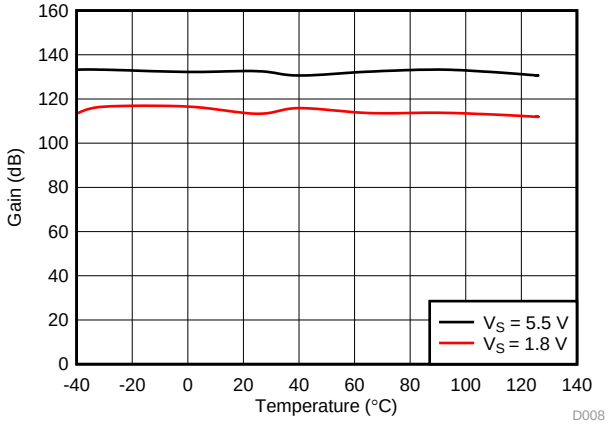


Figure 8. Open-Loop Gain vs Temperature

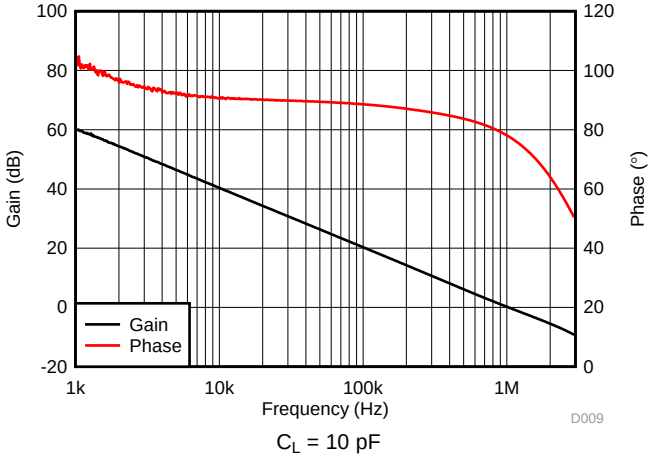


Figure 9. Open-Loop Gain and Phase vs Frequency

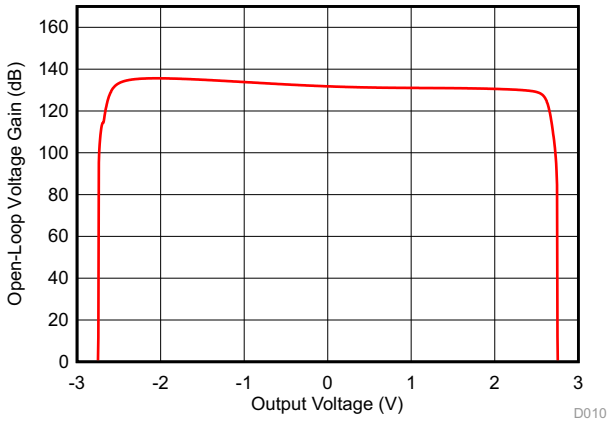


Figure 10. Open-Loop Gain vs Output Voltage

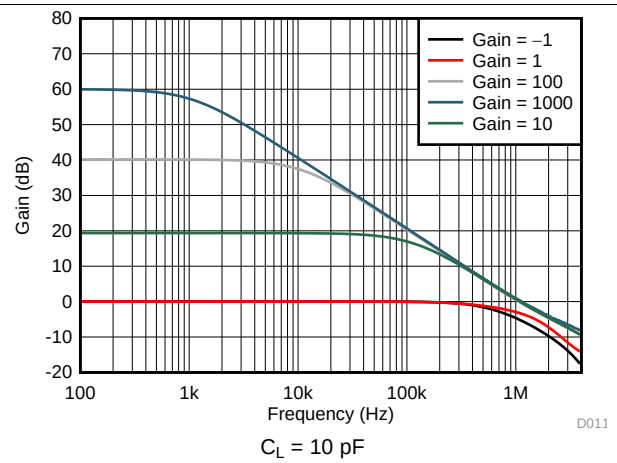


Figure 11. Closed-Loop Gain vs Frequency

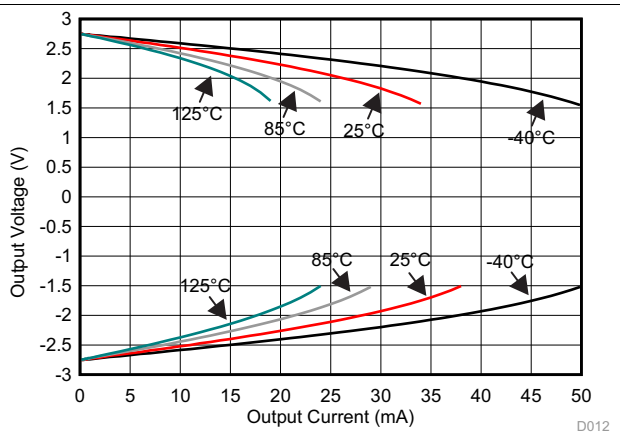


Figure 12. Output Voltage vs Output Current (Claw)

ADVANCE INFORMATION

Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75 V, V– = –2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

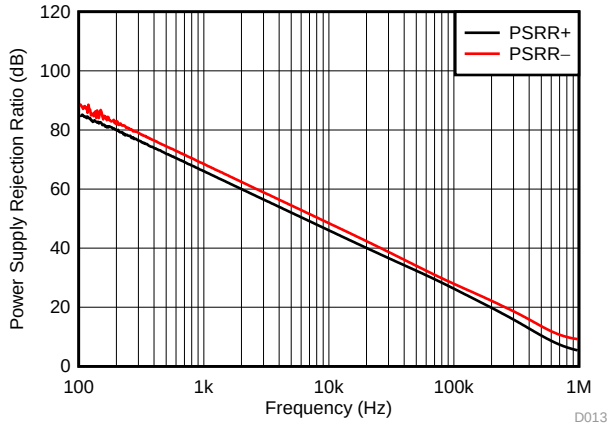
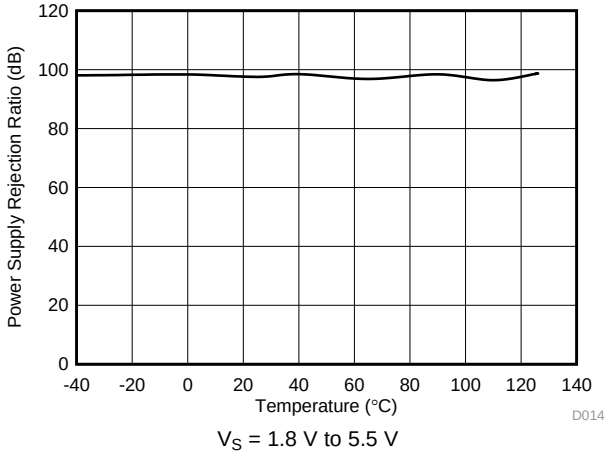


Figure 13. PSRR vs Frequency



V_S = 1.8 V to 5.5 V

Figure 14. DC PSRR vs Temperature

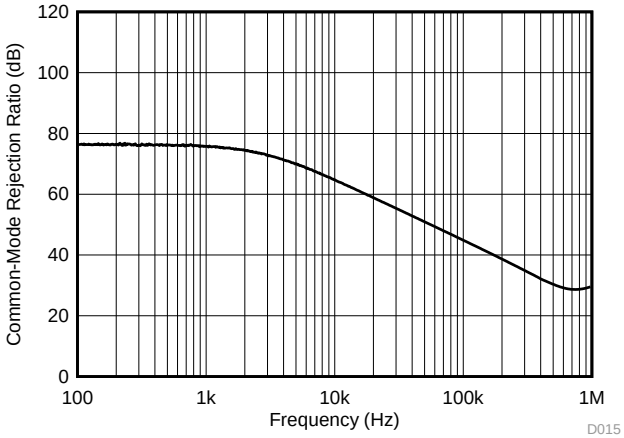
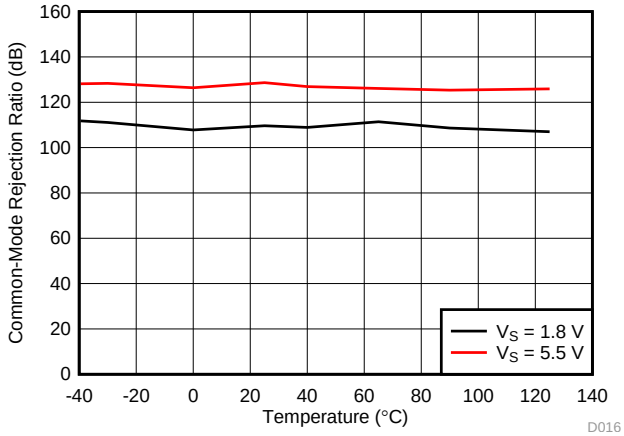


Figure 15. CMRR vs Frequency



V_{CM} = (V–) – 0.1 V to (V+) – 1.4 V

Figure 16. DC CMRR vs Temperature

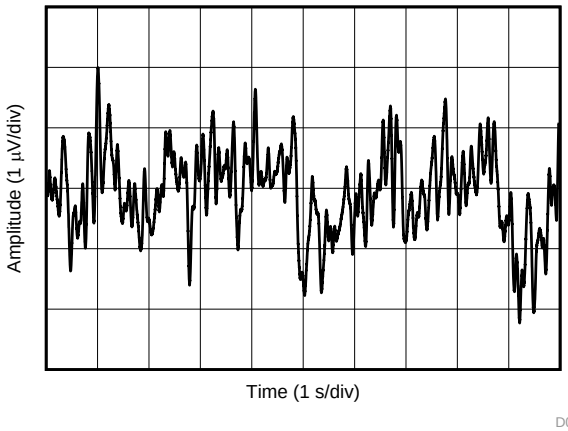


Figure 17. 0.1 Hz to 10 Hz Integrated Voltage Noise

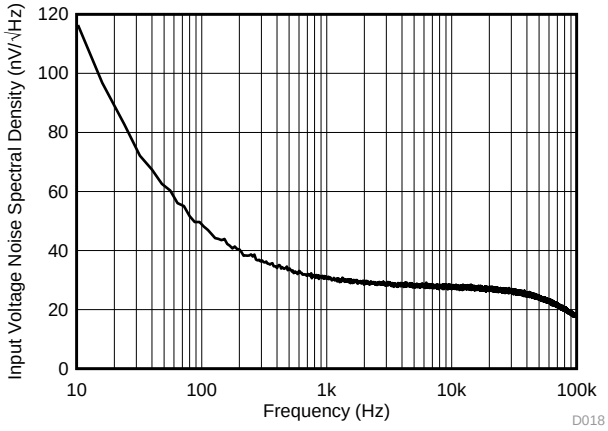
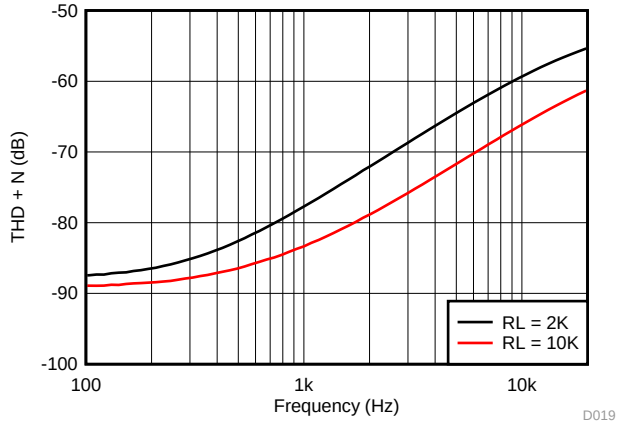


Figure 18. Input Voltage Noise Spectral Density

ADVANCE INFORMATION

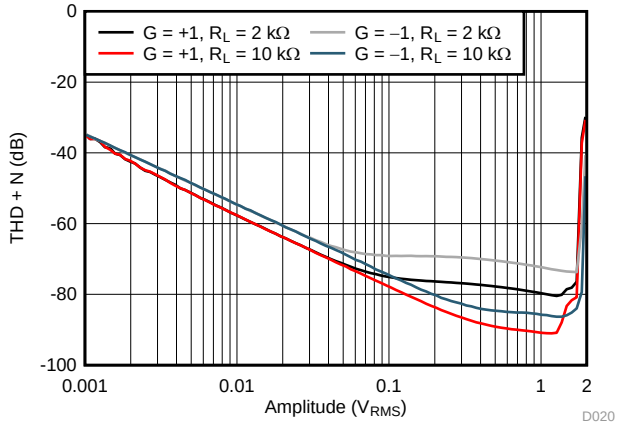
Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75 V, V– = –2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



V_S = 5.5 V V_{CM} = 2.5 V G = 1
BW = 80 kHz V_{OUT} = 0.5 V_{RMS}

Figure 19. THD + N vs Frequency



V_S = 5.5 V V_{CM} = 2.5 V f = 1 kHz
G = 1 BW = 80 kHz

Figure 20. THD + N vs Amplitude

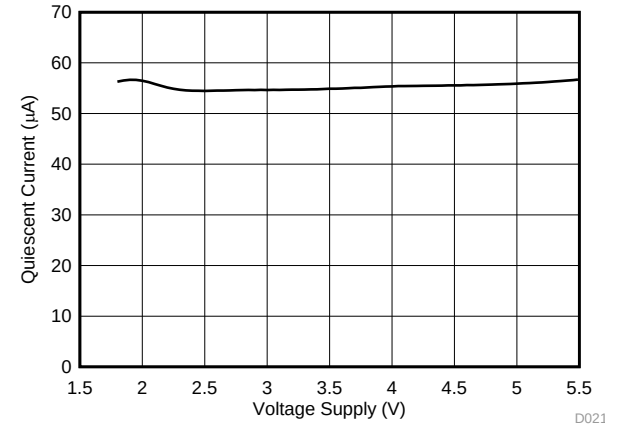


Figure 21. Quiescent Current vs Supply Voltage

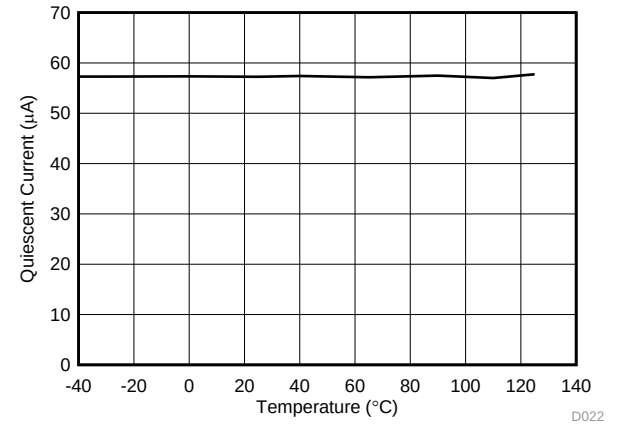


Figure 22. Quiescent Current vs Temperature

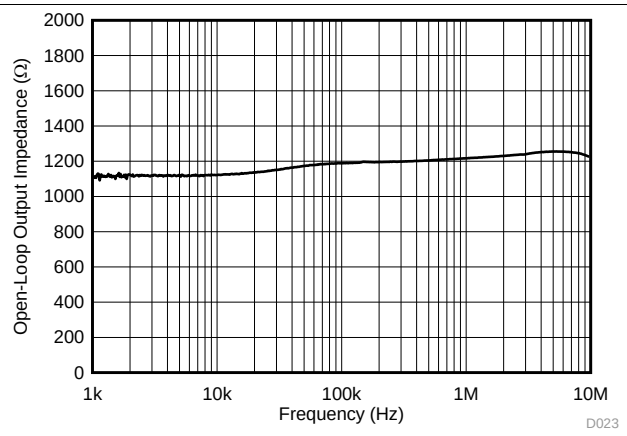
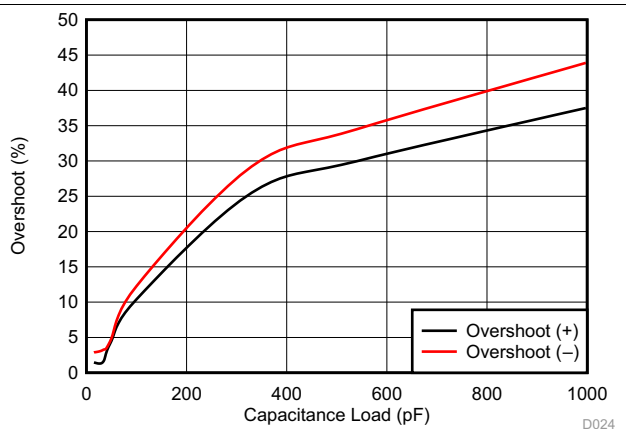


Figure 23. Open-Loop Output Impedance vs Frequency



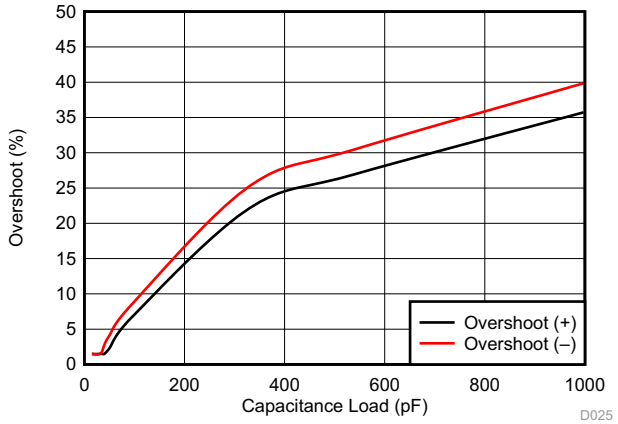
G = 1 V_{IN} = 100 mVpp

Figure 24. Small Signal Overshoot vs Capacitive Load

ADVANCE INFORMATION

Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75 V, V– = –2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



G = –1 V_{IN} = 100 mVpp

Figure 25. Small Signal Overshoot vs Capacitive Load

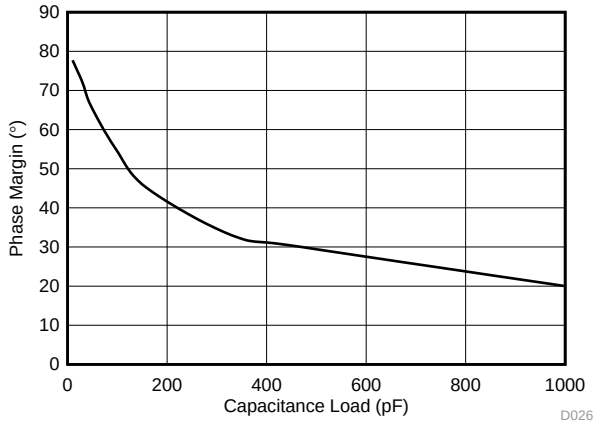
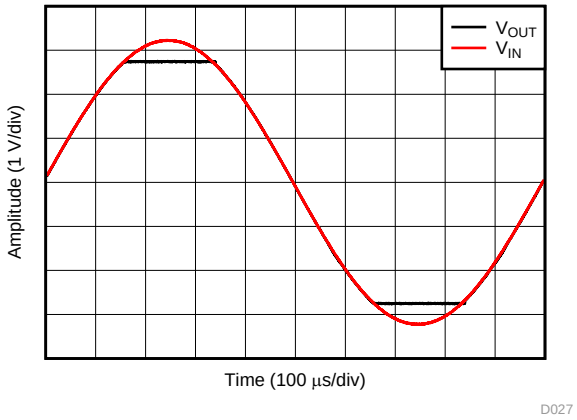
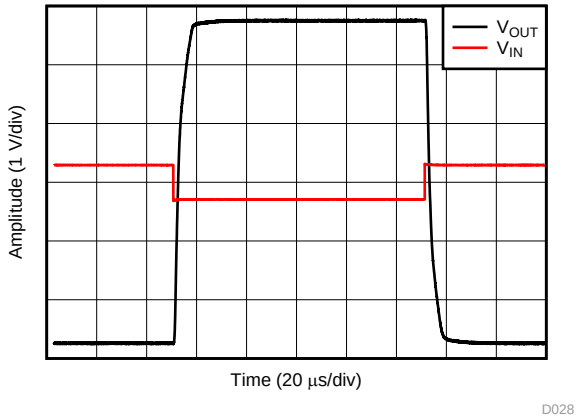


Figure 26. Phase Margin vs Capacitive Load



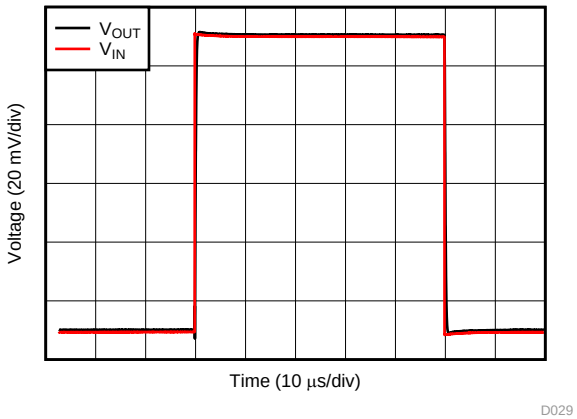
G = 1 V_{IN} = 6.5 V_{PP}

Figure 27. No Phase Reversal



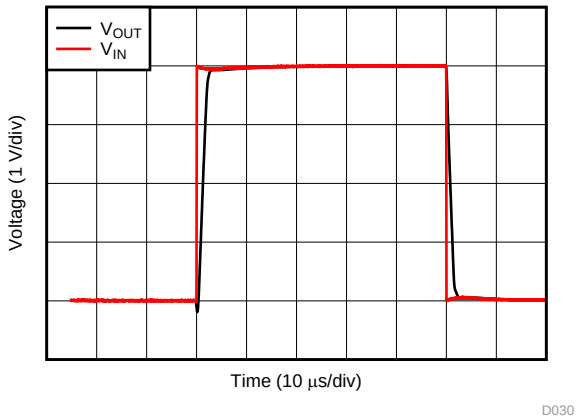
G = –10 V_{IN} = 600 mV_{PP}

Figure 28. Overload Recovery



G = 1 V_{IN} = 100 mV_{PP} C_L = 10 pF

Figure 29. Small-Signal Step Response



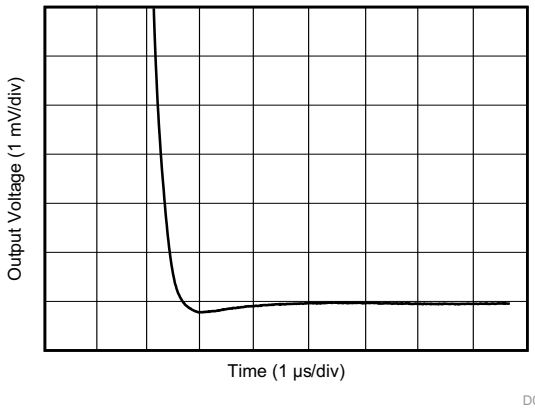
G = 1 V_{IN} = 4 V_{PP} C_L = 10 pF

Figure 30. Large-Signal Step Response

ADVANCE INFORMATION

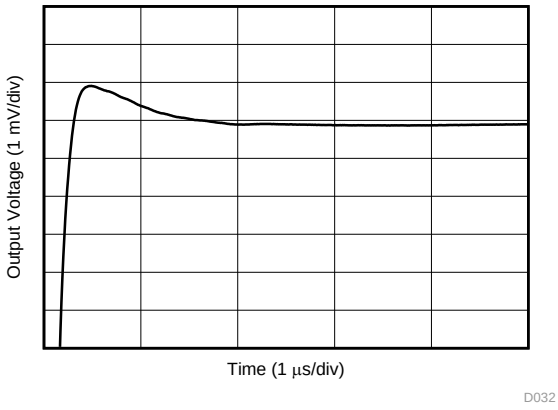
Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75 V, V– = –2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



G = 1 C_L = 100 pF 2-V step

Figure 31. Large-Signal Settling Time (Negative)



G = 1 C_L = 100 pF 2-V step

Figure 32. Large-Signal Settling Time (Positive)

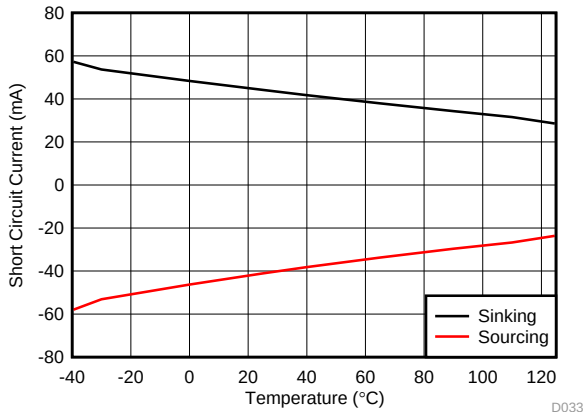


Figure 33. Short-Circuit Current vs Temperature

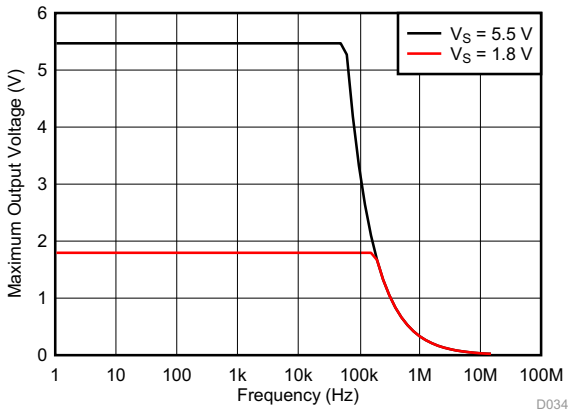


Figure 34. Maximum Output Voltage vs Frequency

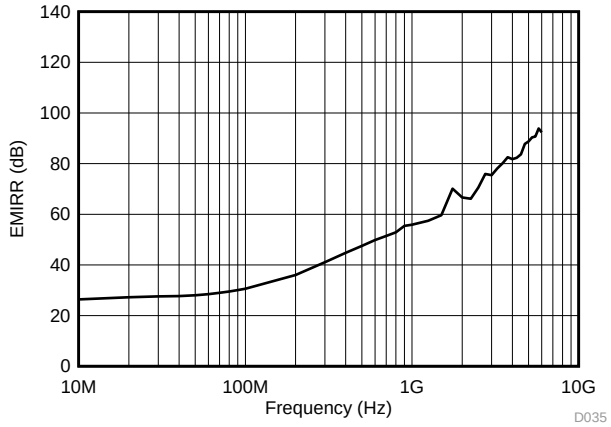


Figure 35. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency

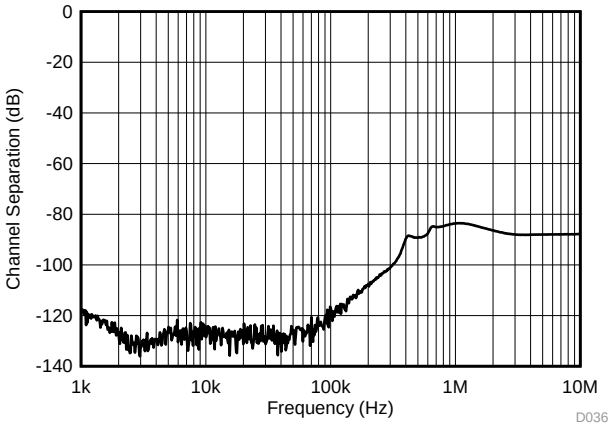


Figure 36. Channel Separation

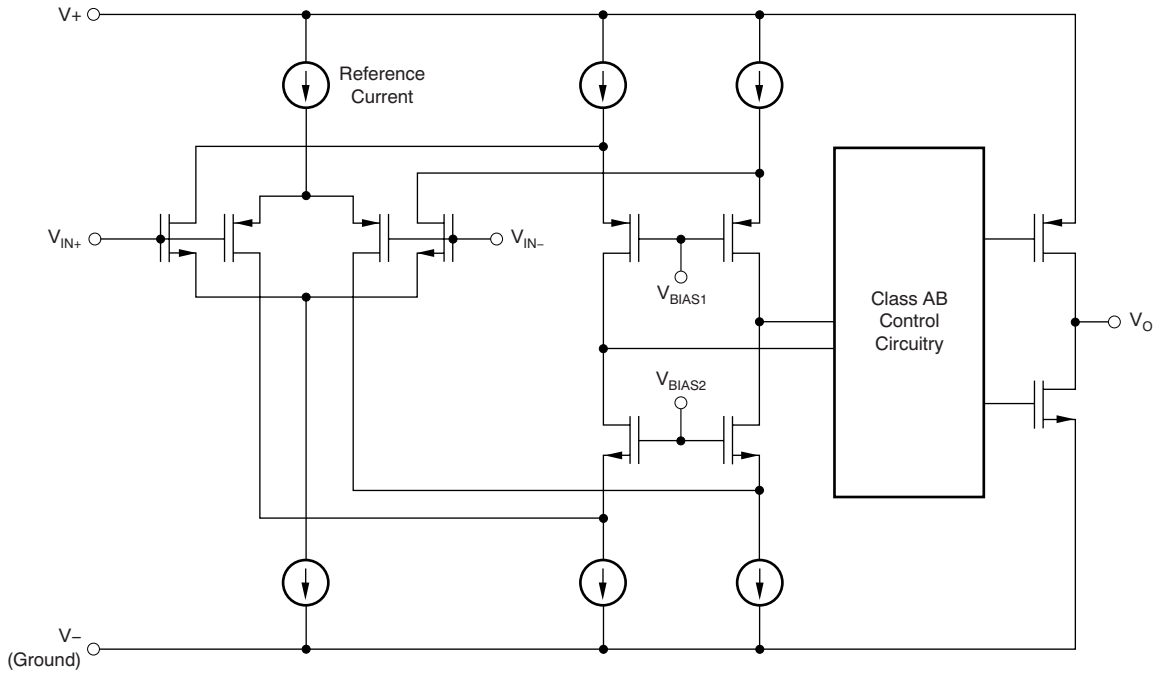
ADVANCE INFORMATION

8 Detailed Description

8.1 Overview

The TLV900x-Q1 is a family of automotive qualified, low-power, rail-to-rail input and output op amps. These devices operate from 1.8 V to 5.5 V, are unity-gain stable, and are designed for a wide range of general-purpose applications. The input common-mode voltage range includes both rails and allows the TLV900x-Q1 family to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes them suitable for driving sampling analog-to-digital converters (ADCs).

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Operating Voltage

The TLV900x-Q1 family of op amps are for operation from 1.8 V to 5.5 V. In addition, many specifications such as input offset voltage, quiescent current, offset current, and short circuit current apply from –40°C to 125°C. Parameters that vary significantly with operating voltages or temperature are shown in the typical characteristics section.

8.3.2 Rail-to-Rail Input

The input common-mode voltage range of the TLV900x-Q1 family extends 100 mV beyond the supply rails for the full supply voltage range of 1.8 V to 5.5 V. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as shown in the *Functional Block Diagram* section. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.4 V to 100 mV above the positive supply, whereas the P-channel pair is active for inputs from 100 mV below the negative supply to approximately (V+) – 1.4 V. There is a small transition region, typically (V+) – 1.2 V to (V+) – 1 V, in which both pairs are on. This 100-mV transition region can vary up to 100 mV with process variation. Thus, the transition region (with both stages on) can range from (V+) – 1.4 V to (V+) – 1.2 V on the low end, and up to (V+) – 1 V to (V+) – 0.8 V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can degrade compared to device operation outside this region.

8.3.3 Rail-to-Rail Output

Designed as a low-power, low-voltage operational amplifier, the TLV900x-Q1 family delivers a robust output drive capability. A class-AB output stage with common-source transistors achieves full rail-to-rail output swing capability. For resistive loads of 10 kΩ, the output swings to within 20 mV of either supply rail, regardless of the applied power-supply voltage. Different load conditions change the ability of the amplifier to swing close to the rails.

8.3.4 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, because of the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return to the linear state. After the charge carriers return to the linear state, the device begins to slew at the specified slew rate. Therefore, the propagation delay (in case of an overload condition) is the sum of the overload recovery time and the slew time. The overload recovery time for the TLV900x-Q1 family is approximately 850 ns.

8.4 Device Functional Modes

The TLV900x-Q1 family has a single functional mode. The devices are powered on as long as the power-supply voltage is between 1.8 V (±0.9 V) and 5.5 V (±2.75 V).

ADVANCE INFORMATION

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TLV900x-Q1 family of low-power, rail-to-rail input and output operational amplifiers is specifically designed for portable applications. The devices operate from 1.8 V to 5.5 V, are unity-gain stable, and are suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving less than or equal to 10-kΩ loads connected to any point between V+ and V–. The input common-mode voltage range includes both rails, and allows the TLV900x-Q1 devices to be used in any single-supply application.

9.2 Typical Application

9.2.1 TLV900x-Q1 Low-Side, Current Sensing Application

Figure 37 shows the TLV900x-Q1 configured in a low-side current sensing application.

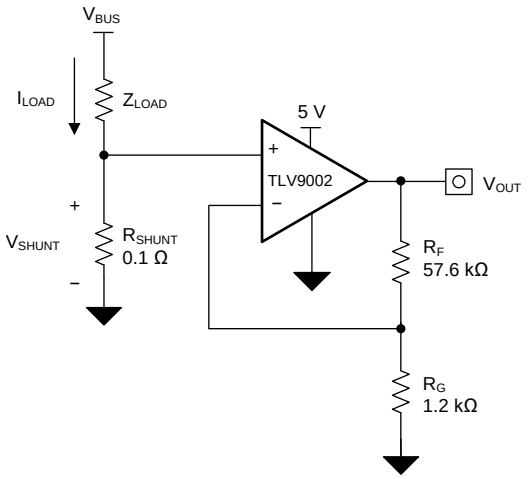


Figure 37. TLV900x-Q1 in a Low-Side, Current-Sensing Application

ADVANCE INFORMATION

Typical Application (continued)

9.2.1.1 Design Requirements

The design requirements for this design are:

- Load current: 0 A to 1 A
- Output voltage: 4.9 V
- Maximum shunt voltage: 100 mV

9.2.1.2 Detailed Design Procedure

The transfer function of the circuit in Figure 37 is given in Equation 1:

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times Gain \quad (1)$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0 A to 1 A. To keep the shunt voltage below 100 mV at maximum load current, the largest shunt resistor is shown using Equation 2:

$$R_{SHUNT} = \frac{V_{SHUNT\_MAX}}{I_{LOAD\_MAX}} = \frac{100mV}{1A} = 100m\Omega \quad (2)$$

Using Equation 2, R_{SHUNT} is calculated to be 100 mΩ. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the TLV900x-Q1 to produce an output voltage of approximately 0 V to 4.9 V. The gain needed by the TLV900x-Q1 to produce the necessary output voltage is calculated using Equation 3:

$$Gain = \frac{\left(V_{OUT\_MAX} - V_{OUT\_MIN}\right)}{\left(V_{IN\_MAX} - V_{IN\_MIN}\right)} \quad (3)$$

Using Equation 3, the required gain is calculated to be 49 V/V, which is set with resistors R_F and R_G. Equation 4 sizes the resistors R_F and R_G, to set the gain of the TLV900x-Q1 to 49 V/V.

$$Gain = 1 + \frac{\left(R_F\right)}{\left(R_G\right)} \quad (4)$$

Selecting R_F as 57.6 kΩ and R_G as 1.2 kΩ provides a combination that equals 49 V/V. Figure 38 shows the measured transfer function of the circuit shown in Figure 37. Notice that the gain is only a function of the feedback and gain resistors. This gain is adjusted by varying the ratio of the resistors and the actual resistors values are determined by the impedance levels that the designer wants to establish. The impedance level determines the current drain, the effect that stray capacitance has, and a few other behaviors. There is no optimal impedance selection that works for every system, you must choose an impedance that is ideal for your system parameters.

9.2.1.3 Application Curve

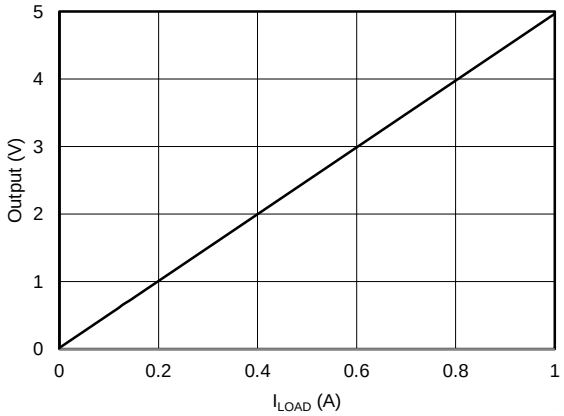


Figure 38. Low-Side, Current-Sense Transfer Function

ADVANCE INFORMATION

Typical Application (continued)

9.2.2 Single-Supply Photodiode Amplifier

Photodiodes are used in many applications to convert light signals to electrical signals. The current through the photodiode is proportional to the photon energy absorbed, and is commonly in the range of a few hundred picoamps to a few tens of microamps. An amplifier in a transimpedance configuration is typically used to convert the low-level photodiode current to a voltage signal for processing in an MCU. The circuit shown in Figure 39 is an example of a single-supply photodiode amplifier circuit using the TLV9002-Q1.

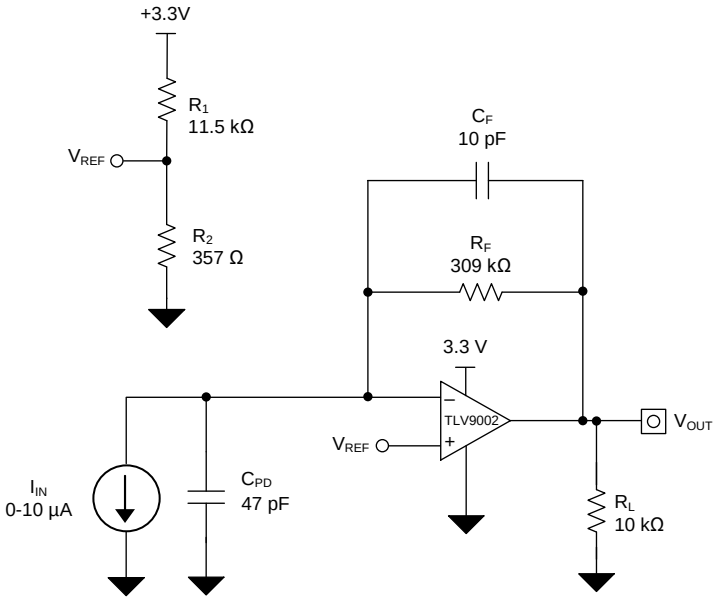


Figure 39. Single-Supply Photodiode Amplifier Circuit

ADVANCE INFORMATION

Typical Application (continued)

9.2.2.1 Design Requirements

The design requirements for this design are:

- Supply voltage: 3.3 V
- Input: 0 µA to 10 µA
- Output: 0.1 V to 3.2 V
- Bandwidth: 50 kHz

9.2.2.2 Detailed Design Procedure

The transfer function between the output voltage (V_{OUT}), the input current, (I_{IN}) and the reference voltage (V_{REF}) is defined in Equation 5.

$$V_{OUT} = I_{IN} \times R_F + V_{REF} \tag{5}$$

Where:

$$V_{REF} = V_+ \times \left(\frac{R_1 \times R_2}{R_1 + R_2} \right) \tag{6}$$

Set V_{REF} to 100 mV to meet the minimum output voltage level by setting R1 and R2 to meet the required ratio calculated in Equation 7.

$$\frac{V_{REF}}{V_+} = \frac{0.1\ V}{3.3\ V} = 0.0303 \tag{7}$$

The closest resistor ratio to meet this ratio sets R1 to 11.5 kΩ and R2 to 357 Ω.

The required feedback resistance can be calculated based on the input current and desired output voltage.

$$R_F = \frac{V_{OUT} - V_{REF}}{I_{IN}} = \frac{3.2\ V - 0.1\ V}{10\ \mu A} = 310 \frac{kV}{A} \approx 309\ k\Omega \tag{8}$$

Calculate the value for the feedback capacitor based on R_F and the desired –3-dB bandwidth, (f_{-3dB}) using Equation 9.

$$C_F = \frac{1}{2 \times \pi \times R_F \times f_{-3dB}} = \frac{1}{2 \times \pi \times 309\ k\Omega \times 50\ kHz} = 10.3\ pF \approx 10\ pF \tag{9}$$

The minimum op amp bandwidth required for this application is based on the value of R_F, C_F, and the capacitance on the INx– pin of the TLV9002-Q1 which is equal to the sum of the photodiode shunt capacitance, (CPD) the common-mode input capacitance, (CCM) and the differential input capacitance (CD) as Equation 10 shows.

$$C_{IN} = C_{PD} + C_{CM} + C_D = 47\ pF + 5\ pF + 1\ pF = 53\ pF \tag{10}$$

The minimum op amp bandwidth is calculated in Equation 11.

$$f_{=BGW} \geq \frac{C_{IN} + C_F}{2 \times \pi \times R_F \times C_F^2} \geq 324\ kHz \tag{11}$$

The 1-MHz bandwidth of the TLV900x-Q1 meets the minimum bandwidth requirement and remains stable in this application configuration.

ADVANCE INFORMATION

Typical Application (continued)

9.2.2.3 Application Curves

The measured current-to-voltage transfer function for the photodiode amplifier circuit is shown in Figure 40. The measured performance of the photodiode amplifier circuit is shown in Figure 41.

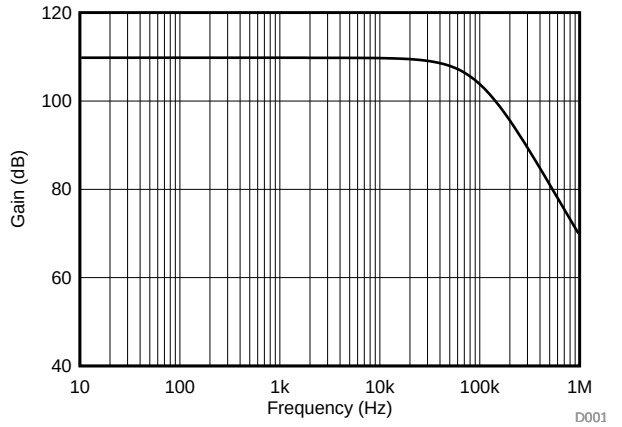


Figure 40. Photodiode Amplifier Circuit AC Gain Results

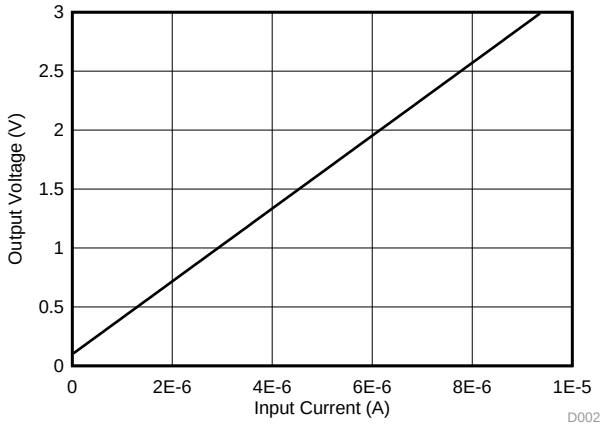


Figure 41. Photodiode Amplifier Circuit DC Results

ADVANCE INFORMATION

10 Power Supply Recommendations

The TLV900x-Q1 family is specified for operation from 1.8 V to 5.5 V (±0.9 V to ±2.75 V); many specifications apply from –40°C to 125°C. The *Typical Characteristics* section presents parameters that may exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 6 V may permanently damage the device; see the *Absolute Maximum Ratings* table.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce coupling errors from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout Guidelines* section.

10.1 Input and ESD Protection

The TLV900x-Q1 family incorporates internal ESD protection circuits on all pins. For input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA. Figure 42 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

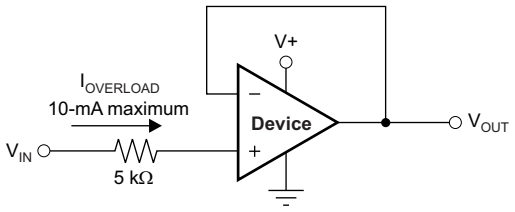


Figure 42. Input Current Protection

ADVANCE INFORMATION

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power connections of the board and propagate to the power pins of the op amp itself. Bypass capacitors are used to reduce the coupled noise by providing a low-impedance path to ground.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is adequate for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see *Circuit Board Layout Techniques*.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace at a 90 degree angle is much better as opposed to running the traces in parallel with the noisy trace.
- Place the external components as close to the device as possible, as shown in Figure 44. Keeping R_F and R_G close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring may significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

11.2 Layout Example

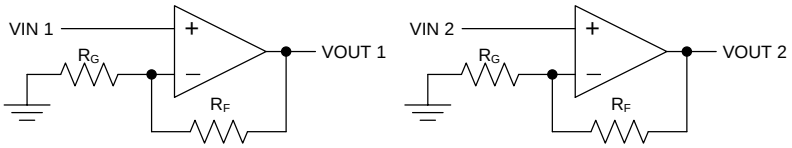


Figure 43. Schematic Representation for Figure 44

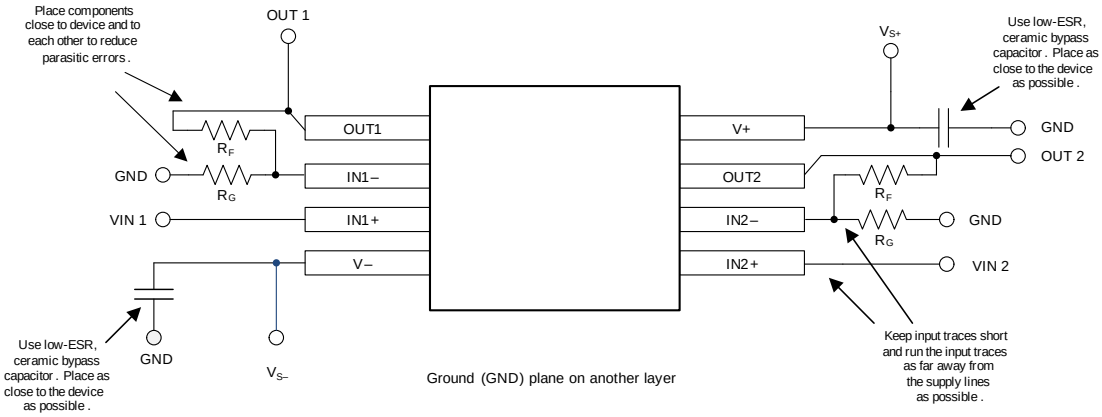


Figure 44. Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers*

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TLV9002-Q1	Click here	Click here	Click here	Click here	Click here
TLV9004-Q1	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

ADVANCE INFORMATION

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTLV9002QDRQ1	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 125		Samples
TLV9002QDRQ1	PREVIEW	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

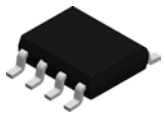
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TLV9002-Q1 :

- Catalog: TLV9002

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

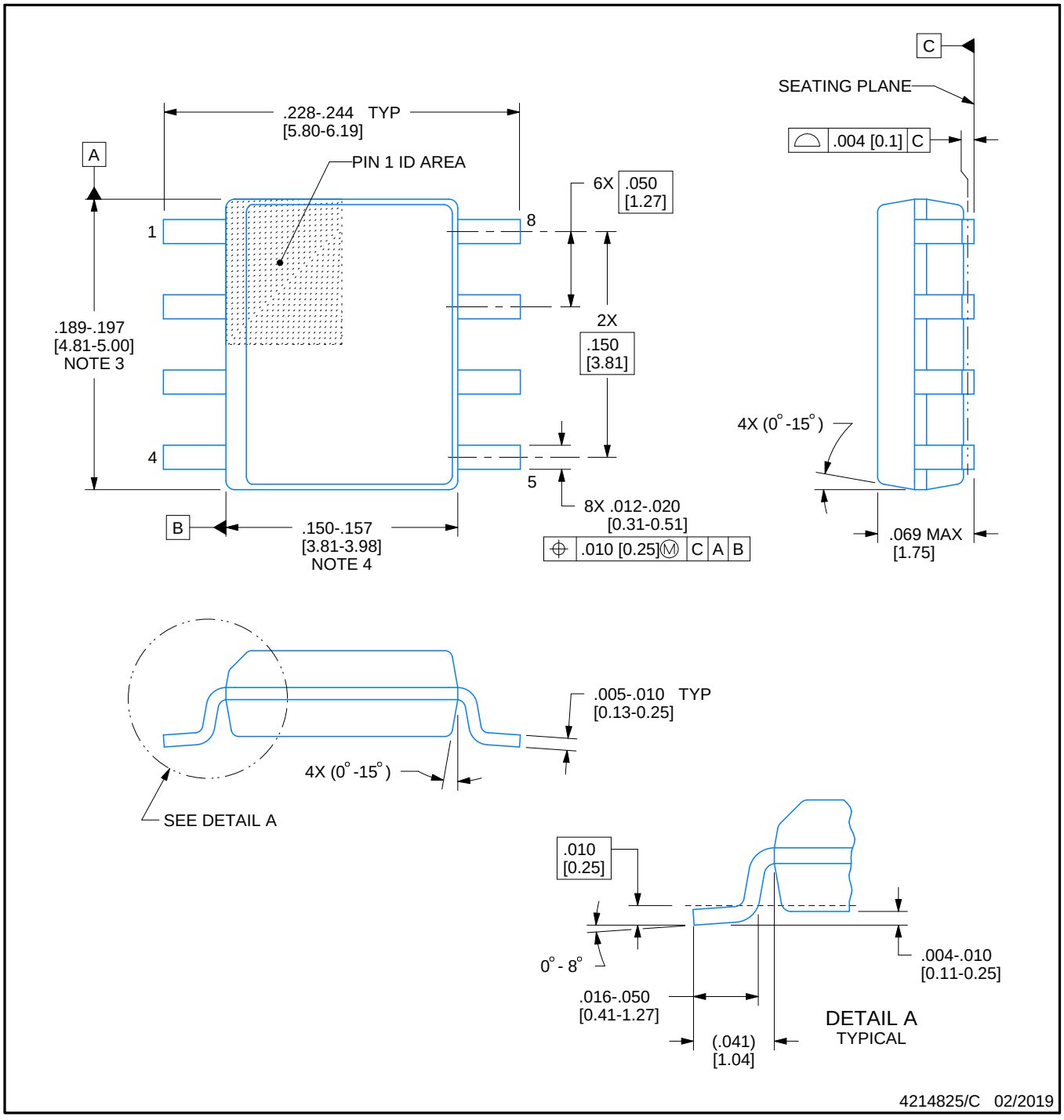


PACKAGE OUTLINE

D0008A

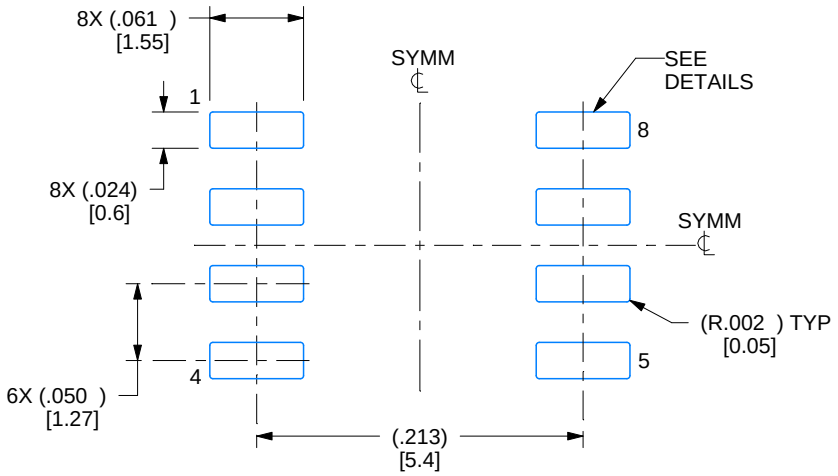
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

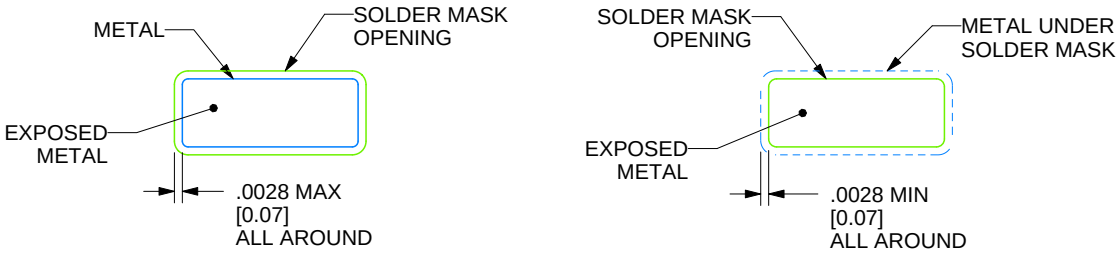


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

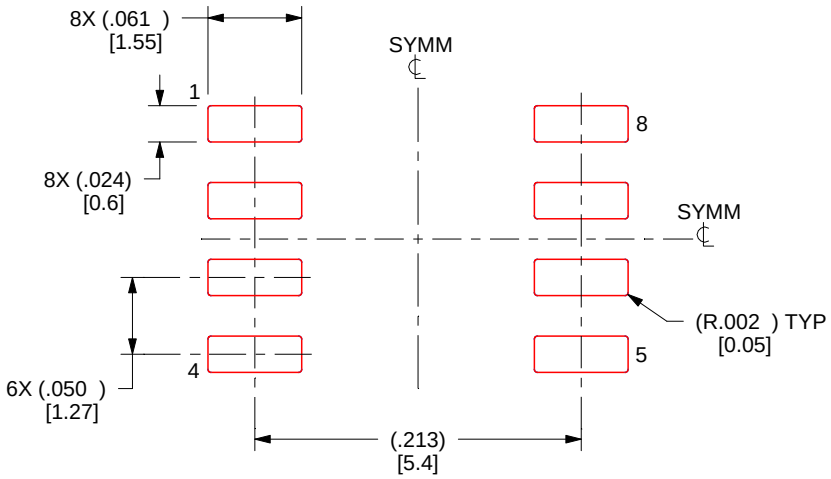
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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