1 Features

- AEC-Q100 qualified for automotive applications
  - Temperature grade 1: –40°C to +125°C, $T_A$
  - Device HBM ESD classification level 3A
  - Device CDM ESD classification level C6
- Rail-to-rail input and output
- Low input offset voltage: ±0.3 mV
- Unity-gain bandwidth: 10 MHz
- Low broadband noise: 10 nV/√Hz
- Low input bias current: 0.5 pA
- Low quiescent current: 538 µA
- Unity-gain stable
- Internal RFI and EMI filter
- Wide supply range: 1.8 V to 5.5 V
- Easier to stabilize with higher capacitive load due to resistive open-loop output impedance
- Shutdown version: TLV906xS

2 Applications

- Optimized for AEC-Q100 grade 1 applications
- Infotainment & cluster
- Passive safety
- Body electronics and lighting
- HEV/EV inverter and motor control
- On-board (OBC) & wireless charger
- Powertrain current sensor
- Advanced driver assistance systems (ADAS)
- Single-supply, low-side, unidirectional current-sensing circuit

3 Description

The TLV9062-Q1 (dual), and TLV9064-Q1 (quad) are dual-, and quad- low-voltage (1.8 V to 5.5 V) operational amplifiers (op amps) with rail-to-rail input- and output-swing capabilities. These devices are cost-effective solutions for automotive applications where low-voltage operation, a small footprint, and high capacitive load drive are required. Although the capacitive load drive of the TLV906x-Q1 is 100 pF, the resistive open-loop output impedance makes stabilizing with higher capacitive loads simpler. These op amps are designed specifically for low-voltage operation (1.8 V to 5.5 V) with performance specifications similar to the OPAx316 and TLVx316 devices, and identical to their non-automotive qualified TLV906x counterparts.

### Device Information

<table>
<thead>
<tr>
<th>PART NUMBER (1)</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLV9061S-Q1</td>
<td>SOT-23 (6)</td>
<td>1.60 mm × 2.90 mm</td>
</tr>
<tr>
<td>TLV9062-Q1</td>
<td>SOIC (8)</td>
<td>3.91 mm × 4.90 mm</td>
</tr>
<tr>
<td></td>
<td>TSSOP (8)</td>
<td>3.00 mm × 4.40 mm</td>
</tr>
<tr>
<td></td>
<td>VSSOP (8)</td>
<td>3.00 mm × 3.00 mm</td>
</tr>
<tr>
<td>TLV9064-Q1</td>
<td>SOIC (14)</td>
<td>8.65 mm × 3.91 mm</td>
</tr>
<tr>
<td></td>
<td>TSSOP (14)</td>
<td>4.40 mm × 5.00 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) Package is preview only for TLV906x-Q1.

---

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.
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2 Applications ............................................................. 1
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2020) to Revision B (September 2020) ........................................ 1
   • Deleted preview note form VSSOP (8) and TSSOP (14) package from Device Information section ............... 1
   • Added thermal information for VSSOP (8) package in Thermal Information section ................................. 7
   • Added thermal information for TSSOP (14) package in Thermal Information section ................................. 7

Changes from Revision * (April 2019) to Revision A (March 2020) ........................................ 1
   • First public release of data sheet ................................ 1
5 Description (continued)

The TLV906x-Q1 family of devices serve as general-purpose automotive amplifiers, for use in low-voltage systems requiring low noise and/or wide bandwidth.

The TLV906x-Q1 family helps simplify system design, because the family is unity-gain stable, integrates the RFI and EMI rejection filter, and provides no phase reversal in overdrive condition.

These devices are available in both dual (TLV9062-Q1), and quad (TLV9064-Q1) versions. Both versions are available in industry standard SOIC, TSSOP packages, with the dual channel also available as a VSSOP.

6 Device Comparison Table

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>NO. OF CHANNELS</th>
<th>PACKAGE LEADS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>D</td>
</tr>
<tr>
<td>TLV9061S-Q1</td>
<td>1</td>
<td>—</td>
</tr>
<tr>
<td>TLV9062-Q1</td>
<td>2</td>
<td>8</td>
</tr>
<tr>
<td>TLV9064-Q1</td>
<td>4</td>
<td>14</td>
</tr>
</tbody>
</table>
7 Pin Configuration and Functions

![Diagram of TLV9061S-Q1 DBV Package](image)

Figure 7-1. TLV9061S-Q1 DBV Package
6-Pin SOT-23
Top View

Pin Functions: TLV9061S-Q1

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>IN–</td>
<td>4</td>
<td>Inverting input</td>
</tr>
<tr>
<td>IN+</td>
<td>3</td>
<td>Noninverting input</td>
</tr>
<tr>
<td>OUT</td>
<td>1</td>
<td>Output</td>
</tr>
<tr>
<td>SHDN</td>
<td>5</td>
<td>Shutdown: low = amp disabled, high = amp enabled. See Shutdown Function section for more information.</td>
</tr>
<tr>
<td>V–</td>
<td>2</td>
<td>Negative (lowest) supply or ground (for single-supply operation)</td>
</tr>
<tr>
<td>V+</td>
<td>6</td>
<td>Positive (highest) supply</td>
</tr>
</tbody>
</table>

![Diagram of TLV9062-Q1 D, DGK, and PW Package](image)

Figure 7-2. TLV9062-Q1 D, DGK, and PW Package
8-Pin SOIC, VSSOP, and TSSOP
Top View

Pin Functions: TLV9062-Q1

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>IN1–</td>
<td>2</td>
<td>Inverting input, channel 1</td>
</tr>
<tr>
<td>IN1+</td>
<td>3</td>
<td>Noninverting input, channel 1</td>
</tr>
<tr>
<td>IN2–</td>
<td>6</td>
<td>Inverting input, channel 2</td>
</tr>
<tr>
<td>IN2+</td>
<td>5</td>
<td>Noninverting input, channel 2</td>
</tr>
<tr>
<td>OUT1</td>
<td>1</td>
<td>Output, channel 1</td>
</tr>
<tr>
<td>OUT2</td>
<td>7</td>
<td>Output, channel 2</td>
</tr>
<tr>
<td>V–</td>
<td>4</td>
<td>Negative (lowest) supply or ground (for single-supply operation)</td>
</tr>
<tr>
<td>V+</td>
<td>8</td>
<td>Positive (highest) supply</td>
</tr>
</tbody>
</table>
Figure 7-3. TLV9064-Q1 D, and PW Package
14-Pin SOIC and TSSOP
Top View

Pin Functions: TLV9064-Q1

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>IN1–</td>
<td>I</td>
<td>Inverting input, channel 1</td>
</tr>
<tr>
<td>IN1+</td>
<td>I</td>
<td>Noninverting input, channel 1</td>
</tr>
<tr>
<td>IN2–</td>
<td>I</td>
<td>Inverting input, channel 2</td>
</tr>
<tr>
<td>IN2+</td>
<td>I</td>
<td>Noninverting input, channel 2</td>
</tr>
<tr>
<td>IN3–</td>
<td>I</td>
<td>Inverting input, channel 3</td>
</tr>
<tr>
<td>IN3+</td>
<td>I</td>
<td>Noninverting input, channel 3</td>
</tr>
<tr>
<td>IN4–</td>
<td>I</td>
<td>Inverting input, channel 4</td>
</tr>
<tr>
<td>IN4+</td>
<td>I</td>
<td>Noninverting input, channel 4</td>
</tr>
<tr>
<td>NC</td>
<td>—</td>
<td>No internal connection</td>
</tr>
<tr>
<td>OUT1</td>
<td>O</td>
<td>Output, channel 1</td>
</tr>
<tr>
<td>OUT2</td>
<td>O</td>
<td>Output, channel 2</td>
</tr>
<tr>
<td>OUT3</td>
<td>O</td>
<td>Output, channel 3</td>
</tr>
<tr>
<td>OUT4</td>
<td>O</td>
<td>Output, channel 4</td>
</tr>
<tr>
<td>V–</td>
<td>I or —</td>
<td>Negative (lowest) supply or ground (for single-supply operation)</td>
</tr>
<tr>
<td>V+</td>
<td>I</td>
<td>Positive (highest) supply</td>
</tr>
</tbody>
</table>
8 Specifications

8.1 Absolute Maximum Ratings

over operating ambient temperature (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage ([V^+] – [V^-])</td>
<td>0</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>Signal input pins Voltage(^{(2)})</td>
<td>(V^+) – 0.5</td>
<td>(V+) + 0.5</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Common-mode</td>
<td>(V–) (\pm 0.2)</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Differential</td>
<td>(V+) – (V–) + 0.2</td>
<td>V</td>
</tr>
<tr>
<td>Current(^{(2)})</td>
<td>–10</td>
<td>10</td>
<td>mA</td>
</tr>
<tr>
<td>Output short-circuit(^{(3)})(^{(4)})</td>
<td>Continuous</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Temperature Specified, (T_A)</td>
<td>–40</td>
<td>125</td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td>Junction, (T_J)</td>
<td>150</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Storage, (T_{stg})</td>
<td>–65</td>
<td>150</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Input pins are diode-clamped to the power-supply rails. Current limit input signals that can swing more than 0.5 V beyond the supply rails to 10 mA or less.

(3) Short-circuit to ground, one amplifier per package.

(4) Long term continuous current limit is determined by electromigration limits.

8.2 ESD Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{(ESD)}) Electrostatic discharge</td>
<td>Human-body model (HBM), per AEC Q100-002(^{(1)})</td>
<td>±4000</td>
</tr>
<tr>
<td></td>
<td>Charged-device model (CDM), per AEC Q100-011</td>
<td>±1500</td>
</tr>
</tbody>
</table>

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with ANSI/ESDA/JEDEC JS-001 Specification.

8.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_S) Supply voltage (V_S = [V^+] – [V^-])</td>
<td>1.8</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>(V_I) Input voltage</td>
<td>((V^-) – 0.1)</td>
<td>((V+) + 0.1)</td>
<td>V</td>
</tr>
<tr>
<td>(V_O) Output voltage</td>
<td>V–</td>
<td>V+</td>
<td>V</td>
</tr>
<tr>
<td>(V_{SHDN_IH}) High level input voltage at shutdown pin (amplifier enabled)</td>
<td>1.1</td>
<td>V+</td>
<td>V</td>
</tr>
<tr>
<td>(V_{SHDN_IL}) Low level input voltage at shutdown pin (amplifier disabled)</td>
<td>V–</td>
<td>0.2</td>
<td>V</td>
</tr>
<tr>
<td>(T_A) Specified temperature</td>
<td>–40</td>
<td>125</td>
<td>°C</td>
</tr>
</tbody>
</table>

8.4 Thermal Information: TLV9061S-Q1

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1)})</th>
<th>TLV9061S-Q1 DBV (SOT-23)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(R_{\theta JA}) Junction-to-ambient thermal resistance</td>
<td>TBD</td>
<td>°C/W</td>
</tr>
<tr>
<td>(R_{\theta JC_top}) Junction-to-case (top) thermal resistance</td>
<td>TBD</td>
<td>°C/W</td>
</tr>
<tr>
<td>(R_{\theta JB}) Junction-to-board thermal resistance</td>
<td>TBD</td>
<td>°C/W</td>
</tr>
<tr>
<td>(\psi_{JT}) Junction-to-top characterization parameter</td>
<td>TBD</td>
<td>°C/W</td>
</tr>
<tr>
<td>(\psi_{JB}) Junction-to-board characterization parameter</td>
<td>TBD</td>
<td>°C/W</td>
</tr>
<tr>
<td>(R_{\theta JC_bot}) Junction-to-case (bottom) thermal resistance</td>
<td>N/A</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
8.5 Thermal Information: TLV9062-Q1

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1)})</th>
<th>TLV9062-Q1</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>D (SOIC)</td>
<td>DGK (VSSOP)</td>
<td>PW (TSSOP)</td>
</tr>
<tr>
<td>8 PINS</td>
<td>8 PINS</td>
<td>8 PINS</td>
</tr>
<tr>
<td>$R_{\text{JA}}$ Junction-to-ambient thermal resistance</td>
<td>152.0</td>
<td>198.5</td>
</tr>
<tr>
<td>$R_{\text{JC(top)}}$ Junction-to-case (top) thermal resistance</td>
<td>92.1</td>
<td>87.2</td>
</tr>
<tr>
<td>$R_{\text{JB}}$ Junction-to-board thermal resistance</td>
<td>95.6</td>
<td>120.3</td>
</tr>
<tr>
<td>$\psi_{\text{JT}}$ Junction-to-top characterization parameter</td>
<td>40.1</td>
<td>23.8</td>
</tr>
<tr>
<td>$\psi_{\text{JB}}$ Junction-to-board characterization parameter</td>
<td>94.8</td>
<td>118.7</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see Semiconductor and IC Package Thermal Metrics.

8.6 Thermal Information: TLV9064-Q1

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1)})</th>
<th>TLV9064-Q1</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>PW (TSSOP)</td>
<td>D (SOIC)</td>
</tr>
<tr>
<td>14 PINS</td>
<td>14 PINS</td>
<td></td>
</tr>
<tr>
<td>$R_{\text{JA}}$ Junction-to-ambient thermal resistance</td>
<td>133.8</td>
<td>111.1</td>
</tr>
<tr>
<td>$R_{\text{JC(top)}}$ Junction-to-case (top) thermal resistance</td>
<td>62.1</td>
<td>67.6</td>
</tr>
<tr>
<td>$R_{\text{JB}}$ Junction-to-board thermal resistance</td>
<td>76.9</td>
<td>67</td>
</tr>
<tr>
<td>$\psi_{\text{JT}}$ Junction-to-top characterization parameter</td>
<td>13.2</td>
<td>27.4</td>
</tr>
<tr>
<td>$\psi_{\text{JB}}$ Junction-to-board characterization parameter</td>
<td>76.3</td>
<td>66.6</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see Semiconductor and IC Package Thermal Metrics.
8.7 Electrical Characteristics

For $V_S$ (total supply voltage) = $(V^+) - (V^-)$ = 1.8 V to 5.5 V at $T_A = 25^\circ$C, $R_L = 10$ kΩ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>OFFSET VOLTAGE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OS}$</td>
<td>Input offset voltage</td>
<td>$V_S$ = 5 V</td>
<td>±0.3</td>
<td>±1.85</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_S$ = 5 V, $T_A = -40^\circ$C to 125$^\circ$C</td>
<td></td>
<td>±2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$dV_{OS}/dT$ Drift</td>
<td>$V_S$ = 5 V, $T_A = -40^\circ$C to 125$^\circ$C</td>
<td>±0.53</td>
<td>µV/^\circ$C</td>
<td></td>
</tr>
<tr>
<td><strong>INPUT VOLTAGE RANGE</strong></td>
<td>$V_{CM}$ Common-mode voltage range</td>
<td>$V_S$ = 1.8 V to 5.5 V</td>
<td>$(V^-) - 0.1$</td>
<td>$V_{CM} &lt; (V^+) - 1.4$</td>
<td>V</td>
</tr>
<tr>
<td>CMRR</td>
<td>Common-mode rejection ratio</td>
<td>$V_S$ = 5.5 V, $V_{CM} = -0.1$ V to 5.6 V</td>
<td>80</td>
<td>103</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_A = -40^\circ$C to 125$^\circ$C</td>
<td>57</td>
<td>75</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_S = 1.8 V, (V^-) - 0.1 V &lt; V_{CM} &lt; (V^+) - 1.4 V,$</td>
<td>88</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_A = -40^\circ$C to 125$^\circ$C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_S = 1.8 V, V_{CM} = -0.1$ V to 1.9 V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_A = -40^\circ$C to 125$^\circ$C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>INPUT BIAS CURRENT</strong></td>
<td>$I_B$ Input bias current</td>
<td>±5</td>
<td>pA</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$I_{OS}$ Input offset current</td>
<td>±5</td>
<td>pA</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>NOISE</strong></td>
<td>$E_n$ Input voltage noise (peak-to-peak)</td>
<td>$V_S = 5 V, f = 0.1$ Hz to 10 Hz</td>
<td>4.77</td>
<td>µV/√Hz</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$e_n$ Input voltage noise density</td>
<td>$V_S = 5 V, f = 10$ kHz</td>
<td>10</td>
<td>nV/√Hz</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_S = 5 V, f = 1$ kHz</td>
<td>16</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$i_n$ Input current noise density</td>
<td>$f = 1$ kHz</td>
<td>23</td>
<td>fA/√Hz</td>
<td></td>
</tr>
<tr>
<td><strong>INPUT CAPACITANCE</strong></td>
<td>$C_{ID}$ Differential</td>
<td>2</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$C_{IC}$ Common-mode</td>
<td>4</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>OPEN-LOOP GAIN</strong></td>
<td>$A_{OL}$ Open-loop voltage gain</td>
<td>$V_S = 1.8 V, (V^-) + 0.04 V &lt; V_{O} &lt; (V^+) - 0.04 V,$</td>
<td>100</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$R_L = 10$ kΩ</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_S = 5.5 V, (V^-) + 0.05 V &lt; V_{O} &lt; (V^+) - 0.05 V,$</td>
<td>104</td>
<td>130</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$R_L = 10$ kΩ</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_S = 1.8 V, (V^-) + 0.06 V &lt; V_{O} &lt; (V^+) - 0.06 V,$</td>
<td>100</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$R_L = 2$ kΩ</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_S = 5.5 V, (V^-) + 0.15 V &lt; V_{O} &lt; (V^+) - 0.15 V,$</td>
<td>130</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$R_L = 2$ kΩ</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>FREQUENCY RESPONSE</strong></td>
<td>GBP Gain bandwidth product</td>
<td>$V_S = 5 V, G = +1$</td>
<td>10</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$\phi_m$ Phase margin</td>
<td>$V_S = 5 V, G = +1$</td>
<td>55</td>
<td>°</td>
<td></td>
</tr>
<tr>
<td></td>
<td>SR Slew rate</td>
<td>$V_S = 5 V, G = +1$</td>
<td>6.5</td>
<td>V/µs</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$t_s$ Setting time</td>
<td>To 0.1%, $V_S = 5 V, 2$-V step, $G = +1, C_L = 100$ pF</td>
<td>0.5</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>To 0.01%, $V_S = 5 V, 2$-V step, $G = +1, C_L = 100$ pF</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$t_{OR}$ Overload recovery time</td>
<td>$V_S = 5 V, V_{IN} \times \text{gain} &gt; V_S$</td>
<td>0.2</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td></td>
<td>THD + N Total harmonic distortion + noise(1)</td>
<td>$V_S = 5.5 V, V_{CM} = 2.5 V, V_O = 1 V_{RMS}, G = +1,$</td>
<td>0.0008%</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$f = 1$ kHz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>OUTPUT</strong></td>
<td>$V_O$ Voltage output swing from supply rails</td>
<td>$V_S = 5.5 V, R_L = 10$ kΩ</td>
<td>20</td>
<td>mL</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_S = 5.5 V, R_L = 2$ kΩ</td>
<td>60</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$I_{SC}$ Short-circuit current</td>
<td>$V_S = 5 V$</td>
<td>±50</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$Z_O$ Open-loop output impedance</td>
<td>$V_S = 5 V, f = 10$ MHz</td>
<td>100</td>
<td>Ω</td>
<td></td>
</tr>
</tbody>
</table>
For $V_S$ (total supply voltage) = $(V+) – (V–) = 1.8$ V to 5.5 V at $T_A = 25^\circ$C, $R_L = 10$ kΩ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$ (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>POWER SUPPLY</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_Q$ Quiescent current per amplifier</td>
<td>$V_S = 5.5$ V, $I_Q = 0$ mA</td>
<td>538</td>
<td>750</td>
<td>800</td>
<td>$\mu$A</td>
</tr>
<tr>
<td></td>
<td>$V_S = 5.5$ V, $I_Q = 0$ mA $T_A = –40^\circ$C to 125$^\circ$C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>SHUTDOWN</strong> [2]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{QSD}$ Quiescent current per amplifier</td>
<td>$V_S = 1.8$ V to 5.5 V, all amplifiers disabled, $SHDN = Low$</td>
<td>0.5</td>
<td>1.5</td>
<td></td>
<td>$\mu$A</td>
</tr>
<tr>
<td>$Z_{SHDN}$ Output impedance during shutdown</td>
<td>$V_S = 1.8$ V to 5.5 V, amplifier disabled</td>
<td>10</td>
<td></td>
<td>8</td>
<td></td>
</tr>
<tr>
<td>$V_{SHDN,TH,H}$ High level voltage shutdown threshold (amplifier enabled)</td>
<td>$V_S = 1.8$ V to 5.5 V</td>
<td>$(V–) + 0.9$</td>
<td></td>
<td>$(V–) + 1.1$</td>
<td></td>
</tr>
<tr>
<td>$V_{SHDN,TH,L}$ Low level voltage shutdown threshold (amplifier disabled)</td>
<td>$V_S = 1.8$ V to 5.5 V</td>
<td>$(V–) + 0.2$</td>
<td></td>
<td>$(V–) + 0.7$</td>
<td></td>
</tr>
<tr>
<td>$t_{ON}$ Amplifier enable time (shutdown) [3]</td>
<td>$V_S = 1.8$ V to 5.5 V, full shutdown; $G = 1$, $V_{OUT} = 0.9 \times V_S/2$, $R_L$ connected to $V–$</td>
<td>10</td>
<td></td>
<td></td>
<td>$\mu$s</td>
</tr>
<tr>
<td>$t_{OFF}$ Amplifier disable time [3]</td>
<td>$V_S = 1.8$ V to 5.5 V, $G = 1$, $V_{OUT} = 0.1 \times V_S/2$, $R_L$ connected to $V–$</td>
<td>0.6</td>
<td></td>
<td></td>
<td>$\mu$s</td>
</tr>
<tr>
<td>SHDN pin input bias current (per pin)</td>
<td>$V_S = 1.8$ V to 5.5 V, $V+ \geq SHDN \geq (V+) – 0.8$ V</td>
<td>130</td>
<td></td>
<td></td>
<td>pA</td>
</tr>
<tr>
<td></td>
<td>$V_S = 1.8$ V to 5.5 V, $V– \leq SHDN \leq V– + 0.8$ V</td>
<td>40</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) Third-order filter; bandwidth = 80 kHz at −3 dB.
(2) Ensured by design and characterization; not production tested.
(3) Disable time ($t_{OFF}$) and enable time ($t_{ON}$) are defined as the time interval between the 50% point of the signal applied to the SHDN pin and the point at which the output voltage reaches the 10% (disable) or 90% (enable) level.

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8.8 Typical Characteristics

at $T_A = 25^\circ C$, $V_S = 5.5$ V, $R_L = 10$ kΩ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

**Figure 8-1. Offset Voltage Production Distribution**

**Figure 8-2. Offset Voltage Drift Distribution**

$T_A = -40^\circ C$ to $125^\circ C$

$V_+ = 2.75$ V  $V_- = -2.75$ V

**Figure 8-3. Offset Voltage vs Temperature**

**Figure 8-4. Offset Voltage vs Common-Mode Voltage**

$V_S = 1.8$ V to $5.5$ V

**Figure 8-5. Offset Voltage vs Power Supply**

$C_L = 10$ pF

**Figure 8-6. Open-Loop Gain and Phase vs Frequency**
Figure 8-7. Open-Loop Gain vs Temperature

Figure 8-8. Closed-Loop Gain vs Frequency

Figure 8-9. Input Bias Current vs Temperature

Figure 8-10. Output Voltage Swing vs Output Current

Figure 8-11. CMRR and PSRR vs Frequency (Referred to Input)

Figure 8-12. CMRR vs Temperature
**CMRR (µV/V) vs Temperature**

\[ V_{CM} = (V-) – 0.1 \, \text{V to} \, (V+) – 1.4 \, \text{V} \]

\[ T_A = -40^\circ\text{C to } 125^\circ\text{C} \quad R_L = 10 \, \text{kΩ} \quad V_S = 5.5 \, \text{V} \]

**Figure 8-13. CMRR vs Temperature**

**PSRR (µV/V) vs Temperature**

\[ V_S = 1.8 \, \text{V to } 5.5 \, \text{V} \]

**Figure 8-14. PSRR vs Temperature**

**0.1-Hz to 10-Hz Input Voltage Noise**

\[ V_S = 1.8 \, \text{V to } 5.5 \, \text{V} \]

**Figure 8-15. 0.1-Hz to 10-Hz Input Voltage Noise**

**Input Voltage Noise Spectral Density vs Frequency**

\[ V_S = 5.5 \, \text{V} \quad R_L = 2 \, \text{kΩ} \quad G = +1 \]

**Figure 8-16. Input Voltage Noise Spectral Density vs Frequency**

**THD + N vs Frequency**

\[ V_T = 5.5 \, \text{V} \quad V_{CM} = 2.5 \, \text{V} \quad R_L = 2 \, \text{kΩ} \]

**Figure 8-17. THD + N vs Frequency**

**THD + N vs Amplitude**

\[ V_S = 5.5 \, \text{V} \quad R_L = 2 \, \text{kΩ} \quad f = 1 \, \text{kHz} \]

**Figure 8-18. THD + N vs Amplitude**
### Figure 8-19. THD + N vs Amplitude

- $V_S = 5.5 \text{ V}$
- $V_{CM} = 2.5 \text{ V}$
- $R_L = 2 \text{ k}\Omega$
- $G = -1$
- $BW = 80 \text{ kHz}$
- $f = 1 \text{ kHz}$

### Figure 8-20. Quiescent Current vs Supply Voltage

- $V_{OUT} = 100 \text{ mV}_{PP}$
- $R_L = 10 \text{ k}\Omega$

### Figure 8-21. Quiescent Current vs Temperature

- $V_{OUT} = 100 \text{ mV}_{PP}$
- $R_L = 10 \text{ k}\Omega$

### Figure 8-22. Open-Loop Output Impedance vs Frequency

- $V_{OUT} = 100 \text{ mV}_{PP}$
- $R_L = 10 \text{ k}\Omega$

### Figure 8-23. Small-Signal Overshoot vs Load Capacitance

- $V_+ = 2.75 \text{ V}$
- $V_- = -2.75 \text{ V}$
- $G = +1 \text{ V/V}$

### Figure 8-24. Small-Signal Overshoot vs Load Capacitance

- $V_+ = 2.75 \text{ V}$
- $V_- = -2.75 \text{ V}$
- $G = -1 \text{ V/V}$
Figure 8-25. No Phase Reversal

Figure 8-26. Overload Recovery

Figure 8-27. Small-Signal Step Response

Figure 8-28. Large-Signal Step Response

Figure 8-29. Short-Circuit Current vs Temperature

Figure 8-30. Maximum Output Voltage vs Frequency and Supply Voltage
Figure 8-31. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency

\[ P_{RF} = -10 \text{ dBm} \]

**Figure 8-32. Channel Separation vs Frequency**

\[ V^+ = 2.75 \text{ V} \quad V^- = -2.75 \text{ V} \]

**Figure 8-33. Phase Margin vs Capacitive Load**

\[ V_S = 5.5 \text{ V} \]

**Figure 8-34. Open Loop Voltage Gain vs Output Voltage**

**Figure 8-35. Large Signal Settling Time (Positive)**

**Figure 8-36. Large Signal Settling Time (Negative)**
9 Detailed Description

9.1 Overview

The TLV906x-Q1 devices are a family of low-power, rail-to-rail input and output op amps. These devices operate from 1.8 V to 5.5 V, are unity-gain stable, and are designed for a wide range of general-purpose applications. The input common-mode voltage range includes both rails and allows the TLV906x-Q1 series to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications. The high bandwidth enables this family to drive the sample-hold circuitry of analog-to-digital converters (ADCs).

9.2 Functional Block Diagram
9.3 Feature Description

9.3.1 Rail-to-Rail Input

The input common-mode voltage range of the TLV906x-Q1 family extends 100 mV beyond the supply rails for the full supply voltage range of 1.8 V to 5.5 V. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as shown in the Functional Block Diagram section. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.4 V to 200 mV above the positive supply, whereas the P-channel pair is active for inputs from 200 mV below the negative supply to approximately (V+) – 1.4 V. There is a small transition region, typically (V+) – 1.2 V to (V+) – 1 V, in which both pairs are on. This 200-mV transition region can vary up to 200 mV with process variation. Thus, the transition region (with both stages on) can range from (V+) – 1.4 V to (V+) – 1.2 V on the low end, and up to (V+) – 1 V to (V+) – 0.8 V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can degrade compared to device operation outside this region.

9.3.2 Rail-to-Rail Output

Designed as a low-power, low-voltage operational amplifier, the TLV906x-Q1 series delivers a robust output drive capability. A class AB output stage with common-source transistors achieves full rail-to-rail output swing capability. For resistive loads of 10-kΩ, the output swings to within 15 mV of either supply rail, regardless of the applied power-supply voltage. Different load conditions change the ability of the amplifier to swing close to the rails.

9.3.3 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, because of the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return to the linear state. After the charge carriers return to the linear state, the device begins to slew at the specified slew rate. Therefore, the propagation delay (in case of an overload condition) is the sum of the overload recovery time and the slew time. The overload recovery time for the TLV906x-Q1 family is approximately 200 ns.

9.3.4 Shutdown Function

The TLV906xS-Q1 devices feature SHDN pins that disable the op amp, placing it into a low-power standby mode. In this mode, the op amp typically consumes less than 1 µA. The SHDN pins are active-low, meaning that shutdown mode is enabled when the input to the SHDN pin is a valid logic low.

The SHDN pins are referenced to the negative supply voltage of the op amp. The threshold of the shutdown feature lies around 800 mV (typical) and does not change with respect to the supply voltage. Hysteresis has been included in the switching threshold to ensure smooth switching characteristics. To ensure optimal shutdown behavior, the SHDN pins should be driven with valid logic signals. A valid logic low is defined as a voltage between V– and V– + 0.2 V. A valid logic high is defined as a voltage between V– + 1.2 V and V+. The shutdown pin must either be connected to a valid high or a low voltage or driven, and not left as an open circuit.

The SHDN pins are high-impedance CMOS inputs. Dual op amp versions are independently controlled, and quad op amp versions are controlled in pairs with logic inputs. For battery-operated applications, this feature may be used to greatly reduce the average current and extend battery life. The enable time is 10 µs for full shutdown of all channels; disable time is 3 µs. When disabled, the output assumes a high-impedance state. This architecture allows the TLV906xS-Q1 to be operated as a gated amplifier (or to have the device output multiplexed onto a common analog output bus). Shutdown time (tOFF) depends on loading conditions and increases as load resistance increases. To ensure shutdown (disable) within a specific shutdown time, the specified 10-kΩ load to midsupply (V_S / 2) is required. If using the TLV906xS-Q1 without a load, the resulting turnoff time is significantly increased.

9.4 Device Functional Modes

Devices in the TLV906x-Q1 family are operational when the power-supply voltage is between 1.8 V (±0.9 V) and 5.5 V (±2.75 V). The TLV906xS devices feature a shutdown mode and are shut down when a valid logic low is applied to the shutdown pin.
10 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TLV906x-Q1 family features 10-MHz bandwidth and 6.5-V/µs slew rate with only 538 µA of supply current per channel, providing good AC performance at very low power consumption. DC applications are well served with a very low input noise voltage of 10 nV/√Hz at 10 kHz, low input bias current, and a typical input offset voltage of 0.3 mV.

10.2 Typical Applications

10.2.1 Typical Low-Side Current Sense Application

*Figure 10-1* shows the TLV906x-Q1 configured in a low-side current-sensing application.

![Figure 10-1. TLV906x-Q1 in a Low-Side, Current-Sensing Application](image)

**10.2.1.1 Design Requirements**

The design requirements for this design are:

- Load current: 0 A to 1 A
- Output voltage: 4.95 V
- Maximum shunt voltage: 100 mV
10.2.1.2 Detailed Design Procedure

The transfer function of the circuit in Figure 10-1 is given in Equation 1.

\[ V_{OUT} = I_{LOAD} \times R_{SHUNT} \times \text{Gain} \]  

(1)

The load current \((I_{LOAD})\) produces a voltage drop across the shunt resistor \((R_{SHUNT})\). The load current is set from 0 A to 1 A. To keep the shunt voltage below 100 mV at maximum load current, the largest shunt resistor is defined using Equation 2.

\[ R_{SHUNT} = \frac{V_{SHUNT\_MAX}}{I_{LOAD\_MAX}} = \frac{100\text{mV}}{1\text{A}} = 100\text{mΩ} \]  

(2)

Using Equation 2, \(R_{SHUNT}\) equals 100 mΩ. The voltage drop produced by \(I_{LOAD}\) and \(R_{SHUNT}\) is amplified by the TLV906x-Q1 to produce an output voltage of approximately 0 V to 4.95 V. Equation 3 calculates the gain required for the TLV906x-Q1 to produce the required output voltage.

\[ \text{Gain} = \frac{(V_{OUT\_MAX} - V_{OUT\_MIN})}{(V_{IN\_MAX} - V_{IN\_MIN})} \]  

(3)

Using Equation 3, the required gain equals 49.5 V/V, which is set with the \(R_F\) and \(R_G\) resistors. Equation 4 sizes the \(R_F\) and \(R_G\) resistors to set the gain of the TLV906x-Q1 to 49.5 V/V.

\[ \text{Gain} = 1 + \left( \frac{R_F}{R_G} \right) \]  

(4)

Selecting \(R_F\) to equal 165 kΩ and \(R_G\) to equal 3.4 kΩ provides a combination that equals approximately 49.5 V/V. Figure 10-2 shows the measured transfer function of the circuit shown in Figure 10-1. Notice that the gain is only a function of the feedback and gain resistors. This gain is adjusted by varying the ratio of the resistors and the actual resistor values are determined by the impedance levels that the designer wants to establish. The impedance level determines the current drain, the effect that stray capacitance has, and a few other behaviors. There is no optimal impedance selection that works for every system, you must choose an impedance that is ideal for your system parameters.

10.2.1.3 Application Curve

![Figure 10-2. Low-Side, Current-Sense, Transfer Function](image-url)
10.2.2 Typical Comparator Application

Comparators are used to differentiate between two different signal levels. For example, a comparator can be used to differentiate between an overvoltage situation and normal operation. The TLV9062-Q1 can be used as a comparator by applying the two voltages being compared to each input without any feedback from output to inverting input.

The TLV9062-Q1 features a rail-to-rail input and output stage with an input common-mode range that exceeds the supply rails by 100 mV. The TLV9062-Q1 is designed to prevent phase reversal over the entire input common-mode range. The propagation delay for the TLV9062-Q1 used as a comparator is equal to the overload recovery time plus the slew rate. Overdrive voltages less than 100 mV result in longer propagation delays because the overload recovery time increases and the slew rate decreases.

![Figure 10-3. Typical Comparator Application](image)

10.2.2.1 Design Requirements

The design requirements for this design are:

- Supply voltage ($V_+$): 5 V
- Input ($V_{IN}$): 0 V–5 V
- Threshold voltage ($V_{TH}$): 2.5 V

10.2.2.2 Detailed Design Procedure

The inverting comparator circuit applies the input voltage ($V_{IN}$) to the inverting terminal of the op amp. Two resistors ($R_1$ and $R_2$) divide the supply voltage ($V_{CC}$) to create a midsupply threshold voltage ($V_{TH}$) as calculated in Equation 1. The circuit is shown in Figure 10-3. When $V_{IN}$ is less than $V_{TH}$, the output voltage transitions to the positive supply and equals the high-level output voltage. When $V_{IN}$ is greater than $V_{TH}$, the output voltage transitions to the negative supply and equals the low-level output voltage, $V_{TH}$.

\[
V_{TH} = \frac{R_2}{R_1 + R_2} \times V_+ = 2.5V
\] (5)
10.2.2.3 Application Curves

Figure 10-4. Comparator Response to Input Voltage (Propagation Delay Included)

Figure 10-5. Rising Edge

Figure 10-6. Falling Edge

Figure 10-7. Falling Edge Propagation Delay vs Input Overdrive Voltage
11 Power Supply Recommendations

The TLV906x-Q1 series is specified for operation from 1.8 V to 5.5 V (±0.9 V to ±2.75 V); many specifications apply from –40°C to 125°C. The Typical Characteristics section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

**CAUTION**

Supply voltages larger than 6 V can permanently damage the device; see the Absolute Maximum Ratings table.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the Layout section.

### 11.1 Input and ESD Protection

The TLV906x-Q1 series incorporates internal ESD protection circuits on all pins. For input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA, as shown in the Absolute Maximum Ratings table. Figure 11-1 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

![Figure 11-1. Input Current Protection](image-url)
12 Layout

12.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of the op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is adequate for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace at a 90 degree angle is much better as opposed to running the traces in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in Figure 12-2, keeping $R_F$ and $R_G$ close to the inverting input minimizes parasitic capacitance on the inverting input.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.
12.2 Layout Example

Figure 12-1. Schematic Representation for

Ground (GND) plane on another layer
Keep input traces short and run the input traces as far away from the supply lines as possible.

Use low-ESR, ceramic bypass capacitor. Place as close to the device as possible.

Place components close to device and to each other to reduce parasitic errors.

Figure 12-2. Layout Example
13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

Texas Instruments, **TLVx313-Q1 Low-Power, Rail-to-Rail In/Out, 500-μV Typical Offset, 1-MHz Operational Amplifier for Cost-Sensitive Systems** data sheet.

Texas Instruments, **TLVx314-Q1 3-MHz, Low-Power, Internal EMI Filter, RRIO, Operational Amplifier** data sheet.

Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers* application report.

Texas Instruments, *QFN/SON PCB Attachment* application report.


13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

<table>
<thead>
<tr>
<th>PARTS</th>
<th>PRODUCT FOLDER</th>
<th>ORDER NOW</th>
<th>TECHNICAL DOCUMENTS</th>
<th>TOOLS &amp; SOFTWARE</th>
<th>SUPPORT &amp; COMMUNITY</th>
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</thead>
<tbody>
<tr>
<td>TLV9062-Q1</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
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<td>TLV9064-Q1</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
</tr>
</tbody>
</table>

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Support Resources

**TI E2E™ support forums** are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

13.5 Trademarks

**TI E2E™** is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

13.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.7 Glossary

**TI Glossary** This glossary lists and explains terms, acronyms, and definitions.
14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
# PACKAGING INFORMATION

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<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead finish/ Ball material</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
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<td>DGK</td>
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<td>VSSOP</td>
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<td>NIPDAU</td>
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<td>2500</td>
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<td>T9064Q</td>
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</table>

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Meaning contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Meaning for that device.
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV9062-Q1, TLV9064-Q1:

- Catalog: TLV9062, TLV9064

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
**TAPE AND REEL INFORMATION**

---

### TAPE DIMENSIONS

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

---

### REEL DIMENSIONS

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### PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal*

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<thead>
<tr>
<th>Device</th>
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*All dimensions are nominal*
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.
E. Reference JEDEC MS-012 variation AB.

4040047-5/M 06/11
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
\[ \text{Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 each side.} \]
\[ \text{Body width does not include interlead flash. Interlead flash shall not exceed 0.25 each side.} \]
E. Falls within JEDEC MO-153

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NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.

2. This drawing is subject to change without notice.

3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.

4. This dimension does not include interlead flash.

5. Reference JEDEC registration MS-012, variation AA.
EXAMPLE BOARD LAYOUT

NOTE: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.
MECHANICAL DATA

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO-187 variation AA, except interlead flash.

4073329/E 05/06
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
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